

**IBIS EVOLUTION**  
**(IBIS, PACKAGE, ELECTRICAL BOARD DESCRIPTION, EMI, SSO, ALGORITHMIC MODELING INTERFACE)**  
**Bob Ross, July 25, 2006, updated September 14, 2007, September 8, 2013, April 20, 2014, July 31, 2015, July 21, 2016, July, 19, 2018, March 15, 2019, December 21, 2021**

**HEADER SECTION (.ibs, .pkg, .ebd, .ims, .emd, .ems)**

Version 1.1	Version 2.1 (.ibs, .pkg)	Version 3.2 (.ebd)	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0 (.ims)	Version 7.1 (.emd, .ems)
[IBIS Ver]	[Copyright]						
[Comment Char] (re-defined anywhere in file)							
[File Name]							
[File Rev]							
[Date]							
[Source]							
[Notes]							
[Disclaimer]							

**TOP-LEVEL KEYWORDS (with END Keywords)**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
[Component]	[Define Package Model] (.ibs, .pkg)	[Model Selector]	[External Circuit]	[Test Load] (defined under [Model] in 4.2)		[Interconnect Model Set] (.ims)	[Begin EMD] (.emd)
[Model]	[End Package Model] (.ibs, .pkg)	[Submodel]	[End External Circuit]	[Test Data] (defined under [Test Load] in 4.2)		[End Interconnect Model Set] (.ims)	[End EMD] (.emd)
[End] (.ibs)	[End] (.pkg)	[Begin Board Description] (.ebd)				[End] (.ims)	[End] (.emd)
		[End Board Description] (.ebd)					[EMD Set] (.ems).
		[End] (.ebd)					[End EMD Set] (.ems)
							[End] (.ems)

**[Component] PINOUT AND PACKAGE SECTION**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
[Component]	[Pin Mapping]	[Series Pin Mapping]	[Alternate Package Models]	[Begin EMI Component]	[Repeater Pin]	[Interconnect Model Group]	[Clock Pins]
[Manufacturer]	[Diff Pin]	[Series Switch Groups]	[End Alternate Package Models]	[End EMI Component]		[Bus Label]	[PDN Domain]
[Package]	[Package Model]		[Node Declarations]			[Die Supply Pads]	[End PDN Domain]
[Pin]			[End Node Declarations]				[PDN Model]
			[Circuit Call]				[End PDN Model]
			[End Circuit Call]				

**[Model] SECTION**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
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[Model]	[Temperature Range]	[Model Spec]	[Receiver Thresholds]	[Begin EMI Model]	[Initial Delay]*		[C Comp Model]
[Voltage Range]	[Pullup Reference]	[Driver Schedule]	[External Reference]	[End EMI Model]			[End C Comp Model]
[Pulldown]	[Pulldown Reference]	[TTgnd]	[Test Data]	[Algorithmic Model]			
[Pullup]	[POWER Clamp Reference]	[TTpower]	[Rising Waveform Near]	[End Algorithmic Model]			
[GND Clamp]	[GND Clamp Reference]	[On]	[Falling Waveform Near]	[ISSO PU]			
[POWER Clamp]	[Rgnd]	[Off]	[Rising Waveform Far]	[ISSO PD]			
[Ramp]	[Rpower]	[R Series]	[Falling Waveform Far]	[Composite Current] (under [Rising Waveform])			
	[Rac]	[L Series]	[Diff Rising Waveform Near]	[Composite Current] (under Falling Waveform)			
	[Cac]	[Rl Series]	[Diff Falling Waveform Near]	[C Comp Corner]			
	[Rising Waveform]	[C Series]	[Diff Rising Waveform Far]				
	[Falling Waveform]	[Lc Series]	[Diff Falling Waveform Far]				
		[Rc Series]	[Test Load]				
		[Series Current]	[External Model]				
		[Series MOSFET]	[End External Model]				
		[Add Submodel]					

**[Submodel] SECTION**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
		[Submodel]			[Initial Delay]*		
		[Pullup] (1.1)					
		[Pulldown] (1.1)					
		[GND Clamp] (1.1)					
		[POWER Clamp] (1.1)					
		[Ramp] (1.1)					
		[Rising Waveform] (2.1)					
		[Falling Waveform] (2.1)					
		[Submodel Spec]					
		[GND Pulse Table]					
		[POWER Pulse Table]					

**PACKAGE MODEL DEFINITION (within .jbs or as .pkg)**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
	[Define Package Model]	[Number Of Sections]			[Merged Pins]*		
	[Manufacturer] (1.1)						
	[OEM]						
	[Description]						
	[Number Of Pins]						
	[Pin Numbers]						

	[Model Data]						
	[End Model Data]						
	[Resistance Matrix]						
	[Inductance Matrix]						
	[Capacitance Matrix]						
	[Row]						
	[Bandwidth]						
	[End Package Model]						

**ELECTRICAL BOARD DESCRIPTION (.ebd)**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
		[Begin Board Description]					
		[Manufacturer] (1.1)					
		[Number Of Pins] (1.1)					
		[Pin List]					
		[Path Description]					
		[Reference Designator Map]					
		[End Board Description]					

**INTERCONNECT MODEL SET (within .ibs or .ims)**

						[Interconnect Model Set]	
						[Manufacturer] (1.1)	
						[Description] (2.1)	
						[Interconnect Model]	
						[End Interconnect Model]	
						[End Interconnect Set]	

**[Model] SUBPARAMETERS**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
Polarity	Cref		C_comp_pullup				
Enable	Rref		C_comp_pulldown				
Model_type	Vref		C_comp_power_clamp				
C_comp	Vmeas		C_comp_gnd_clamp				
Vinh			Rref_diff				
Vinl			Cref_diff				

**Model\_type SELECTIONS**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
Input	Open_sink	3-state_ECL	Input_diff				
Output	Open_source	Series	Output_diff				
3-state	I/O_open_drain	Series_switch	3-state_diff				
Open_drain	I/O_open_sink		I/O_diff				
I/O	I/O_open_source						
	Input_ECL						
	Output_ECL						

	I/O_ECL						
	Terminator						
<b>[Model Spec] SUBPARAMETERS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
		Vinh	Cref	Weak_R			
		Vinl	Rref	Weak_I			
		Vinh+	Vref	Weak_V			
		Vinh-	Cref_rising	D_overshoot_area_h			
		Vinl+	Cref_falling	D_overshoot_area_l			
		Vinl-	Rref_rising	D_overshoot_ampl_h			
		S_overshoot_high	Rref_falling	D_overshoot_ampl_l			
		S_overshoot_low	Vref_rising				
		D_overshoot_high	Vref_falling				
		D_overshoot_low	Vmeas_rising				
		D_overshoot_time	Vmeas_falling				
		Pulse_high	Rref_diff				
		Pulse_low	Cref_diff				
		Pulse_time					
		V_meas					
<b>[Submodel] SUBPARAMETER</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
		Submodel_type					
<b>Submodel_type SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
		Dynamic_clamp	Fall_back				
		Bus_hold					
<b>[Submodel Spec] SUBPARAMETERS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
		V_trigger_r					
		V_trigger_f					
		Off_delay					
<b>[C Comp Model] SUBPARAMETERS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
							C_comp_model_mode
							Param
							File_TS
							File_IBIS-ISS
							Number_of_terminals (7.0)
<b>[Interconnect Model] SUBPARAMETERS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1

						Param	
						File_TS	
						File_IBIS-ISS	
						Unused_port_termination	
						Number_of_terminals	
<b>[Interconnect Model] Unused_port_termination SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
						Reference	
						Open	
						Resistance	
<b>[C Comp Model] Terminal_type COLUMN SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
							Buffer_I/O (7.0)
							Buffer_I
							Pullup_ref (7.0)
							Pulldown_ref (7.0)
							Power_clamp_ref (7.0)
							Gnd_clamp_ref (7.0)
							Ext_ref (7.0)
							A_gnd (7.0)
<b>[interconnect Model] Terminal_type COLUMN SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
						Pin_I/O	
						Pad_I/O	
						Buffer_I/O	
						Pin_Rail	
						Pad_Rail	
						Buffer_Rail	
						Pullup_ref	
						Pulldown_ref	
						Power_clamp_ref	
						Gnd_clamp_ref	
						Ext_ref	
						A_gnd	
<b>[EMD Model] Terminal_type COLUMN SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
							Pin_I/O (7.0)
							Pin_Rail (7.0)
							A_gnd (7.0)
<b>[Interconnect Model] Terminal_type_qualifiers COLUMN SELECTION</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
						pin_name	

						signal_name	
						bus_label	
						pad_name	
<b>[EMD Model] Terminal_type_qualifiers COLUMN SELECTION</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
							pin_name (7.0)
							signal_name (7.0)
							bus_label (7.0)
<b>[Interconnect Model] Aggressor_Only COLUMN SELECTION</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
						Aggressor_Only	
<b>[EMD Model] Aggressor_Only COLUMN SELECTION</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
							Aggressor_Only (7.0)
<b>Test_data_type and Test_load_type SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
			Single_ended				
			Differential				
<b>[Begin EMI Component] KEYWORDS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
				[Pin EMI]			
				[Pin Domain EMI]			
<b>Model_emi_type SELECTIONS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
				Ferrite			
				Not_a_Ferrite			
<b>(SUBPARAMETERS) FOR OTHER KEYWORDS</b>							
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
[Component]		[Component] (Si_location, Timing_location)		[Begin EMI Component] (Domain, Cpd, C_Heatsink_gnd, C_Heatsink_float)	[Repeater Pin] (tx_non_inv_pin) [Initial Delay] (V-T, I-T)*		[Clock Pins] (clocked_pins, relationship)
[Package] (R_pkg, L_pkg, C_pkg)				[Pin EMI] (domain_name, clock_div)			[PDN Domain] (Bus_label, Signal_name)
[Pin] (signal_name, model_name, R_pin, L_pin, C_pin)				[Pin Domain EMI] (percentage)			[PDN Model] (R_pdn, C_pdn, R_leak)

	[Pin Mapping] (pulldown_ref, pullup_ref, gnd_clamp_ref, power_clamp_ref)		[Pin Mapping] (ext_ref)	[Begin EMI Model] (Model_emi_type, Model_Domain)		[Bus Label] (signal_pin)	
						[Die Supply Pads] (signal_pin, bus_label)	
	[Diff Pin] (inv_pin, vdiff, t_delay, tdelay_min, tdelay_max)			[Algorithmic Model] (Executable)	[Algorithmic Model] (Executable_Rx*, Executable_Tx*)		
		[Series Pin Mapping] (pin_2, model_name, function_table_group)		[C Comp Corner] (C_comp, C_comp_pullup, C_comp_pulldown, C_comp_power_clamp, C_comp_gnd_clamp)			
		[Series Switch Groups] (On, Off)					
			[Circuit Call] (Signal_pin, Diff_signal_pins, Series_pins, Port_map)			[Circuit Call] (Parameters) (4.2), (Converter_Parameters) (6.0)	
			[Receiver Thresholds] (Vth, Vth_min, Vth_max, Vinh_ac, Vinh_dc, Vinl_ac, Vinl_dc, Threshold_sensitivity, Reference_supply, Vcross_low, V_cross_high, Vdiff_ac, Vdiff_dc, Tslew_ac, Tdiffslew_ac)				
		[Series MOSFET] (Vds)					
[Ramp] (dV/dt_r, dV/dt_f)	[Ramp] (R_load)						
	[Rising Waveform] (R_fixture, V_fixture, V_fixture_min, V_fixture_max, C_fixture, L_fixture, R_dut, L_dut, C_dut)						
	[Falling Waveform] (R_fixture, V_fixture, V_fixture_min, V_fixture_max, C_fixture, L_fixture, R_dut, L_dut, C_dut)						
			[Test Data] (Test_data_type, Driver_model,				

			Driver_model_inv, Test_load) (moved to top-level in 5.1)				
			[Test Load] (Test_load_type, C1_near, Rs_near, Ls_near, C2_near, Rp1_near, Rp2_near, Td, Zo, Rpl_far, Rp2_far, C1_far, Ls_far, Rs_far, V_term1, V_term2, Receiver_model, Receiver_model_inv, R_diff_near, R_diff_far) (moved to top-level in 5.1)				
			[External Model] (Language, Corner, Parameters, Ports, D_to_A, A_to_D)		[External Model] (Converter_Parameters)		
			[External Circuit] (Language, Corner, Parameters, Ports, D_to_A, A_to_D)		[External Circuit] (Converter_Parameters)		
	[Pin Numbers]	[Pin Numbers] (Len, L, C, R, Fork, Endfork)					
		[Pin List] (signal_name)					
		[Begin Board Description] (Len, L, C, R, Fork, Endfork, Node, Pin)					

**OTHER NOTABLE CHANGES**

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0	Version 7.1
File width = 80			File width = 120			File width = 1024	
Filename length = 8		Filename length = 20	Filename length = 40			Filename length = 60, filename case-insensitive	
						File_reference linkage includes subdirectories	
Model name length = 20			Model name length = 40				
		Submodel name length = 20	Submodel name length = 40				
	[Rising Waveform], [Falling Waveform] rows = 100		[Rising Waveform], [Falling Waveform] rows = 1000				
Vinh, Vinl optional for Input and I/O	Vinh, Vinl required for Input and I/O						



Reserved words NC POWER, GND, NA			Added reserved word CIRCUITCALL				
Fixed keyword space and underbar convention	Space and underbar equivalent in keywords						
Original comment characters	+, - removed as comment characters						
Multipliers M, k, m, u, n, p	Multipliers T, G and f added						
Buffers by extraction		By construction added	By language linkage added	EMI, SSO, and Algorithmic Modeling Interface added, [Test Load] and [Test Data] hierarchy changed	PAM4 mapping and other IBIS-AMI parameters	Interconnect Modeling, linkage to IBIS-ISS, and Touchstone; Files references with paths; Backchannel (BCI);, more IBIS-AMI parameters, linkage to 4-port Touchstone	Electrical Module Description and EMD Set files added, [Clocked Pins], [C Comp Model], [PDN Domain] added