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| **IBIS EVOLUTION**  **(IBIS, PACKAGE, ELECTRICAL BOARD DESCRIPTION, EMI, SSO, ALGORITHMIC MODELING INTERFACE)**  **Bob Ross, July 25, 2006, updated September 14, 2007, September 8, 2013, April 20, 2014, July 31, 2015, July 21, 2016, July, 19, 2018, March 15, 2019, December 21, 2021** | | | | | | | |
| **HEADER SECTION (.ibs, .pkg, .ebd, .ims, .emd, .ems)** | | | | | | | |
| Version 1.1 | Version 2.1 (.ibs, .pkg) | Version 3.2 (.ebd) | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | Version 7.0 (.ims) | Version 7.1 (.emd, .ems) |
| [IBIS Ver] | [Copyright] |  | x |  |  |  |  |
| [Comment Char]  (re-defined anywhere in file) |  |  |  |  |  |  |  |
| [File Name] |  |  |  |  |  |  |  |
| [File Rev] |  |  |  |  |  |  |  |
| [Date] |  |  |  |  |  |  |  |
| [Source] |  |  |  |  |  |  |  |
| [Notes] |  |  |  |  |  |  |  |
| [Disclaimer] |  |  |  |  |  |  |  |

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| **TOP-LEVEL KEYWORDS (with END Keywords)** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
| [Component] | [Define Package Model] (.ibs, .pkg) | [Model Selector] | [External Circuit] | [Test Load]  (defined under [Model] in 4.2) |  | | [Interconnect Model Set] (.ims) | [Begin EMD] (.emd) |
| [Model] | [End Package Model] (.ibs, .pkg) | [Submodel] | [End External Circuit] | [Test Data]  (defined under [Test Load] in 4.2) |  | | [End Interconnect Model Set] (.ims) | [End EMD] (.emd) |
| [End] (.ibs) | [End] (.pkg) | [Begin Board  Description] (.ebd) |  |  |  | | [End] (.ims) | [End] (.emd) |
|  |  | [End Board  Description] (.ebd) |  |  |  | |  | [EMD Set] (.ems). |
|  |  | [End] (.ebd) |  |  |  | |  | [End EMD Set] (.ems) |
|  |  |  |  |  |  | |  | [End] (.ems) |
| **[Component] PINOUT AND PACKAGE SECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
| [Component] | [Pin Mapping] | [Series Pin Mapping] | [Alternate Package Models] | [Begin EMI Component] | [Repeater Pin] | | [Interconnect Model Group] | [Clock Pins] |
| [Manufacturer] | [Diff Pin] | [Series Switch Groups] | [End Alternate Package Models] | [End EMI Component] |  | | [Bus Label] | [PDN Domain] |
| [Package] | [Package Model] |  | [Node Declarations] |  |  | | [Die Supply Pads] | [End PDN Domain] |
| [Pin] |  |  | [End Node Declarations] |  |  | |  | [PDN Model] |
|  |  |  | [Circuit Call] |  |  | |  | [End PDN Model] |
|  |  |  | [End Circuit Call] |  |  | |  |  |
| **[Model] SECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
| [Model] | [Temperature Range] | [Model Spec] | [Receiver Thresholds] | [Begin EMI Model] | [Initial Delay]\* | |  | [C Comp Model] |
| [Voltage Range] | [Pullup Reference] | [Driver Schedule] | [External Reference] | [End EMI Model] |  | |  | [End C Comp Model] |
| [Pulldown] | [Pulldown Reference] | [TTgnd] | [Test Data] | [Algorithmic Model] |  | |  |  |
| [Pullup] | [POWER Clamp  Reference] | [TTpower] | [Rising Waveform Near] | [End Algorithmic Model] |  | |  |  |
| [GND Clamp] | [GND Clamp  Reference] | [On] | [Falling Waveform Near] | [ISSO PU] |  | |  |  |
| [POWER Clamp] | [Rgnd] | [Off] | [Rising Waveform Far] | [ISSO PD] |  | |  |  |
| [Ramp] | [Rpower] | [R Series] | [Falling Waveform Far] | [Composite Current] (under [Rising Waveform]) |  | |  |  |
|  | [Rac] | [L Series] | [Diff Rising Waveform Near] | [Composite Current] (under Falling Waveform]) |  | |  |  |
|  | [Cac] | [Rl Series] | [Diff Falling Waveform Near] | [C Comp Corner] |  | |  |  |
|  | [Rising Waveform] | [C Series] | [Diff Rising Waveform Far] |  |  | |  |  |
|  | [Falling Waveform] | [Lc Series] | [Diff Falling Waveform Far] |  |  | |  |  |
|  |  | [Rc Series] | [Test Load] |  |  | |  |  |
|  |  | [Series Current] | [External Model] |  |  | |  |  |
|  |  | [Series MOSFET] | [End External Model] |  |  | |  |  |
|  |  | [Add Submodel] |  |  |  | |  |  |
| **[Submodel] SECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  | [Submodel] |  |  | [Initial Delay]\* | |  |  |
|  |  | [Pullup] (1.1) |  |  |  | |  |  |
|  |  | [Pulldown] (1.1) |  |  |  | |  |  |
|  |  | [GND Clamp] (1.1) |  |  |  | |  |  |
|  |  | [POWER Clamp] (1.1) |  |  |  | |  |  |
|  |  | [Ramp] (1.1) |  |  |  | |  |  |
|  |  | [Rising Waveform] (2.1) |  |  |  | |  |  |
|  |  | [Falling Waveform]  (2.1) |  |  |  | |  |  |
|  |  | [Submodel Spec] |  |  |  | |  |  |
|  |  | [GND Pulse Table] |  |  |  | |  |  |
|  |  | [POWER Pulse  Table] |  |  |  | |  |  |
| **PACKAGE MODEL DEFINITION (within .ibs or as .pkg)** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  | [Define Package Model] | [Number Of Sections] |  |  | [Merged Pins]\* | |  |  |
|  | [Manufacturer] (1.1) |  |  |  |  | |  |  |
|  | [OEM] |  |  |  |  | |  |  |
|  | [Description] |  |  |  |  | |  |  |
|  | [Number Of Pins] |  |  |  |  | |  |  |
|  | [Pin Numbers] |  |  |  |  | |  |  |
|  | [Model Data] |  |  |  |  | |  |  |
|  | [End Model Data] |  |  |  |  | |  |  |
|  | [Resistance Matrix] |  |  |  |  | |  |  |
|  | [Inductance Matrix] |  |  |  |  | |  |  |
|  | [Capacitance Matrix] |  |  |  |  | |  |  |
|  | [Row] |  |  |  |  | |  |  |
|  | [Bandwidth] |  |  |  |  | |  |  |
|  | [End Package Model] |  |  |  |  | |  |  |
| **ELECTRICAL BOARD DESCRIPTION (.ebd)** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  | [Begin Board  Description] |  |  |  | |  |  |
|  |  | [Manufacturer] (1.1) |  |  |  | |  |  |
|  |  | [Number Of Pins] (1.1) |  |  |  | |  |  |
|  |  | [Pin List] |  |  |  | |  |  |
|  |  | [Path Description] |  |  |  | |  |  |
|  |  | [Reference Designator  Map] |  |  |  | |  |  |
|  |  | [End Board Description] |  |  |  | |  |  |
| **INTERCONNECT MODEL SET (within .ibs or .ims)** | | | | | | | | |
|  |  |  |  |  |  | | [Interconnect Model Set] |  |
|  |  |  |  |  |  | | [Manufacturer] (1.1) |  |
|  |  |  |  |  |  | | [Description] (2.1) |  |
|  |  |  |  |  |  | | [Interconnect Model] |  |
|  |  |  |  |  |  | | [End Interconnect Model] |  |
|  |  |  |  |  |  | | [End Interconnect Set] |  |
| **[Model] SUBPARAMETERS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
| Polarity | Cref |  | C\_comp\_pullup |  |  | |  |  |
| Enable | Rref |  | C\_comp\_pulldown |  |  | |  |  |
| Model\_type | Vref |  | C\_comp\_power\_clamp |  |  | |  |  |
| C\_comp | Vmeas |  | C\_comp\_gnd\_clamp |  |  | |  |  |
| Vinh |  |  | Rref\_diff |  |  | |  |  |
| Vinl |  |  | Cref\_diff |  |  | |  |  |
| **Model\_type SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
| Input | Open\_sink | 3-state\_ECL | Input\_diff |  |  | |  |  |
| Output | Open\_source | Series | Output\_diff |  |  | |  |  |
| 3-state | I/O\_open\_drain | Series\_switch | 3-state\_diff |  |  | |  |  |
| Open\_drain | I/O\_open\_sink |  | I/O\_diff |  |  | |  |  |
| I/O | I/O\_open\_source |  |  |  |  | |  |  |
|  | Input\_ECL |  |  |  |  | |  |  |
|  | Output\_ECL |  |  |  |  | |  |  |
|  | I/O\_ECL |  |  |  |  | |  |  |
|  | Terminator |  |  |  |  | |  |  |
| **[Model Spec] SUBPARAMETERS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  | Vinh | Cref | Weak\_R |  | |  |  |
|  |  | Vinl | Rref | Weak\_I |  | |  |  |
|  |  | Vinh+ | Vref | Weak\_V |  | |  |  |
|  |  | Vinh- | Cref\_rising | D\_overshoot\_area\_h |  | |  |  |
|  |  | Vinl+ | Cref\_falling | D\_overshoot\_area\_l |  | |  |  |
|  |  | Vinl- | Rref\_rising | D\_overshoot\_ampl\_h |  | |  |  |
|  |  | S\_overshoot\_high | Rref\_falling | D\_overshoot\_ampl\_l |  | |  |  |
|  |  | S\_overshoot\_low | Vref\_rising |  |  | |  |  |
|  |  | D\_overshoot\_high | Vref\_falling |  |  | |  |  |
|  |  | D\_overshoot\_low | Vmeas\_rising |  |  | |  |  |
|  |  | D\_overshoot\_time | Vmeas\_falling |  |  | |  |  |
|  |  | Pulse\_high | Rref\_diff |  |  | |  |  |
|  |  | Pulse\_low | Cref\_diff |  |  | |  |  |
|  |  | Pulse\_time |  |  |  | |  |  |
|  |  | V\_meas |  |  |  | |  |  |
| **[Submodel] SUBPARAMETER** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  | Submodel\_type |  |  |  | |  |  |
| **Submodel\_type SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  | Dynamic\_clamp | Fall\_back |  |  | |  |  |
|  |  | Bus\_hold |  |  |  | |  |  |
| **[Submodel Spec] SUBPARAMETERS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  | V\_trigger\_r |  |  |  | |  |  |
|  |  | V\_trigger\_f |  |  |  | |  |  |
|  |  | Off\_delay |  |  |  | |  |  |
| **[C Comp Model] SUBPARAMETERS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | |  | C\_comp\_model\_mode |
|  |  |  |  |  |  | |  | Param |
|  |  |  |  |  |  | |  | File\_TS |
|  |  |  |  |  |  | |  | File\_IBIS-ISS |
|  |  |  |  |  |  | |  | Number\_of\_terminals (7.0) |
| **[Interconnect Model] SUBPARAMETERS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | | Param |  |
|  |  |  |  |  |  | | File\_TS |  |
|  |  |  |  |  |  | | File\_IBIS-ISS |  |
|  |  |  |  |  |  | | Unused\_port\_termination |  |
|  |  |  |  |  |  | | Number\_of\_terminals |  |
| **[Interconnect Model] Unused\_port\_termination SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | | Reference |  |
|  |  |  |  |  |  | | Open |  |
|  |  |  |  |  |  | | Resistance |  |
| **[C Comp Model] Terminal\_type COLUMN SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | |  | Buffer\_I/O (7.0) |
|  |  |  |  |  |  | |  | Buffer\_I |
|  |  |  |  |  |  | |  | Pullup\_ref (7.0) |
|  |  |  |  |  |  | |  | Pulldown\_ref (7.0) |
|  |  |  |  |  |  | |  | Power\_clamp\_ref (7.0) |
|  |  |  |  |  |  | |  | Gnd\_clamp\_ref (7.0) |
|  |  |  |  |  |  | |  | Ext\_ref (7.0) |
|  |  |  |  |  |  | |  | A\_gnd (7.0) |
| **[interconnect Model] Terminal\_type COLUMN SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | | Pin\_I//O |  |
|  |  |  |  |  |  | | Pad\_I/O |  |
|  |  |  |  |  |  | | Buffer\_I/O |  |
|  |  |  |  |  |  | | Pin\_Rail |  |
|  |  |  |  |  |  | | Pad\_Rail |  |
|  |  |  |  |  |  | | Buffer\_Rail |  |
|  |  |  |  |  |  | | Pullup\_ref |  |
|  |  |  |  |  |  | | Pulldown\_ref |  |
|  |  |  |  |  |  | | Power\_clamp\_ref |  |
|  |  |  |  |  |  | | Gnd\_clamp\_ref |  |
|  |  |  |  |  |  | | Ext\_ref |  |
|  |  |  |  |  |  | | A\_gnd |  |
| **[EMD Model] Terminal\_type COLUMN SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | |  | Pin\_I/O (7.0) |
|  |  |  |  |  |  | |  | Pin\_Rail (7.0) |
|  |  |  |  |  |  | |  | A\_gnd (7.0) |
| **[Interconnect Model] Terminal\_type\_qualifiers COLUMN SELECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | | pin\_name |  |
|  |  |  |  |  |  | | signal\_name |  |
|  |  |  |  |  |  | | bus\_label |  |
|  |  |  |  |  |  | | pad\_name |  |
| **[EMD Model] Terminal\_type\_qualifiers COLUMN SELECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | |  | pin\_name (7.0) |
|  |  |  |  |  |  | |  | signal\_name (7.0) |
|  |  |  |  |  |  | |  | bus\_label (7.0) |
| **[Interconnect Model] Aggressor\_Only COLUMN SELECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | | Aggressor\_Only |  |
| **[EMD Model] Aggressor\_Only COLUMN SELECTION** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  |  |  | |  | Aggressor\_Only (7.0) |
| **Test\_data\_type and Test\_load\_type SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  | Single\_ended |  |  | |  |  |
|  |  |  | Differential |  |  | |  |  |
| **[Begin EMI Component] KEYWORDS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  | [Pin EMI] |  | |  |  |
|  |  |  |  | [Pin Domain EMI] |  | |  |  |
| **Model\_emi\_type SELECTIONS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
|  |  |  |  | Ferrite |  | |  |  |
|  |  |  |  | Not\_a\_Ferrite |  | |  |  |
| **(SUBPARAMETERS) FOR OTHER KEYWORDS** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | | Version 6.0/6.1\* | Version 7.0 | Version 7.1 |
| [Component] |  | [Component]  (Si\_location,  Timing\_location) |  | [Begin EMI Component]  (Domain, Cpd, C\_Heatsink\_gnd, C\_Heatsink\_float) | | [Repeater Pin] (tx\_non\_inv\_pin)  [Intial Delay] (V-T, I-T)\* |  | [Clocked Pins] (clocked\_pins, relationship) |
| [Package]  (R\_pkg, L\_pkg, C\_pkg) |  |  |  | [Pin EMI] (domain\_name, clock\_div) | |  |  | [PDN Domain] (Bus\_label, Signal\_name) |
| [Pin]  (signal\_name,  model\_name, R\_pin, L\_pin, C\_pin) |  |  |  | [Pin Domain EMI} (percentage) | |  |  | [PDN Model] (R\_pdn, C\_pdn, R\_leak) |
|  | [Pin Mapping]  (pulldown\_ref,  pullup\_ref,  gnd\_clamp\_ref,  power\_clamp\_ref) |  | [Pin Mapping]  (ext\_ref) | [Begin EMI Model] (Model\_emi\_type, Model\_Domain) | |  | [Bus Label] (signal\_pin) |  |
|  |  |  |  |  | |  | [Die Supply Pads] (signal\_pin, bus\_label) |  |
|  | [Diff Pin]  (inv\_pin, vdiff, t\_delay, tdelay\_min,  tdelay\_max) |  |  | [Algorithmic Model] (Executable) | | [Algorithmic Model] (Executable\_Rx\*, Executable\_Tx\*) |  |  |
|  |  | [Series Pin Mapping]  (pin\_2, model\_name,  function\_table\_group) |  | [C Comp Corner] (C\_comp, C\_comp\_pullup, C\_comp\_pulldown, C\_comp\_power\_clamp, C\_comp\_gnd\_clamp | |  |  |  |
|  |  | [Series Switch  Groups]  (On, Off) |  |  | |  |  |  |
|  |  |  | [Circuit Call]  (Signal\_pin,  Diff\_signal\_pins,  Series\_pins, Port\_map) |  | |  | [Circuit Call] (Parameters) (4.2), (Converter\_Parameters) (6.0) |  |
|  |  |  | [Receiver Thresholds]  (Vth, Vth\_min, Vth\_max, Vinh\_ac,Vinh\_dc, Vinl\_ac, Vinl\_dc,  Threshold\_sensitivity,  Reference\_supply, Vcross\_low, V\_cross\_high,  Vdiff\_ac, Vdiff\_dc,  Tslew\_ac, Tdiffslew\_ac) |  | |  |  |  |
|  |  | [Series MOSFET]  (Vds) |  |  | |  |  |  |
| [Ramp]  (dV/dt\_r, dV/dt\_f) | [Ramp]  (R\_load) |  |  |  | |  |  |  |
|  | [Rising Waveform]  (R\_fixture, V\_fixture,  V\_fixture\_min,  V\_fixture\_max,  C\_fixture, L\_fixture,  R\_dut, L\_dut, C\_dut) |  |  |  | |  |  |  |
|  | [Falling Waveform]  (R\_fixture, V\_fixture,  V\_fixture\_min,  V\_fixture\_max,  C\_fixture, L\_fixture,  R\_dut, L\_dut, C\_dut) |  |  |  | |  |  |  |
|  |  |  | [Test Data]  (Test\_data\_type, Driver\_model,  Driver\_model\_inv, Test\_load)  (moved to top-level in 5.1) |  | |  |  |  |
|  |  |  | [Test Load]  (Test\_load\_type, C1\_near, Rs\_near, Ls\_near, C2\_near,  Rpl\_near, Rp2\_near, Td, Zo, Rpl\_far, Rp2\_far, C1\_far, Ls\_far, Rs\_far, V\_term1, V\_term2, Receiver\_model,  Receiver\_model\_inv,  R\_diff\_near, R\_diff\_far)  (moved to top-level in 5.1) |  | |  |  |  |
|  |  |  | [External Model]  (Language, Corner, Parameters, Ports, D\_to\_A, A\_to\_D) |  | | [External Model] (Converter\_Parameters) |  |  |
|  |  |  | [External Circuit]  (Language, Corner, Parameters, Ports, D\_to\_A, A\_to\_D) |  | | [External Circuit] (Converter\_Parameters) |  |  |
|  | [Pin Numbers] | [Pin Numbers]  (Len, L, C, R, Fork,  Endfork) |  |  | |  |  |  |
|  |  | [Pin List]  (signal\_name) |  |  | |  |  |  |
|  |  | [Begin Board  Description]  (Len, L, C, R, Fork,  Endfork, Node, Pin) |  |  | |  |  |  |
| **OTHER NOTABLE CHANGES** | | | | | | | | |
| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0/6.1\* | | Version 7.0 | Version 7.1 |
| File width = 80 |  |  | File width = 120 |  |  | | File width = 1024 |  |
| Filename length = 8 |  | Filename length = 20 | Filename length = 40 |  |  | | Filename length = 60, filename case-insensitive |  |
|  |  |  |  |  |  | | File\_reference linkage includes subdirectories |  |
| Model name  length = 20 |  |  | Model name length = 40 |  |  | |  |  |
|  |  | Submodel name  length = 20 | Submodel name length = 40 |  |  | |  |  |
|  | [Rising Waveform],  [Falling Waveform]  rows = 100 |  | [Rising Waveform],  [Falling Waveform]  rows = 1000 |  |  | |  |  |
| Vinh, Vinl optional  for Input and I/O | Vinh, Vinl required for Input and I/O |  |  |  |  | |  |  |
| Reserved words NC  POWER, GND, NA |  |  | Added reserved word  CIRCUITCALL |  |  | |  |  |
| Fixed keyword space and underbar convention | Space and underbar  equivalent in  keywords |  |  |  |  | |  |  |
| Original comment characters | +, - removed as comment characters |  |  |  |  | |  |  |
| Multipliers M, k, m, u, n, p | Multipliers T, G and f added |  |  |  |  | |  |  |
| Buffers by extraction |  | By construction added | By language linkage added | EMI, SSO, and Algorithmic Modeling Interface added, [Test Load] and [Test Data] hierarchy changed | PAM4 mapping and other IBIS-AMI parameters | | Interconnect Modeling, linkage to IBIS-ISS, and Touchstone; Files references with paths; Backchannel (BCI);, more IBIS-AMI parameters, linkage to 4-port Touchstone | Electrical Module Description and EMD Set files added, [Clocked Pins], [C Comp Model], [PDN Domain] added |