

IBIS EVOLUTION
(IBIS, PACKAGE, ELECTRICAL BOARD DESCRIPTION, EMI, SSO, ALGORITHMIC MODELING INTERFACE)
Bob Ross, July 25, 2006, updated September 14, 2007, September 8, 2013, April 20, 2014, July 31, 2015, July 21, 2016, July, 19, 2018, March 15, 2019

HEADER SECTION (.ibs, .pkg, .ebd, .ims)

Version 1.1	Version 2.1 (.ibs, .pkg)	Version 3.2 (.ebd)	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0 (.ims)
[IBIS Ver]	[Copyright]					
[Comment Char] (re-defined anywhere in file)						
[File Name]						
[File Rev]						
[Date]						
[Source]						
[Notes]						
[Disclaimer]						

TOP-LEVEL KEYWORDS (with END Keywords)

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
[Component]	[Define Package Model] (.ibs, .pkg)	[Model Selector]	[External Circuit]	[Test Load] (defined under [Model] in 4.2)		[Interconnect Model Set] (.ims)
[Model]	[End Package Model] (.ibs, .pkg)	[Submodel]	[End External Circuit]	[Test Data] (defined under [Test Load] in 4.2)		[End Interconnect Model Set] (.ims)
[End]	[End] (.pkg)	[Begin Board Description] (.ebd)				[End] (.ims)
		[End Board Description] (.ebd)				
		[End] (.ebd)				

[Component] PINOUT AND PACKAGE SECTION

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
[Component]	[Pin Mapping]	[Series Pin Mapping]	[Alternate Package Models]	[Begin EMI Component]	[Repeater Pin]	[Interconnect Model Group]
[Manufacturer]	[Diff Pin]	[Series Switch Groups]	[End Alternate Package Models]	[End EMI Component]		[Bus Label]
[Package]	[Package Model]		[Node Declarations]			[Die Supply Pads]
[Pin]			[End Node Declarations]			
			[Circuit Call]			
			[End Circuit Call]			

[Model] SECTION

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
[Model]	[Temperature Range]	[Model Spec]	[Receiver Thresholds]	[Begin EMI Model]	[Initial Delay]*	
[Voltage Range]	[Pullup Reference]	[Driver Schedule]	[External Reference]	[End EMI Model]		

[Pulldown]	[Pulldown Reference]	[TTgnd]	[Test Data]	[Algorithmic Model]		
[Pullup]	[POWER Clamp Reference]	[TTpower]	[Rising Waveform Near]	[End Algorithmic Model]		
[GND Clamp]	[GND Clamp Reference]	[On]	[Falling Waveform Near]	[ISSO PU]		
[POWER Clamp]	[Rgnd]	[Off]	[Rising Waveform Far]	[ISSO PD]		
[Ramp]	[Rpower]	[R Series]	[Falling Waveform Far]	[Composite Current] (under [Rising Waveform])		
	[Rac]	[L Series]	[Diff Rising Waveform Near]	[Composite Current] (under Falling Waveform)		
	[Cac]	[RI Series]	[Diff Falling Waveform Near]	[C Comp Corner]		
	[Rising Waveform]	[C Series]	[Diff Rising Waveform Far]			
	[Falling Waveform]	[Lc Series]	[Diff Falling Waveform Far]			
		[Rc Series]	[Test Load]			
		[Series Current]	[External Model]			
		[Series MOSFET]	[End External Model]			
		[Add Submodel]				
[Submodel] SECTION						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
		[Submodel]			[Initial Delay]*	
		[Pullup] (1.1)				
		[Pulldown] (1.1)				
		[GND Clamp] (1.1)				
		[POWER Clamp] (1.1)				
		[Ramp] (1.1)				
		[Rising Waveform] (2.1)				
		[Falling Waveform] (2.1)				
		[Submodel Spec]				
		[GND Pulse Table]				
		[POWER Pulse Table]				
PACKAGE MODEL DEFINITION (within .ibs or as .pkg)						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
	[Define Package Model]	[Number Of Sections]			[Merged Pins]*	
	[Manufacturer] (1.1)					
	[OEM]					
	[Description]					
	[Number Of Pins]					
	[Pin Numbers]					
	[Model Data]					
	[End Model Data]					
	[Resistance Matrix]					

	[Inductance Matrix]					
	[Capacitance Matrix]					
	[Row]					
	[Bandwidth]					
	[End Package Model]					
ELECTRICAL BOARD DESCRIPTION (.ebd)						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
		[Begin Board Description]				
		[Manufacturer] (1.1)				
		[Number Of Pins] (1.1)				
		[Pin List]				
		[Path Description]				
		[Reference Designator Map]				
		[End Board Description]				
INTERCONNECT MODEL SET (within .ibs or .ims)						
						[Interconnect Model Set]
						[Manufacturer] (1.1)
						[Description] (2.1)
						[Interconnect Model]
						[End Interconnect Model]
						[End Interconnect Set]
[Model] SUBPARAMETERS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
Polarity	Cref		C_comp_pullup			
Enable	Ref		C_comp_pulldown			
Model_type	Vref		C_comp_power_clamp			
C_comp	Vmeas		C_comp_gnd_clamp			
Vinh			Rref_diff			
Vinl			Cref_diff			
Model_type SELECTIONS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
Input	Open_sink	3-state_ECL	Input_diff			
Output	Open_source	Series	Output_diff			
3-state	I/O_open_drain	Series_switch	3-state_diff			
Open_drain	I/O_open_sink		I/O_diff			
I/O	I/O_open_source					
	Input_ECL					
	Output_ECL					
	I/O_ECL					
	Terminator					
[Model Spec] SUBPARAMETERS						

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
		Vinh	Cref	Weak_R		
		Vinl	Rref	Weak_I		
		Vinh+	Vref	Weak_V		
		Vinh-	Cref_rising	D_overshoot_area_h		
		Vinl+	Cref_falling	D_overshoot_area_l		
		Vinl-	Rref_rising	D_overshoot_ampl_h		
		S_overshoot_high	Rref_falling	D_overshoot_ampl_l		
		S_overshoot_low	Vref_rising			
		D_overshoot_high	Vref_falling			
		D_overshoot_low	Vmeas_rising			
		D_overshoot_time	Vmeas_falling			
		Pulse_high	Rref_diff			
		Pulse_low	Cref_diff			
		Pulse_time				
		V_meas				
[Submodel] SUBPARAMETER						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
		Submodel_type				
Submodel_type SELECTIONS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
		Dynamic_clamp	Fall_back			
		Bus_hold				
[Submodel Spec] SUBPARAMETERS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
		V_trigger_r				
		V_trigger_f				
		Off_delay				
[Interconnect Model] SUBPARAMETERS						
						Param
						File_TS
						File_IBIS-ISS
						Unused_port_termination
						Number_of_terminals
[Interconnect Model] Unused_port_termination SELECTIONS						
						Reference
						Open
						Resistance
[interconnect Model] Terminal_type COLUMN SELECTIONS						
						Pin_I/O
						Pad_I/O
						Buffer_I/O

						Pin_Rail
						Pad_Rail
						Buffer_Rail
						Pullup_ref
						Pulldown_ref
						Power_clamp_ref
						Gnd_clamp_ref
						Ext_ref
						A_gnd
[Interconnect Model] Terminal_type_qualifiers COLUMN SELECTION						
						pin_name
						signal_name
						bus_label
						pad_name
[Interconnect Model] Aggressor_Only COLUMN SELECTION						
						Aggressor_Only
Test_data_type and Test_load_type SELECTIONS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
			Single_ended			
			Differential			
[Begin EMI Component] KEYWORDS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
				[Pin EMI]		
				[Pin Domain EMI]		
Model_emi_type SELECTIONS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
				Ferrite		
				Not_a_Ferrite		
(SUBPARAMETERS) FOR OTHER KEYWORDS						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
[Component]		[Component] (Si_location, Timing_location)		[Begin EMI Component] (Domain, Cpd, C_Heatsink_gnd, C_Heatsink_float)	[Repeater Pin] (tx_non_inv_pin) [Initial Delay] (V-T, I-T)*	
[Package] (R_pkg, L_pkg, C_pkg)				[Pin EMI] (domain_name, clock_div)		
[Pin] (signal_name, model_name, R_pin, L_pin, C_pin)				[Pin Domain EMI] (percentage)		
	[Pin Mapping]		[Pin Mapping]	[Begin EMI Model]		[Bus Label] (signal_pin)

	(pulldown_ref, pullup_ref, gnd_clamp_ref, power_clamp_ref)		(ext_ref)	(Model_emi_type, Model_Domain)		
						[Die Supply Pads] (signal_pin, bus_label)
	[Diff Pin] (inv_pin, vdiff, t_delay, tdelay_min, tdelay_max)			[Algorithmic Model] (Executable)	[Algorithmic Model] (Executable_Rx*, Executable_Tx*)	
		[Series Pin Mapping] (pin_2, model_name, function_table_group)		[C Comp Corner] (C_comp, C_comp_pullup, C_comp_pulldown, C_comp_power_clamp, C_comp_gnd_clamp)		
		[Series Switch Groups] (On, Off)				
			[Circuit Call] (Signal_pin, Diff_signal_pins, Series_pins, Port_map)			[Circuit Call] (Parameters) (4.2), (Converter_Parameters) (6.0)
			[Receiver Thresholds] (Vth, Vth_min, Vth_max, Vinh_ac,Vinh_dc, Vinl_ac, Vinl_dc, Threshold_sensitivity, Reference_supply, Vcross_low, V_cross_high, Vdiff_ac, Vdiff_dc, Tslew_ac, Tdiffslew_ac)			
		[Series MOSFET] (Vds)				
[Ramp] (dV/dt_r, dV/dt_f)	[Ramp] (R_load)					
	[Rising Waveform] (R_fixture, V_fixture, V_fixture_min, V_fixture_max, C_fixture, L_fixture, R_dut, L_dut, C_dut)					
	[Falling Waveform] (R_fixture, V_fixture, V_fixture_min, V_fixture_max, C_fixture, L_fixture, R_dut, L_dut, C_dut)					
			[Test Data] (Test_data_type, Driver_model, Driver_model_inv, Test_load) (moved to top-level in			

			5.1)			
			[Test Load] (Test_load_type, C1_near, Rs_near, Ls_near, C2_near, Rp1_near, Rp2_near, Td, Zo, Rp1_far, Rp2_far, C1_far, Ls_far, Rs_far, V_term1, V_term2, Receiver_model, Receiver_model_inv, R_diff_near, R_diff_far) (moved to top-level in 5.1)			
			[External Model] (Language, Corner, Parameters, Ports, D_to_A, A_to_D)		[External Model] (Converter_Parameters)	
			[External Circuit] (Language, Corner, Parameters, Ports, D_to_A, A_to_D)		[External Circuit] (Converter_Parameters)	
	[Pin Numbers]	[Pin Numbers] (Len, L, C, R, Fork, Endfork)				
		[Pin List] (signal_name)				
		[Begin Board Description] (Len, L, C, R, Fork, Endfork, Node, Pin)				
OTHER NOTABLE CHANGES						
Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0/6.1*	Version 7.0
File width = 80			File width = 120			File width = 1024
Filename length = 8		Filename length = 20	Filename length = 40			Filename length = 60, filename case-insensitive
						File_reference linkage includes subdirectories
Model name length = 20			Model name length = 40			
		Submodel name length = 20	Submodel name length = 40			
	[Rising Waveform], [Falling Waveform] rows = 100		[Rising Waveform], [Falling Waveform] rows = 1000			
Vinh, Vinl optional for Input and I/O	Vinh, Vinl required for Input and I/O					
Reserved words NC POWER, GND, NA			Added reserved word CIRCUITCALL			
Fixed keyword space and underbar	Space and underbar equivalent in					

convention	keywords					
Original comment characters	+, - removed as comment characters					
Multipliers M, k, m, u, n, p	Multipliers T, G and f added					
Buffers by extraction		By construction added	By language linkage added	EMI, SSO, and Algorithmic Modeling Interface added, [Test Load] and [Test Data] hierarchy changed	PAM4 mapping and other IBIS-AMI parameters	Interconnect Modeling, linkage to IBIS-ISS, and Touchstone; Files references with paths; Backchannel (BCI);, more IBIS-AMI parameters, linkage to 4-port Touchstone