Addressing DDR5 design challenges with IBIS-AMI modeling techniques

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EDI CON 2017 IBIS Summit
Boston, Massachusetts
September 13, 2017

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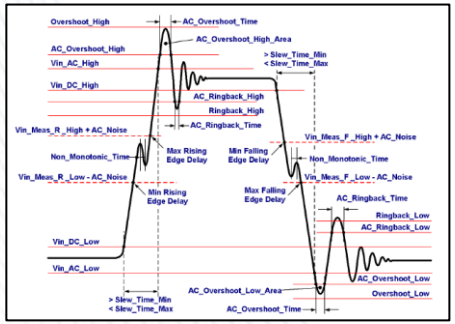
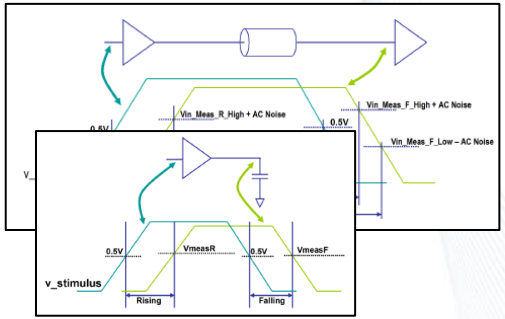
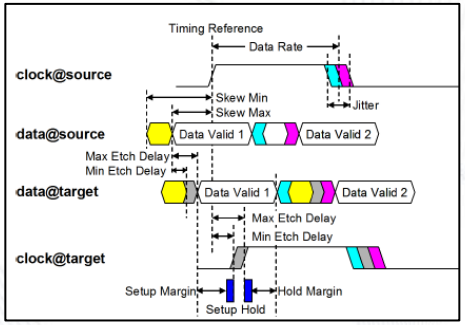
Agenda

- Traditional DDR analysis
- Eyes and probabilities
- IBIS-AMI models
- DDR5 topologies and transactions
- Optimizing terminations
- Pulse response analysis
- Applying equalization
- Summary

Traditional DDR Analysis







Signal Integrity + Flight Time Extraction + Timing Analysis

- Combined signal integrity + timing analysis
  ➔ voltage and timing margins
- SI analysis < 100 data bits
- Margins computed based on worst case data

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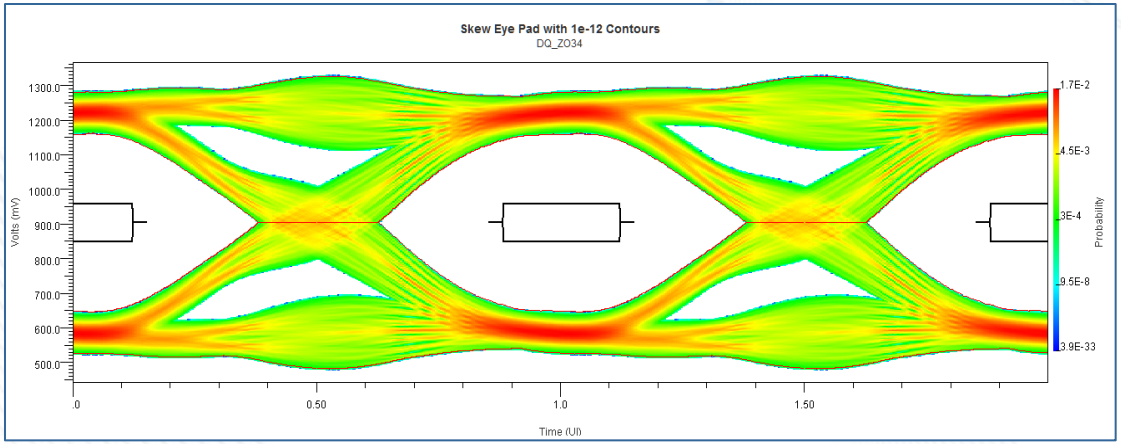
Eyes and Probabilities



- SerDes analysis techniques used to predict eye characteristics > 1M bits
- Eye margins measured against reference mask
  - Timing / skew adjustments are assumed

IBIS-AMI Models

Goals

- **Interoperable:** different vendor models work together
- **Portable:** one model runs in multiple simulators
- **Flexible:** supports Statistical and Time-Domain simulation
- **High Performance:** simulates a million bits per CPU minute
- **Accurate:** high correlation to simulations / measurement

Assumptions

- “High impedance node” between analog I/O & equalization circuitry
- Analog I/O operates in linear region
- EQ behavior modeled by code linked into simulator
- EQ models meet AMI API

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Serial Channels vs. DDR Topologies

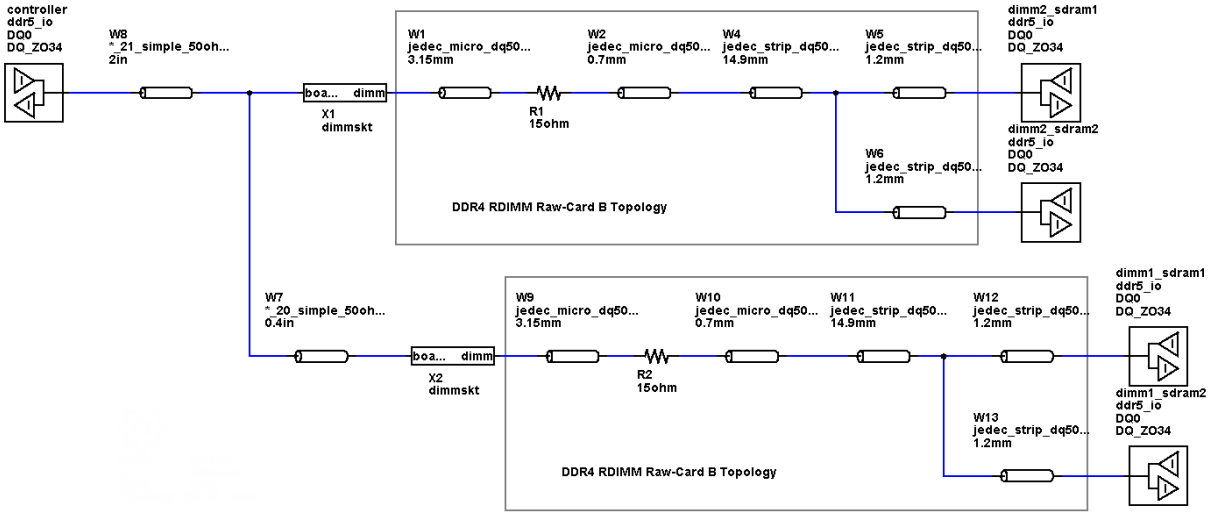
Serial Channels

- Differential
- Long and lossy
- Unidirectional
- Continuous operation
- Simple impedance control
- Point to point topology

DDR Topologies

- Single-ended & differential
- Short and reflective
- Bidirectional
- Communicate in bursts
- Complex impedance control
- Multiple sources / loads with long branches

DDR5 Topologies and Transactions



1. (Write) Controller to DIMM1
2. (Write) Controller to DIMM2
3. (Read) DIMM1 to Controller
4. (Read) DIMM2 to Controller

Optimizing Terminations

Driver settings:

- DQ_ZO34 Generic DDR5 34 Ohm Driver
- DQ_ZO40 Generic DDR5 40 Ohm Driver
- DQ_ZO48 Generic DDR5 48 Ohm Driver

Receiver / terminator settings:

- DQ_IN_ODTOFF Generic DDR5 Receiver with No ODT
- DQ_IN_ODT34 Generic DDR5 Receiver with 34 ohm ODT
- DQ_IN_ODT40 Generic DDR5 Receiver with 40 ohm ODT
- DQ_IN_ODT48 Generic DDR5 Receiver with 48 ohm ODT
- DQ_IN_ODT60 Generic DDR5 Receiver with 60 ohm ODT
- DQ_IN_ODT80 Generic DDR5 Receiver with 80 ohm ODT
- DQ_IN_ODT120 Generic DDR5 Receiver with 120 ohm ODT
- DQ_IN_ODT240 Generic DDR5 Receiver with 240 ohm ODT

Each transaction:

(Driver) * (Receiver) * (Terminator)**3

= 3 * 8 * 8**3

= 12,288 combinations per transaction

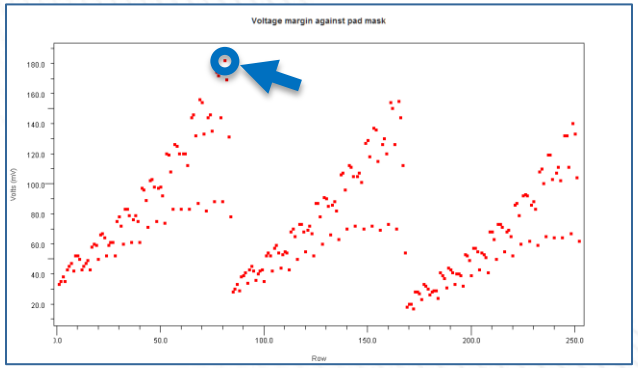
* 4 transactions

= 49,152 total termination settings (!)

Finding The Best Case

Variable:	Type:	Format:	Variation Group:	Value 1:	Value 2:	Value 3:	Value 4:	Value 5:	Value 6:	Value 7:
$controller:t1:model	IBIS Model	List	<none>	DQ_ZO34	DQ_ZO40	DQ_ZO48				
$dimm1_sdram1:t1:model	IBIS Model	List	<none>	DQ_IN_ODT34	DQ_IN_ODT40	DQ_IN_ODT48	DQ_IN_ODT60	DQ_IN_ODT80	DQ_IN_ODT120	DQ_IN_ODT240
$dimm1_sdram2:t1:model	IBIS Model	List	<none>	DQ_IN_ODT120	DQ_IN_ODT240	DQ_IN_ODTOFF				
$dimm2_sdram1:t1:model	IBIS Model	List	dimm2	DQ_IN_ODT60	DQ_IN_ODT80	DQ_IN_ODT120	DQ_IN_ODT240			
$dimm2_sdram2:t1:model	IBIS Model	List	dimm2	DQ_IN_ODT60	DQ_IN_ODT80	DQ_IN_ODT120	DQ_IN_ODT240			
$UI	UI	List	<none>	0.313ns - ddr5_dq_3200						

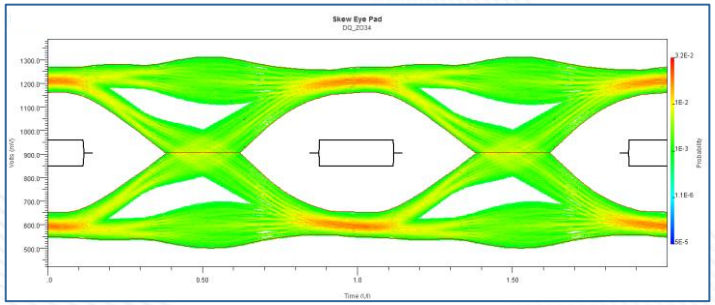
252 cases tested (out of a possible 12,288)



Voltage margin distribution

$CONTROLLER:T1:MODEL	DQ_ZO34
$DIMM1_SDRAM1:T1:MODEL	DQ_IN_ODT240
$DIMM1_SDRAM2:T1:MODEL	DQ_IN_ODTOFF
$DIMM2_SDRAM1:T1:MODEL	DQ_IN_ODT60
$DIMM2_SDRAM2:T1:MODEL	DQ_IN_ODT60

Best case conditions



Voltage and timing margin against mask

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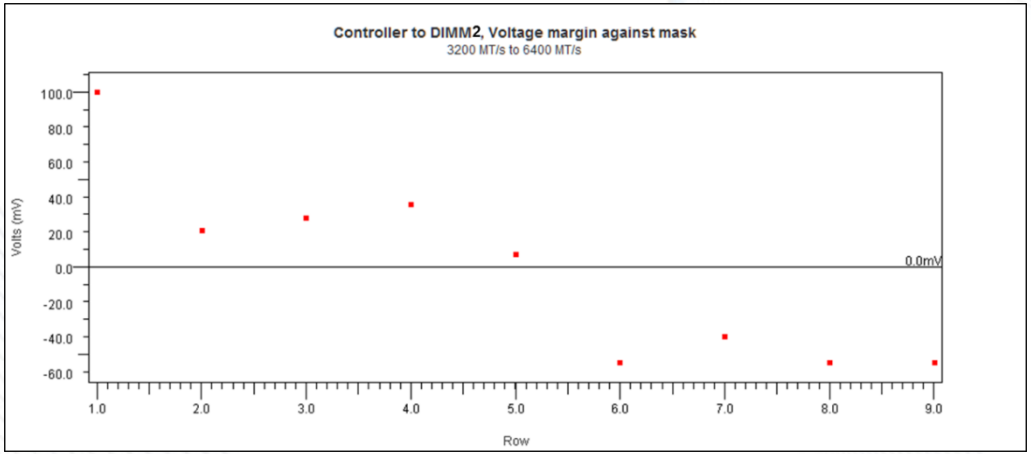
The Limiting Transaction

Transfer	Skew_Eye_Pad Inner (V)	Skew_Eye_Pad Inner (ps)
controller_to_dimm1_sdram1	0.179	69.736
dimm1_sdram1_to_controller	0.138	70.961
dimm2_sdram1_to_controller	0.102	57.485
controller_to_dimm2_sdram1	0.100	39.722

- Termination settings for each transaction were optimized
- Best voltage and timing margins determined for each transaction
- We'll focus on the worst case transaction for this study

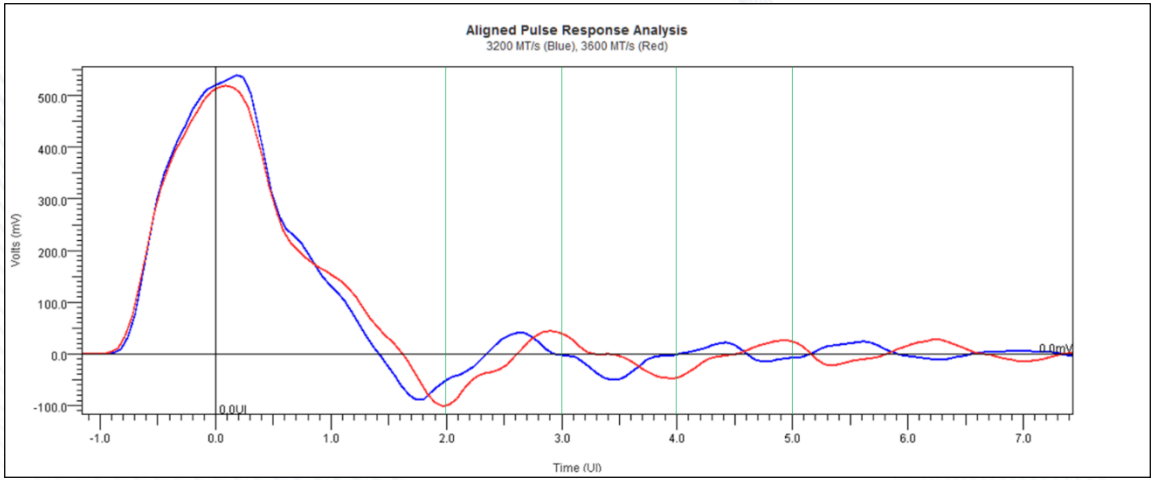
Limiting Transaction vs. Speed



- Data rate: 3200 to 6400MT/s, increments of 400 MT/s
- Voltage margin against mask is plotted
- Two questions
  - Why is 3600 MT/s so much worse than 3200 MT/s?
  - How can 4400 MT/s be better than 3600 MT/s?

Pulse Response Analysis

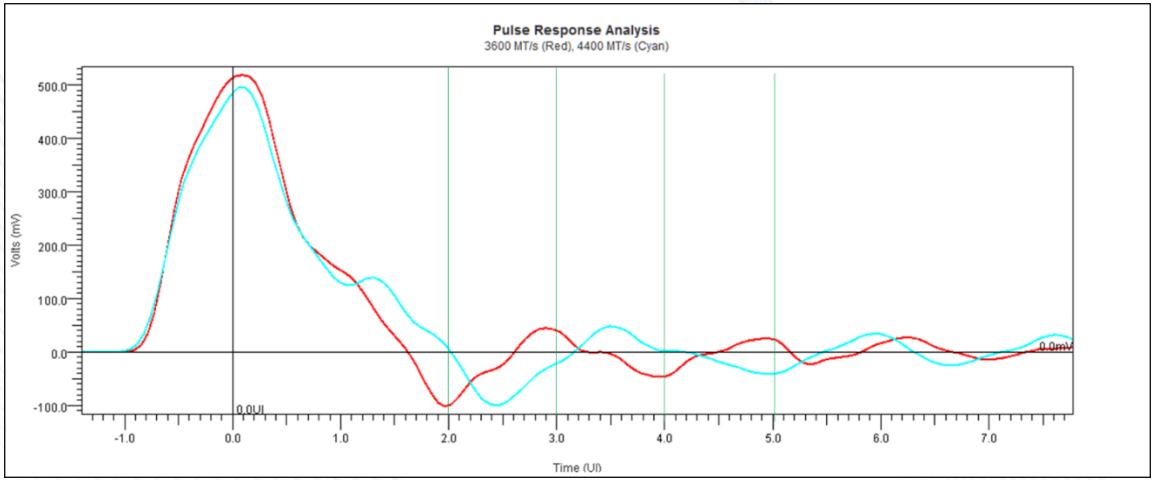
3200 MT/s (Blue) vs 3600 MT/s (Red)



- Vertical lines denote ISI at sampling times
- 3600 MT/s **maximizes** ISI at sample point

Pulse Response Analysis

4400 MT/s (Cyan) vs 3600 MT/s (Red)



- 4400 MT/s has less pulse height & width
- 4400 MT/s ISI is much better than 3600 MT/s

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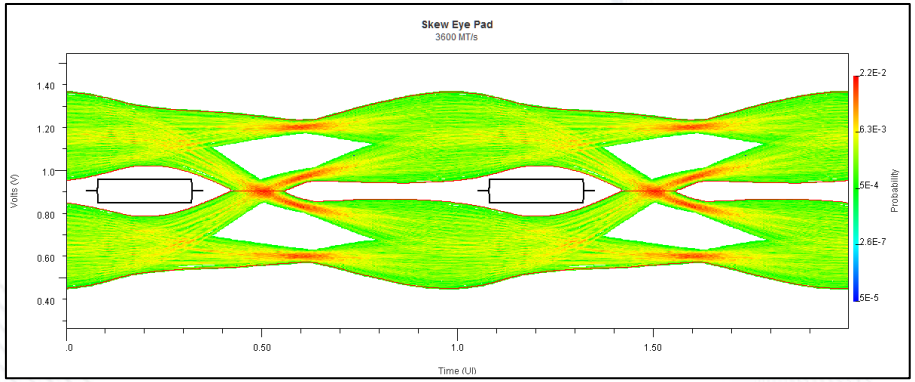
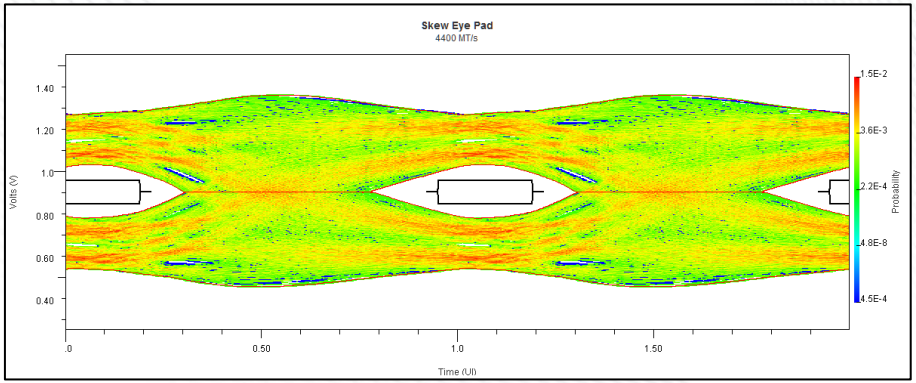
3600 MT/s vs. 4400 MT/s

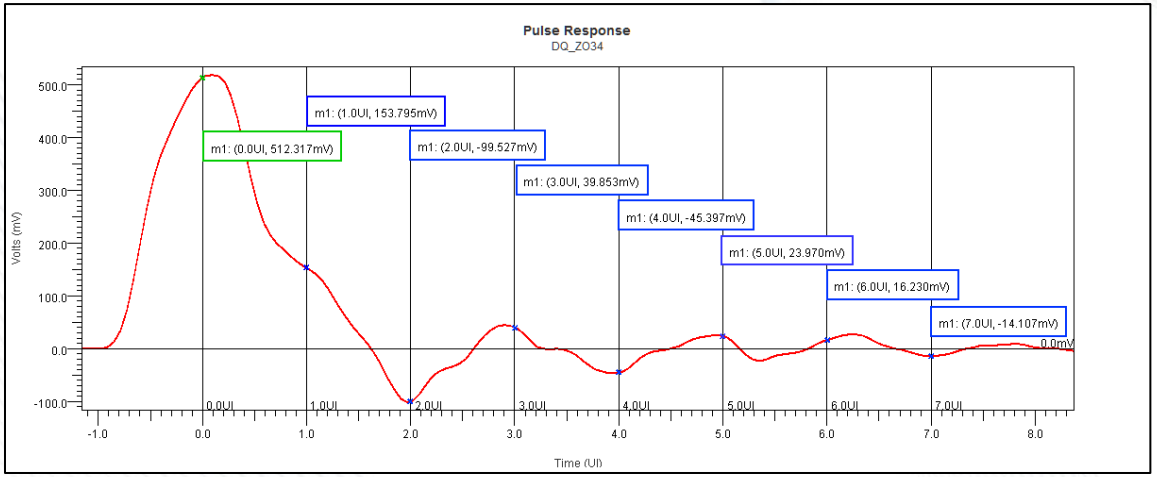


3600 MT/s



4400 MT/s

Applying Equalization



- Problem here isn't loss, it's **ringing**
- TX FIR and RX CTLE filters deal with loss
- RX DFE is best suited to correct ringing
- RX ISI voltages can be read directly off the plot

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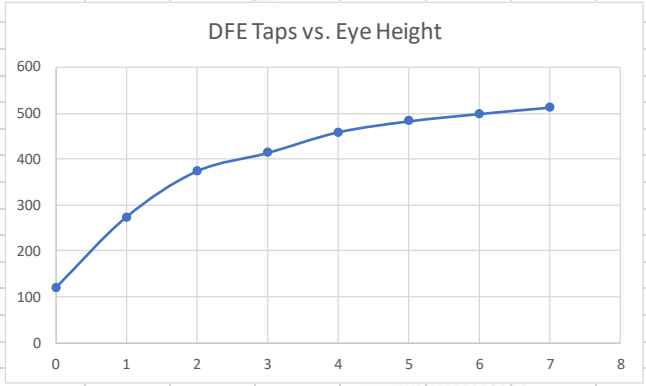
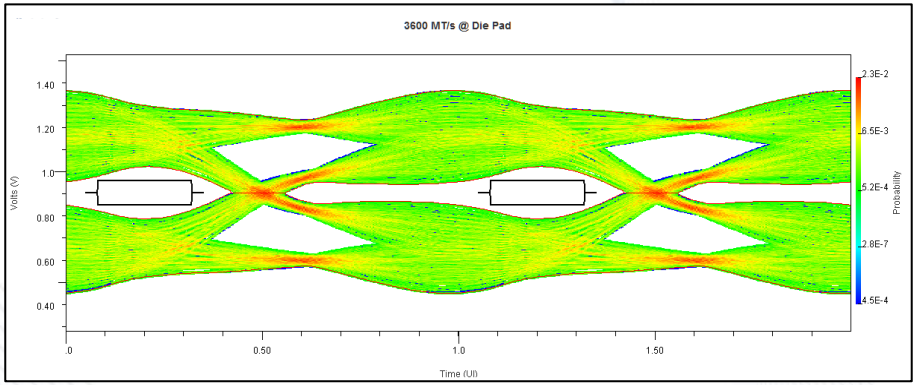
Eye Height vs. DFE Taps

			Eye Height	
	mV	DFE Taps	mV	% Improvement
		0	120	
ISI 1	154	1	274	128%
ISI 2	100	2	374	212%
ISI 3	40	3	414	245%
ISI 4	45	4	459	283%
ISI 5	24	5	483	303%
ISI 6	16	6	499	316%
ISI 7	14	7	513	328%

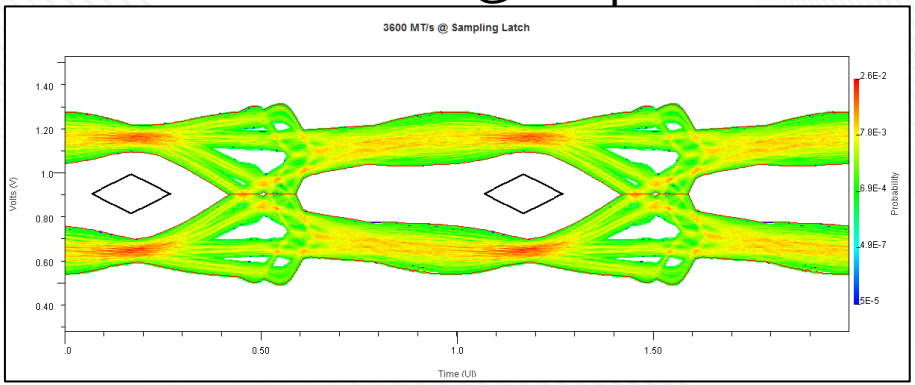


- We compute theoretical eye opening from the pulse response
- We also compute how DFE taps could improve eye height
  - Assumes tap range, granularity, training efficiency

Impact of 2 DFE Taps

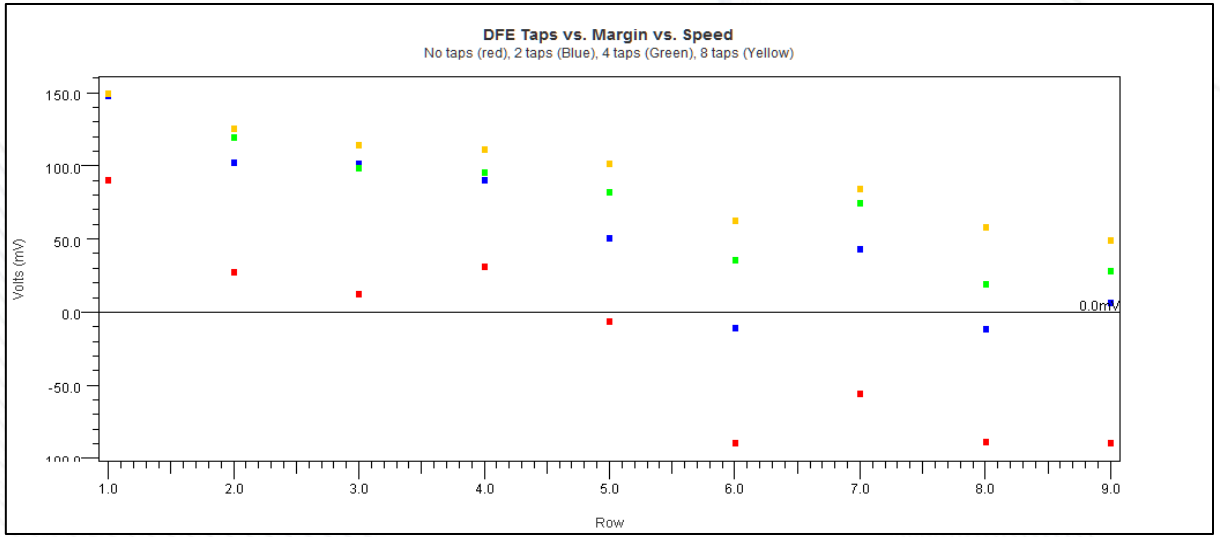


3600 MT/s @ die pad



3600 MT/s @ sampling latch

DFE Taps vs. Speed



- Data rate: 3200 to 6400MT/s, increments of 400 MT/s
- Voltage margin against mask is plotted
- DFE taps: 0 (Red), 2 (Blue), 4 (Green), 8 (Yellow)

Summary

- Modern DDR analysis uses techniques that predict behavior over millions of data bits
- Optimizing driver / receiver termination settings is essential to ensuring margin
- Pulse response analysis provides useful insight into how ringing affects DDR design margins
- AMI models can be used to predict how Tx/Rx EQ will improve design margins
- This presentation only covered **part** of the full methodology needed for DDR5 analysis

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