IBIS Open Forum Minutes

Meeting Date: **September 13, 2017**
Meeting Location: **EDI CON 2017 IBIS Summit, Boston, Massachusetts, USA**

VOTING MEMBERS AND 2017 PARTICIPANTS

ANSYS	Curtis Clark*, Toru Watanabe
Applied Simulation Technology	(Fred Balistreri)
Broadcom	[Bob Miller], (Cathy Liu)
Cadence Design Systems	Brad Brim, Sivaram Chillarige, Debabrata Das Ambrish Varma*, Kumar Keshavan*, Ken Willis* Brad Griffin*
Cisco Systems	(Bidyut Sen)
CST	Stefan Paret, Matthias Troescher, Burkhard Doliwa Danilo Di Febo, Alexander Melkozerov
Ericsson	Zilwan Mahmod
GLOBALFOUNDRIES	Steve Parker
Huawei Technologies	(Jinjun Li)
IBM	Luis Armenta, Adge Hawes, Greg Edlund
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Hsinho Wu, Eddie Frie Gianni Signorini, Barry Grquinovic
IO Methodology	Lance Wang*
Keysight Technologies	Radek Biernacki, Pegah Alavi, Fangyi Rao Stephen Slater, Jian Yang
Maxim Integrated	Joe Engert, Don Greer, Yan Liang, Hock Seow
Mentor, A Siemens Business (formerly Mentor Graphics)	Arpad Muranyi, Nitin Bhagwath, Praveen Anmula Fadi Deek, Raj Raghuram, Dmitry Smirnov Bruce Yuan, Carlo Bleu
Micron Technology	Randy Wolff, Justin Butterfield, Jeff Shiba*, Harry Shin*
NXP	(John Burnett)
Qualcomm	Tim Michalka, Kevin Roselle
Raytheon	Joseph Aday
SiSoft	Mike LaBonte*, Walter Katz, Todd Westerhoff* Steve Silva*
Synopsys	Kevin Li, Ted Mido, John Ellis, Scott Wedge
Teraspeed Labs	Bob Ross
Xilinx	(Raymond Anderson)
Zuken	Ralf Bruening, Michael Schaeder, Alfonso Gambuzza

OTHER PARTICIPANTS IN 2017

Accton	Raul Lozano
ASUS	Nick Huang, Bin-chyi Tseng
Continental AG	Stefanie Schatt
eASIC	David Banas
Extreme Networks	Bob Haller
Ghent University	Paolo Manfredi
Hamburg University of Technology	Torsten Revschel, Torsen Wendt
IdemWorks	Michelangelo Bandinu
Independent	Dian Yang, Lawrence Der*
John Baprawski, Inc.	John Baprawski
KEI Systems	Shinichi Maeda
Lattice Semiconductor	Maryam Shahbazi, Dinh Tran
Leading Edge	Pietro Vergine
Lexington Consulting	Mike Barg*
Politecnico di Torino	Claudio Siviero, Stefano Grivet-Talocia, Igor Stievano
SAE International	(Thomas Munns)
Signal Metrics	Ron Olisar
SPISim	Wei-hsing Huang
STMicroelectronics	Fabio Brina, Olivier Bayet
Toshiba	Yasuki Torigoshi
Université Blaise Pascal	Mohamed Toure
Université de Bretagne Occidentale	Mihai Telescu
ZTE Corporation	(Shunlin Zhu)

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
September 15, 2017	624 999 876	IBISfriday11

For teleconference dial-in information, use the password at the following website:

http://tinyurl.com/zeulerr

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Boston, Massachusetts at the Hynes Convention Center, during the EDI CON 2017 conference. About 13 people representing 7 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/sep17/

Mike LaBonte welcomed everyone to the Summit, opening the meeting at 1:00 p.m. He noted that this was the first ever EDI CON IBIS Summit. He thanked the sponsors EDI CON, SiSoft and Teraspeed Labs.

IBIS UPDATE

Mike LaBonte (SiSoft)

Mike LaBonte showed the 25 current members of IBIS, the IBIS officers, and he detailed the many IBIS Open Forum and task group meetings and Summits. The parent organization of the IBIS Open Forum is the SAE Industry Technologies Consortia. IBIS version 7.0 is under development, and it has been just over two years since version 6.1 was ratified. He discussed a possible timeline for release of IBIS version 7.0 and a list of BIRDs to be included and excluded. He gave an overview of some prominent BIRDs targeted for inclusion in IBIS version 7.0 including BIRD147 for backchannel support, BIRD158 for AMI Touchstone analog buffer model support, BIRD188 for expanded Rx noise support for AMI, and BIRD189 for interconnect modeling using IBIS-ISS and Touchstone.

LEVERAGING IBIS CAPABILITIES FOR MULTI-GIGABIT INTERFACES

Ken Willis (Cadence Design Systems)

Ken Willis noted that the presentation related to the EDI CON paper “Signal Integrity Methodology for Double-Digit Multi-Gigabit Interfaces”. Use of Spice [External Model]s makes it easy to write simple parameterized Spice subcircuits for I/O buffers when IBIS availability does not align with a project schedule. The EDA tool user can select parameter values from a GUI using the [External Model] “Parameters” and “Converter_Parameters” syntax. Ken asked if the IBIS committee might add a simple example to the IBIS Cookbook to help aid in adoption of [External Model].

Ken described the typical modules of an Rx AMI model including gain, CTLE and DFE. These modules typically adapt at different rates, and the initial modules like gain and CTLE usually adapt more slowly than the DFE. He showed how adjusting the adaptation algorithms of the AMI model led to better adaptation and a significant difference in final eye height. Ken showed details of the backchannel flow from BIRD147. He went on to show the application of IBIS-AMI modeling and simulation techniques to DDR4/5. Cadence developed an IBIS-AMI model for a DDR4 controller that included equalization. He showed correlation between an IBIS-AMI model-based channel simulation and a transistor-level circuit simulation.

Todd Westerhoff asked how Ken meant to "standardize on the format of display" for AMI parameters. Ken said we might standardize names. Kumar Keshavan said we might define a fixed file name for the model to write to. Todd noted that they could be passed out via AMI_parameters_out. All agreed we would need some standardization on names, units, etc. for certain parameters if we wanted all tools to present output parameters similarly.

Regarding backchannel modeling, Todd asked if the Tx sends the necessary test pattern or if the tool has to do it. Kumar noted that the original backchannel proposal included the test pattern as part of the BCI. But with the latest version, if there is a required test pattern then the tool has to provide (send) it. Kumar noted that most protocols now work with any PRBS type pattern instead of specific training patterns. Todd asked if the Tx is typically the slowest to converge. Kumar said it was.

ADDRESSING DDR5 DESIGN CHALLENGES WITH IBIS-AMI MODELING TECHNIQUES
Todd Westerhoff, Doug Burns, Eric Brock (SiSoft)

Todd Westerhoff noted that traditional DDR memory system analysis combines SI with timing analysis to calculate voltage and timing margins, typically analyzing less than 100 bits. In contrast, SerDes analysis involves predicting eye characteristics with more than 1 million bits simulated. He highlighted goals and assumptions of IBIS-AMI models then contrasted serial channel topologies to DDR topologies. He showed that for a DDR channel with 2 DIMMs, each with 2 ranks, there can be 49,152 possible termination settings/transactions to analyze. For the study, he focused on the worst case transaction with optimized termination settings. When analyzing the transaction over multiple speeds, the voltage margin was better at 4400 MT/s than at 3600 MT/s. By analyzing the pulse response of the system, one can see that ISI is maximized at the sample point for the 3600 MT/s case. Todd noted that the main issue with the channel's SI isn't loss, but reflections (ringing). Tx FIR and Rx CTLE deal well with loss, but an Rx DFE is best suited to correct ISI from ringing. A theoretical eye opening can be computed from the pulse response, and increased numbers of DFE taps can improve eye height. Todd concluded that channel simulation techniques using IBIS-AMI models can be used to help design DDR5 systems that use equalization.

Jeff Shiba asked if package length needed to be considered in flight time analysis. Todd said it depends on how you specify timing. Todd noted that often signal quality at the pin is so bad that you can't do it. You do it at the pad and compensate for the package time.

Ken Willis asked if DDR designs tried to approximate a quasi-point-to-point channel. Todd noted that they try their best with termination. Todd noted that his approach in the presentation was to optimize termination for the non-equalization case, and then turn on equalization. He noted that this was easy, but not necessarily going to provide the best solution.

Ambrish Varma asked if different edge rates from single ended DDR simulations were a problem. Kumar noted that designers try to minimize edge rate differences because it kills their margins. Todd said it will be a question of what the reality of the actual circuit is.

Ken noted that he could envision many techniques to address signaling issues, for example a switch to dynamically shut off branches based on chip select. Todd said it would depend on the switch's performance, parasitic loading, cost, etc.

INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE

Michael Mirmak (Intel Corporation)
[Presented by Mike LaBonte (SiSoft)]

Mike LaBonte stated that BIRD189.4 was recently released by the Interconnect Task Group and is available for review. The BIRD is intended for IBIS Version 7.0, and its purpose is to improve package and on-die interconnect models by supporting IBIS-ISS and Touchstone models. This includes models of both I/O and supply connections. An optional die pad interface between pins and buffers is introduced. A one-to-one path connection is assumed for I/Os. Supply rails can have multiple terminals and be merged at the various interfaces. Mike showed some details of new keywords and subparameters as well as syntax examples. More revisions are in progress from the Interconnect Task Group.

IBIS-AMI DUAL MODELS: WHY THE JITTERS?

Mike LaBonte (SiSoft)

Mike LaBonte noted that a dual IBIS-AMI model has an AMI file with GetWave_Exists set to true and Init_Returns_Impulse set to true. This is the best option for running both time domain and statistical analysis. Mike reviewed some fundamentals of channel simulation including inputs and outputs of time-domain and statistical simulations, channel impairments, step response and pulse response analysis, eye height prediction from pulse response cursor analysis, and methods for all the ISI in a given channel. He then discussed jitter and noise impairments and equalization methods. He concluded that IBIS-AMI time domain simulation with AMI_GetWave can model non-linear effects such as DFE and saturation, but it can be impossible to simulate enough bits to prove the low BER requirements of some technologies. IBIS-AMI statistical simulation can quickly evaluate low BER, but it cannot see time-variant effects such as DFE and saturation. So, dual IBIS-AMI models are required.

Ken Willis noted that it was not uncommon to see Init-only models used for Tx devices, and that these could perform properly in a time domain simulation as well. Mike agreed.

Kumar Keshavan said that in practice many model makers simply don’t do statistical models. He said there are too many techniques and effects that can’t be properly modeled in Init. Validating models is expensive, so model makers won’t do it for a model that won’t perform properly. It can be difficult to justify doing an Init model, and some vendors only use GetWave based models. Kumar did suggest that a scenario in which GetWave based models were used to run an adaptive simulation to arrive at settings, and then an Init call utilized those settings, might be an effective way to get useful results from the statistical flow.

Ambrish Varma noted that some dual models relied on the results of adaptation done in the Init call, even when running GetWave, and those can be problematic. Q factor extrapolation of GetWave results could be used, so statistical simulation flow might not be the only means to get to low BER simulations.

CLOSING REMARKS

Mike LaBonte again thanked the sponsors SiSoft and Teraspeed Labs as well as EDI CON, the presenters, organizers and attendees.

The meeting concluded at approximately 4:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held September 15, 2017. The following IBIS Open Forum teleconference meeting is tentatively scheduled on October 6, 2017.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available

on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	July 14, 2017	August 4, 2017	August 25, 2017	September 13, 2017
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	X	-	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	-	-
GLOBALFOUNDRIES	Producer	Inactive	X	X	-	-
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	-
IO Methodology	User	Active	-	X	X	X
Keysight Technologies	User	Active	X	X	X	-
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	X
NXP	Producer	Inactive	-	-	-	-
Qualcomm	Producer	Inactive	-	-	-	-
Raytheon	User	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	X
Synopsys	User	Active	X	X	X	-
Teraspeed Labs	General Interest	Active	X	X	X	-
Xilinx	Producer	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	-

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.