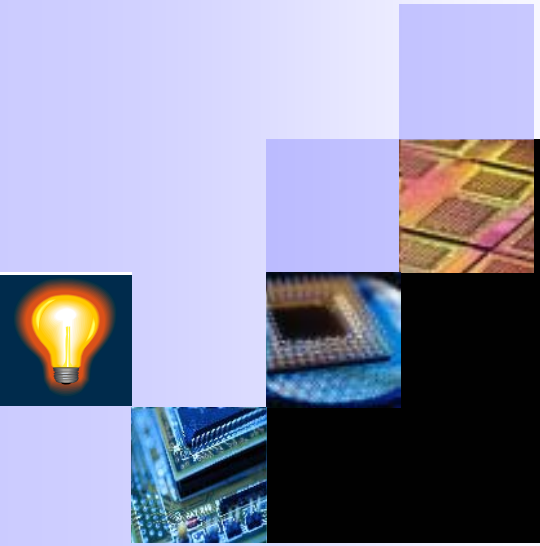

Power Delivery System Design Automation

A Proposal for Specification of System-Level Design Requirements

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Sigrity, Inc.

Asian IBIS Summit, Tokyo, Japan

September 14, 2007

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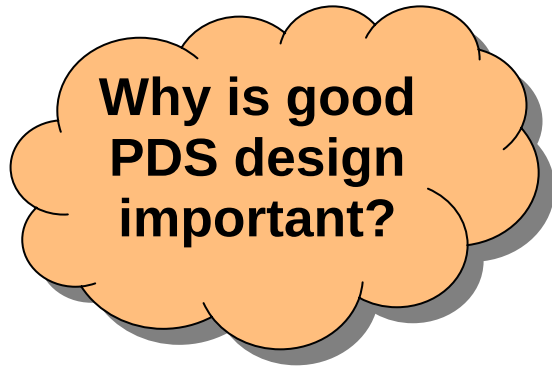
SIGRITY

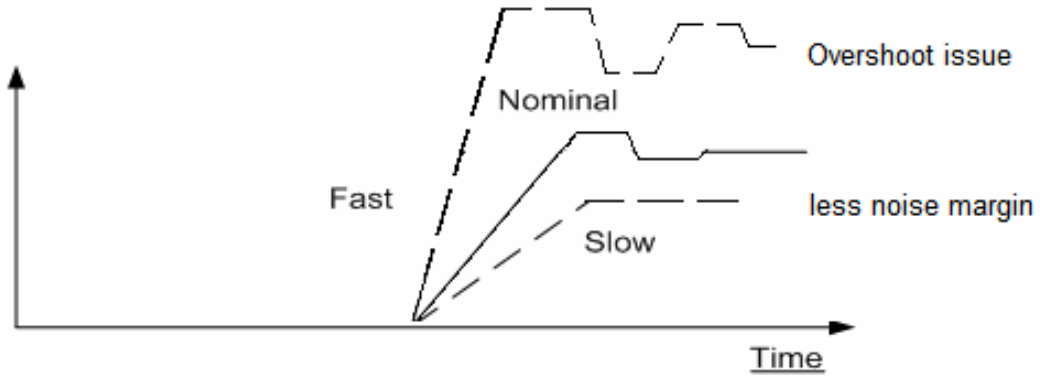
Agenda



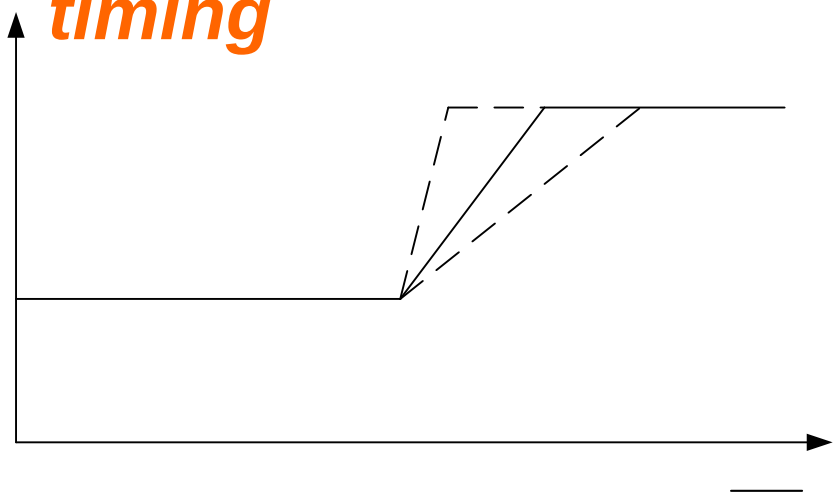
- ***PDS affects I/O performance***
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- PDS Design Flow

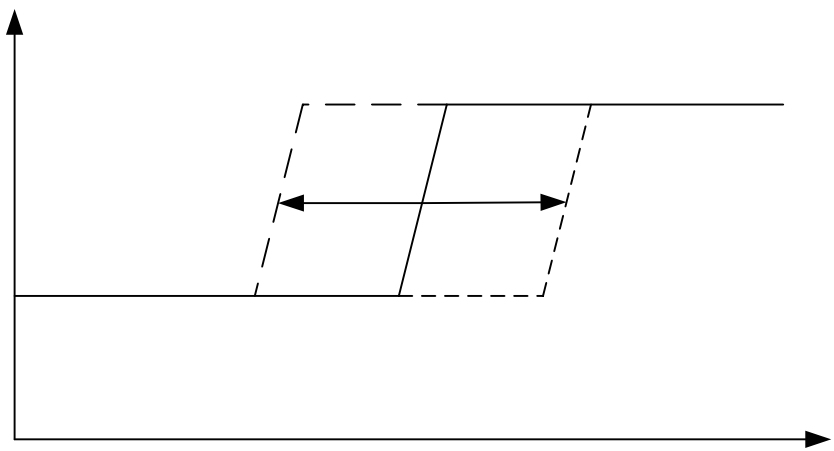
PDS Affects I/O Performance

- Noise from bad PDS affects ***signal quality***



- Noise from bad PDS affects ***timing***





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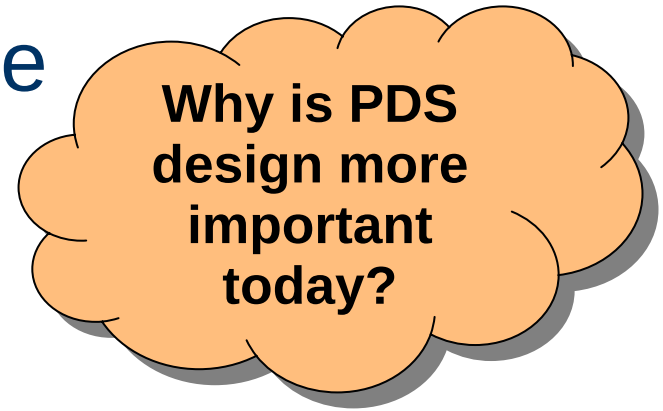
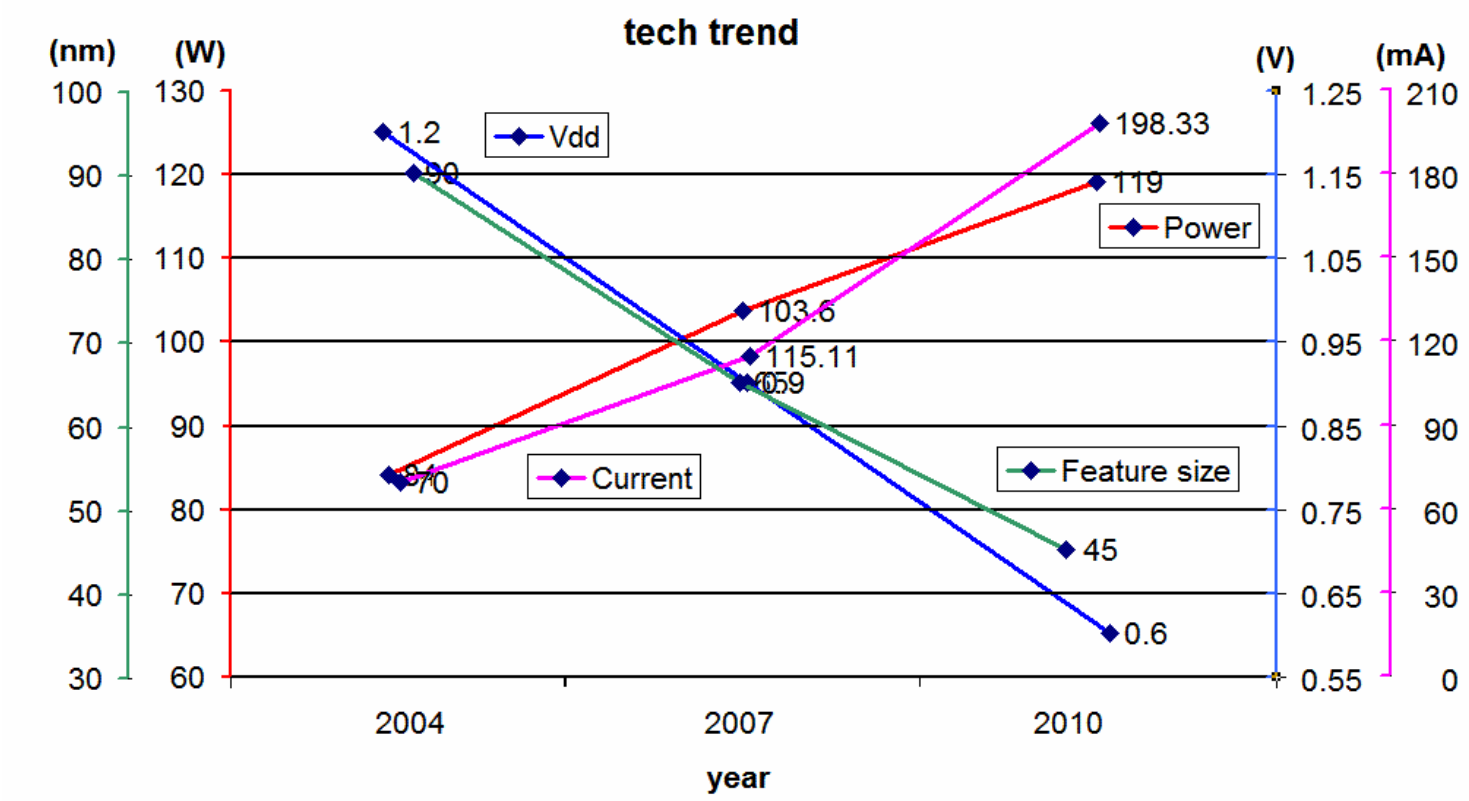


Technology Trends



- **With process size shrinking, system voltages dropping, load currents rising, and clock rates increasing,** good PDS design is now crucial to proper system performance.

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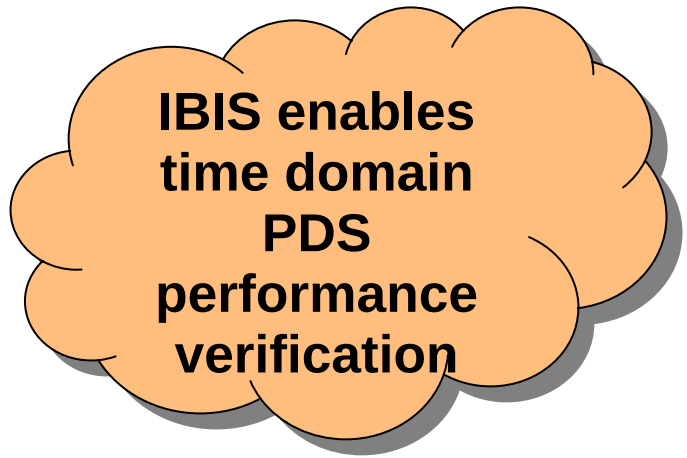
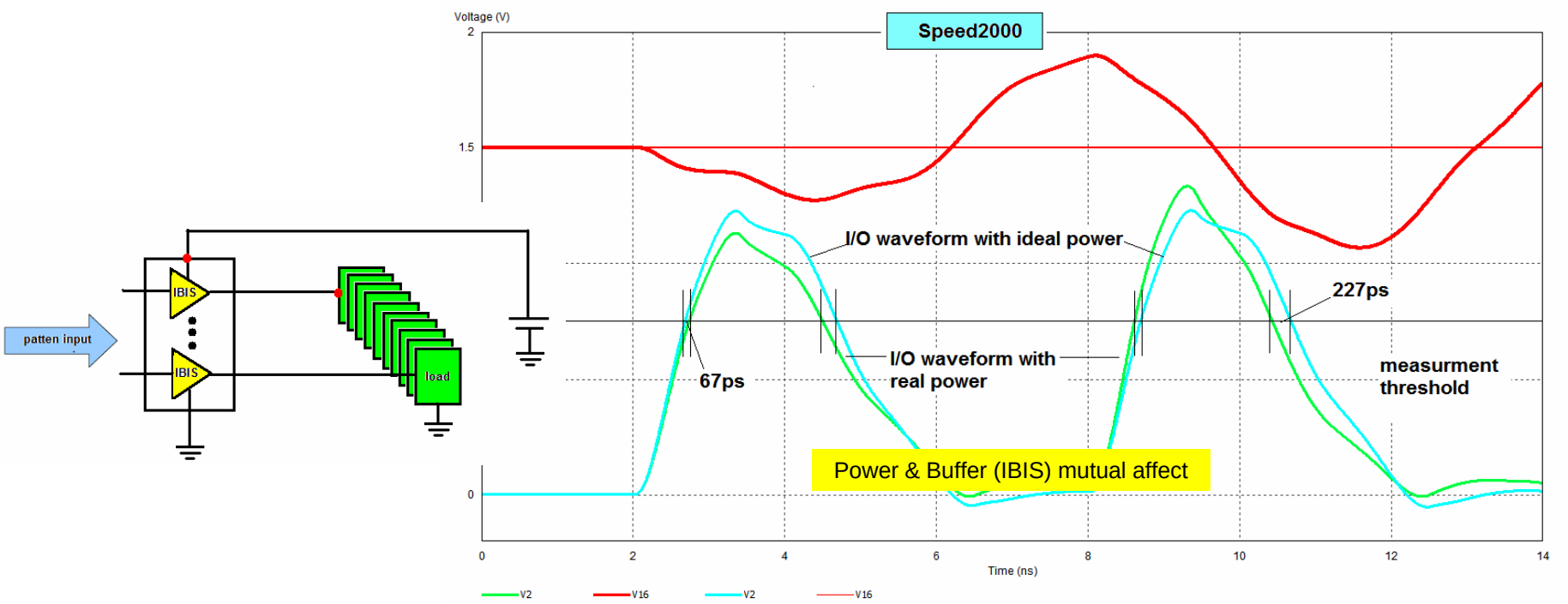


Time Domain Analysis

SSN analysis with IBIS



- IBIS provides an effective means to study how the PDS and signals interact
  - Direct indication of Peak-to-Peak noise
  - Produces signal waveforms with real power supply and return currents
  - Relies on pattern assumptions, one simulation for one input vector
- Common methodology to validate final performance of system

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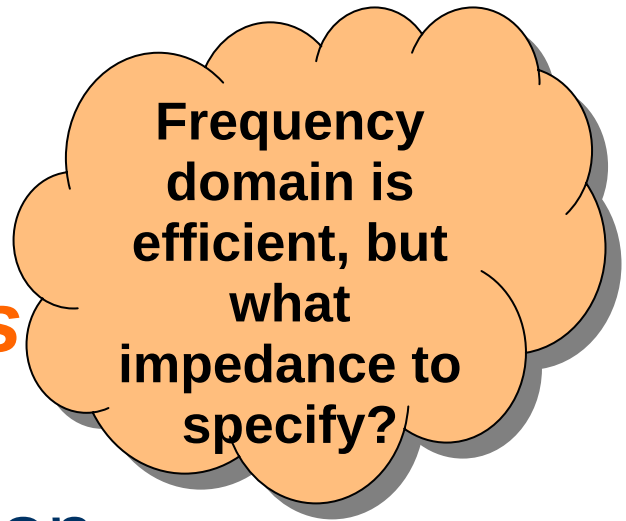
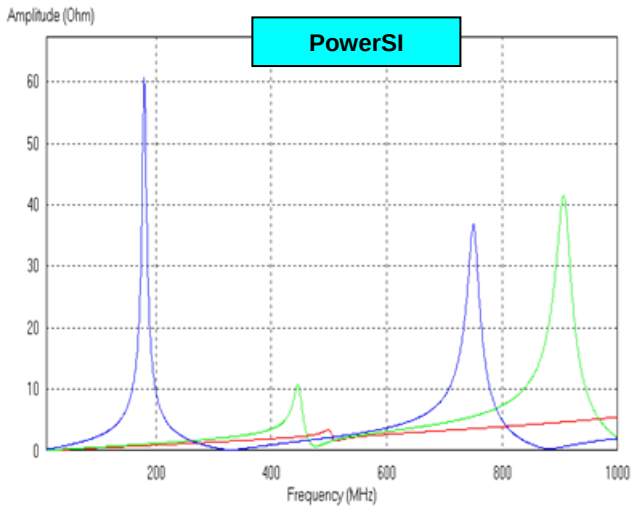
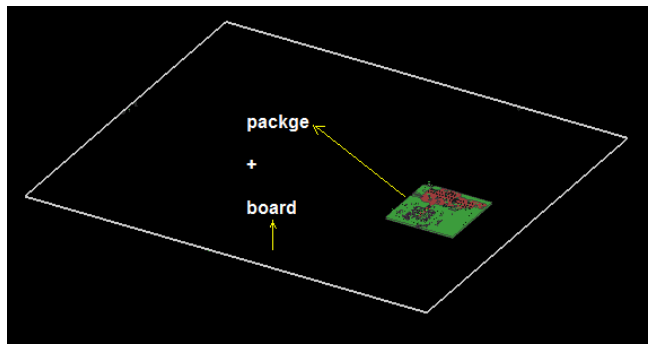
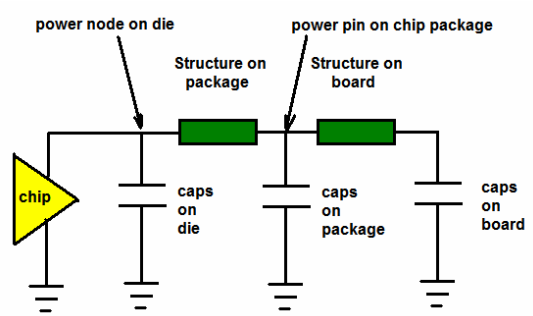


Frequency Domain Analysis
PDS impedance approach







- Higher PDS performance corresponds to lower input impedance seen from the component (chip) into the system.
- PDS impedance at the chip, looking into the package and board, can be simulated accurately with EDA tools, including the effects of: VRM, board, package, and decaps.
- PDS design success can be judged by comparison of actual impedance to a “target” impedance (*Z_target*).

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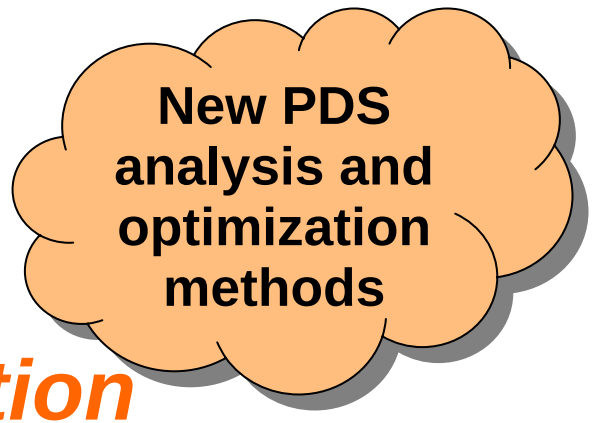
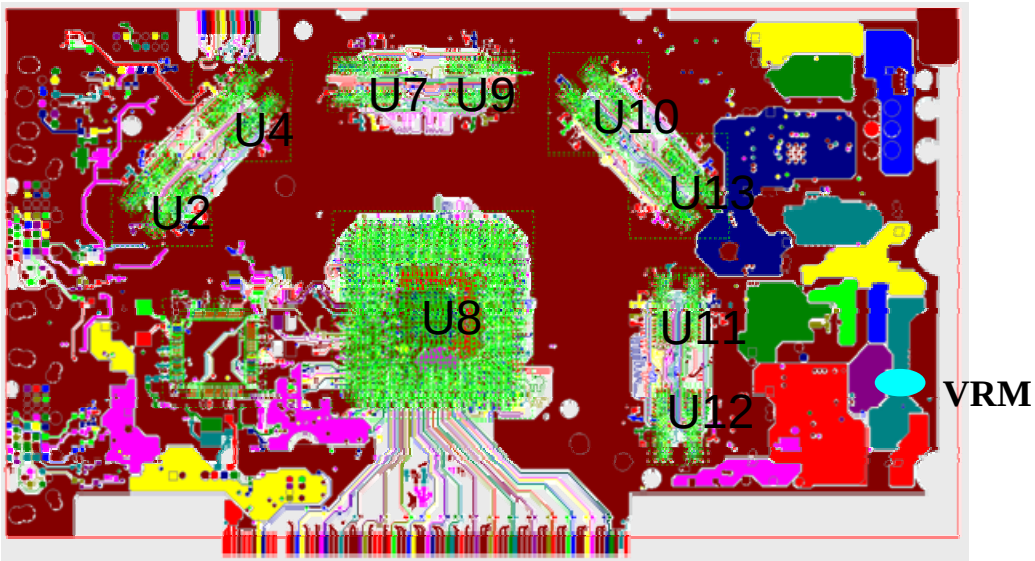
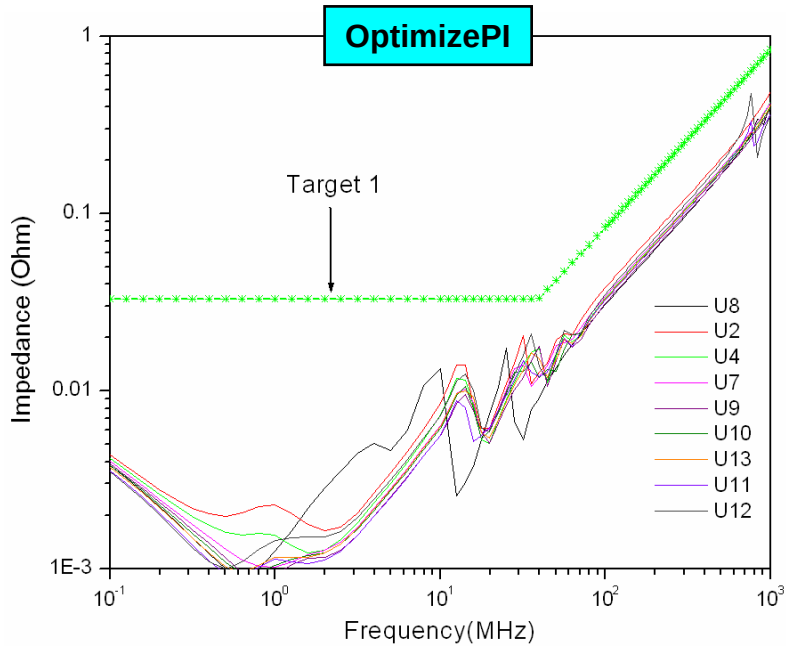


Automated PDS Design Flow
- Performance and Cost Optimization

- Input for PDS design
  - Physical: stack-up, layout, decap library
  - Electrical: initial decap placement, Z_target
- Analysis and Optimization tasks for PDS
  - Frequency domain, full-wave PDS analysis
  - Optimization of decap placement/selection
- Results of automated EDA design flow
  - Lowest manufacturing cost for specified system-level performance
  - Highest performance for a given cost target
  - Reduced design area
  - Interactive cost-performance tradeoffs

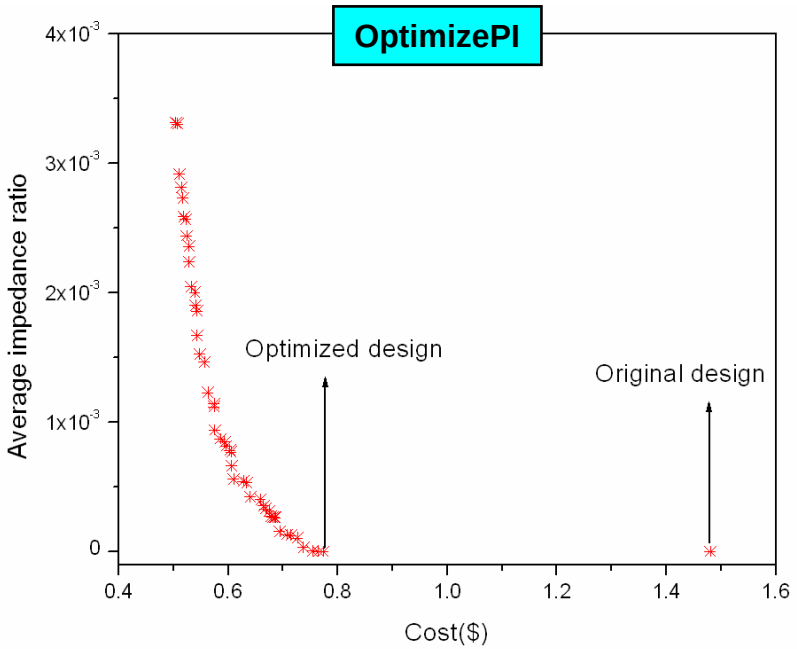
Case 1



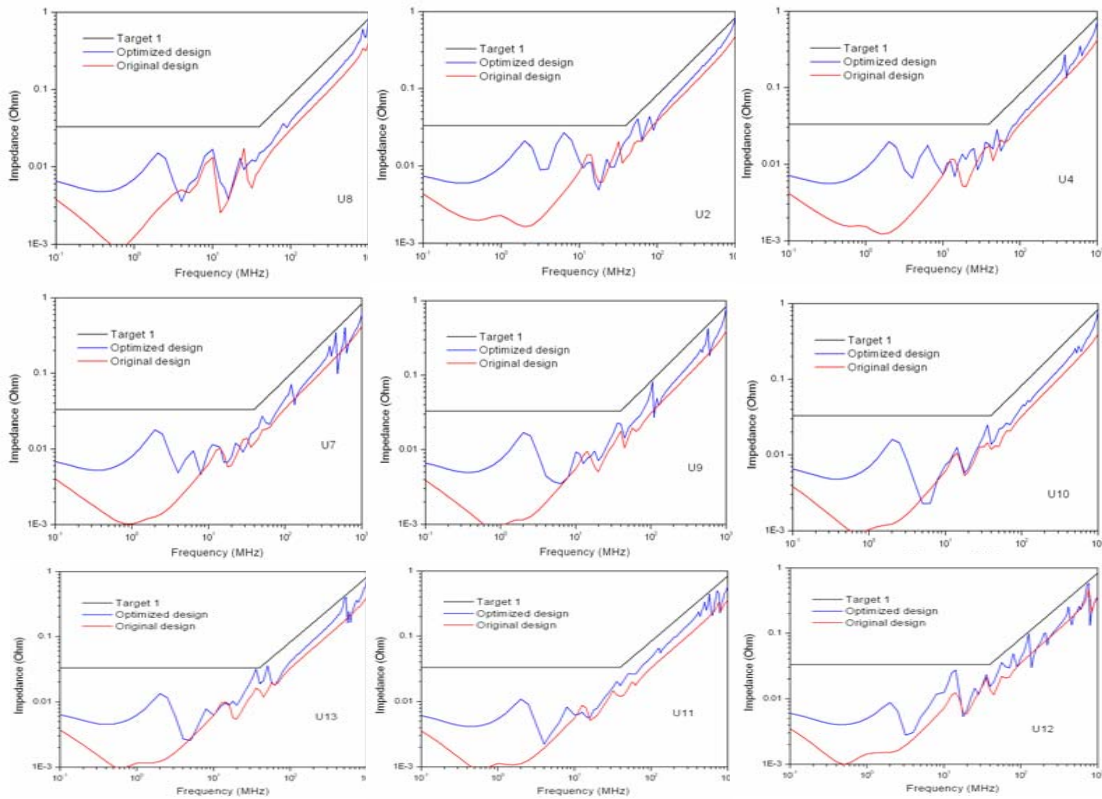


- Nine component impedances control the optimization process
- Green curve is the user-specified Z_target
  - Original design used as a reference

Optimum Performance vs. Cost



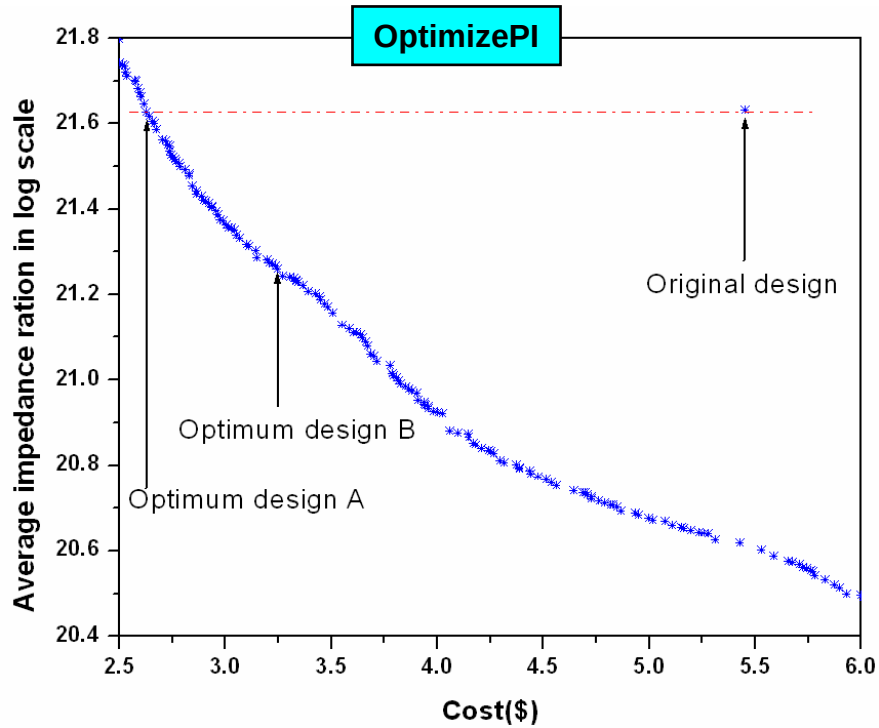
Design	Cost
Original	1.48
Optimized	0.77



- Cost reduced by half, while maintaining the required system-level performance
- Component-level performance details are shown

Case 2

- Eleven component impedances control the optimization process
- No Z_target was provided by component manufacturer
- Original design impedance used as the target
- Interactive cost-performance tradeoffs are examined



Capacitor Configurations

	Average Impedance Ratio	Cost($)
Original Design	**21.633**	**5.49**
Optimum Design A	**21.628**	**2.67**
Optimum Design B	**21.270**	**3.32**

Optimum Design A

Cap ID	Qty
1	1
2	3
3	5
4	13
5	5
6	45
20	4
23	4

Cost: **$2.67**

Optimum Design B

Cap ID	Qty
1	1
2	2
3	2
4	3
5	6
6	47
10	3
20	8
23	4

Cost: **$3.32**

Original Design

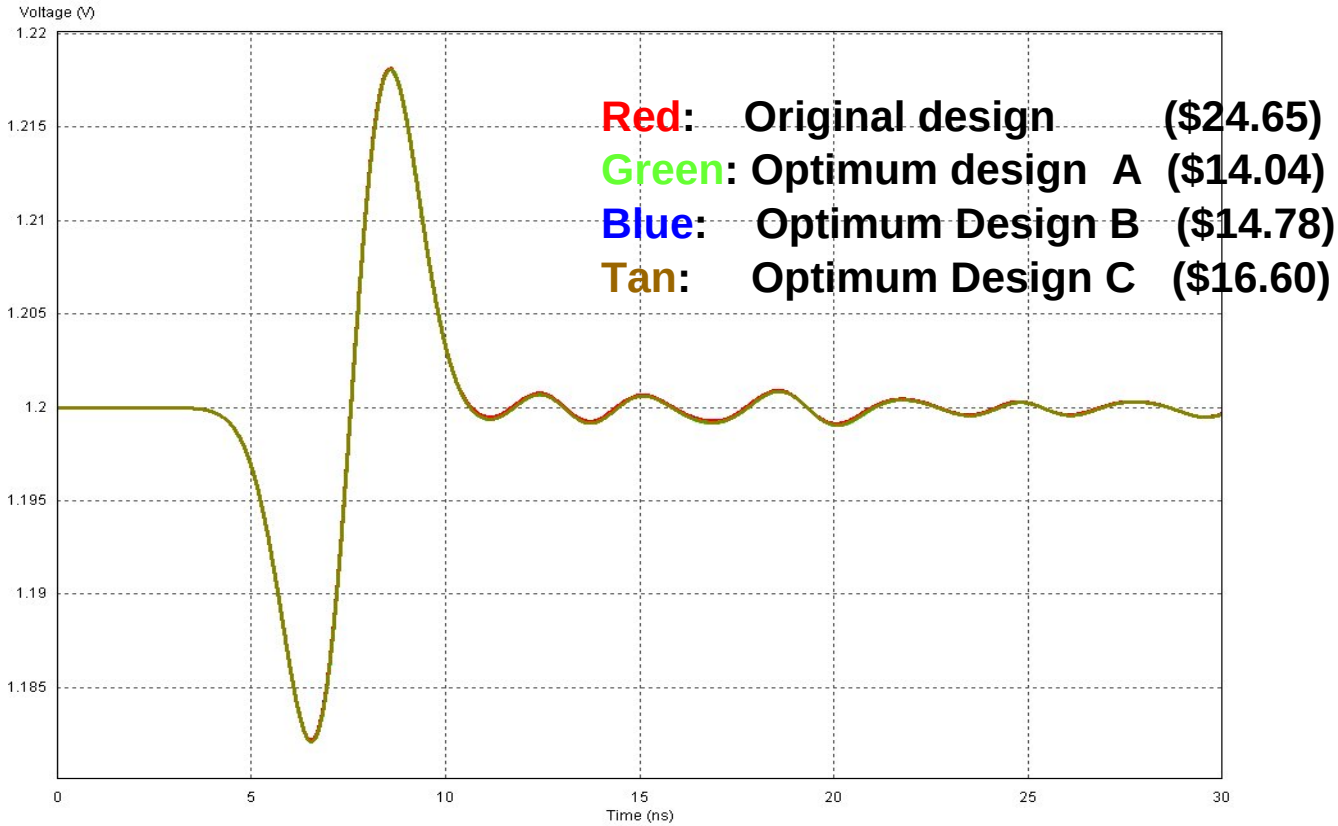
Cap ID	Qty
1	32
3	2
7	30
9	2
11	1
23	3
20	14
27	1
28	8

Cost: **$5.49**

- Interactive cost-performance tradeoffs quickly determine designs with both better performance and lower cost

Case 3 - Time Domain Verification

- Frequency-domain optimization is performed first
- All devices driven simultaneously with Gaussian current pulses
- Time domain voltage noise performance provides an alternative means of verifying the frequency-domain impedance performance prediction



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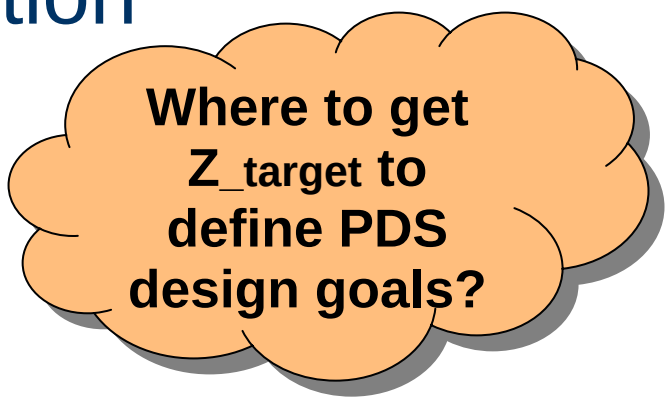
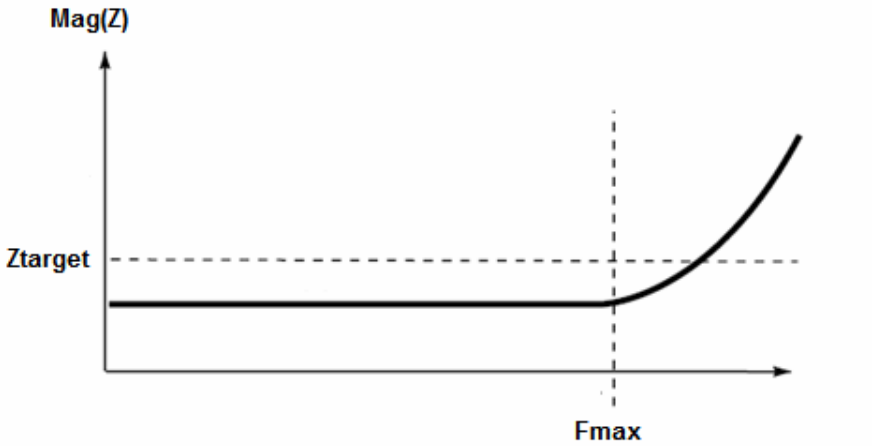


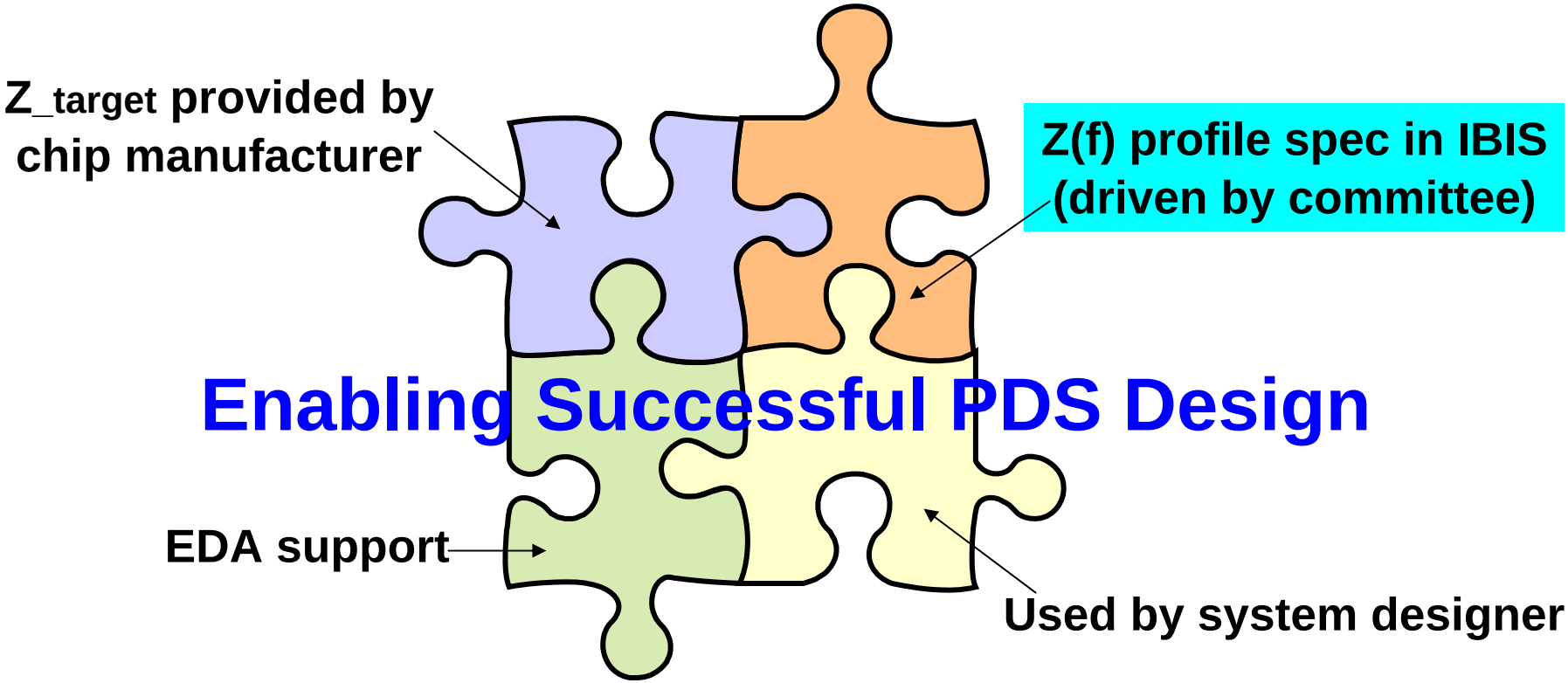
Target Impedance



$$Z_{target} = \frac{V_{dd} \times 0.05}{I \times 50\%}$$

- Z_target from simple calculation
  - more detailed and accurate simulations are usually available
- Z_target from reference design (*chip manufacturer*)
  - I/O cell design completed and can generate Z_target requirements
  - Available EDA tools are able to extract Z_target of reference and demo designs
- Z_target from previous successful designs (*system manufacturer*)
  - Meet or beat actual PDS impedance of previous generation system

Proposal for Z_target Specification in IBIS



A win-win-win scenario:

- System designers require Z_target to define PDS design goals.
- Chip manufacturer's existing component-specific PI knowledge can be leveraged in a standard manner.
- EDA vendors can provide support of Z_target specification in IBIS to enable automated and successful PDS design.

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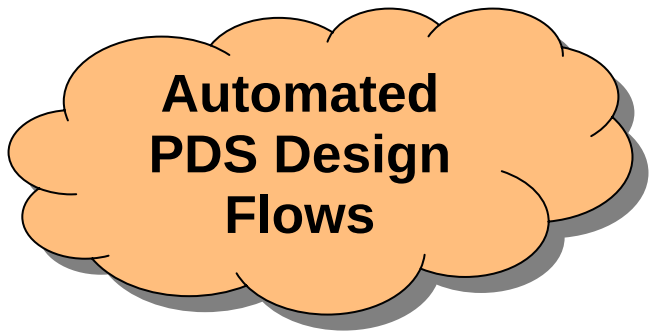
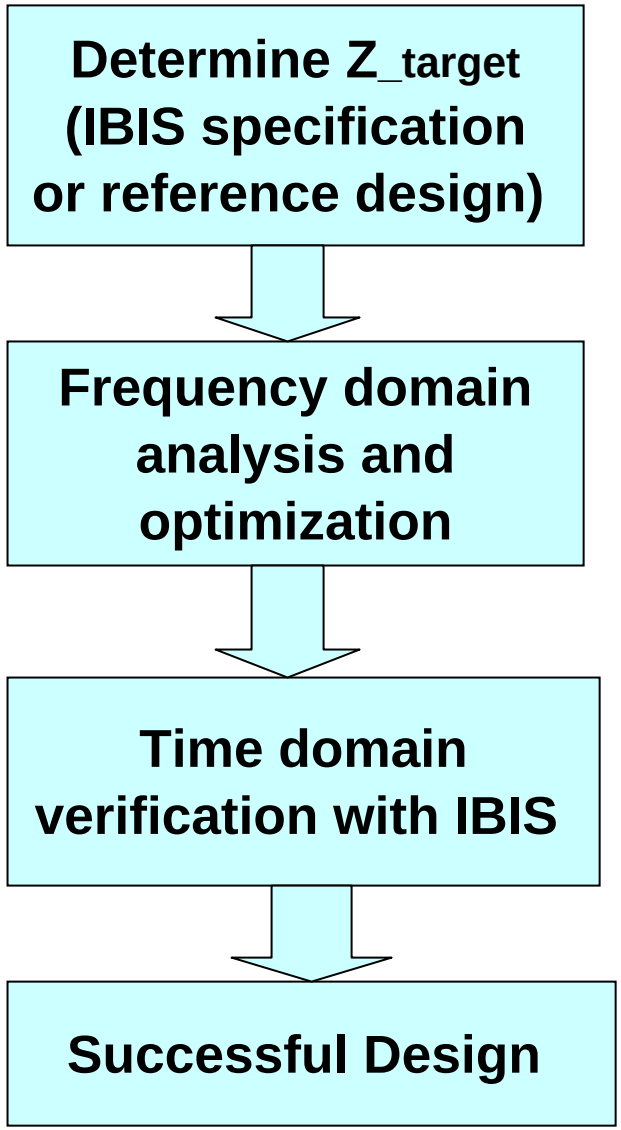


PDS Design Flow

- Z_target profile definition proposal
  - Leverages existing knowledge of chip vendors
  - Enables system design goals to be defined
- EDA vendors can quickly apply this information with PDS analysis and optimization tools
- Verification with IBIS in time domain is suggested, applying actual current profiles.



Sigrity, Inc.

Key to the Power and Signal Integrity Solution for IC Packages and PCBs