

# **JEITA EDA WG Activity**

**Sep 14, 2007**  
**IBIS Summit in Japan**

**JEITA EDA-WG**  
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*JEITA ; Japan Electronics and Information Technology Industries Association*

# **Outlines**

**1. JEITA EDA-WG Activities**

**2. Short Term Direction of JEITA EDA WG**

# 1. JEITA EDA-WG Activities

## Objectives

### Standardization activity of EDA Model

#### for **Digital Consumer Electronics**

Cellular Phone, LCD /PDP TV,  
Digital Camera/Video, DVD Recorder

(Digital , RF, and Analog circuits)

#### EDA Model

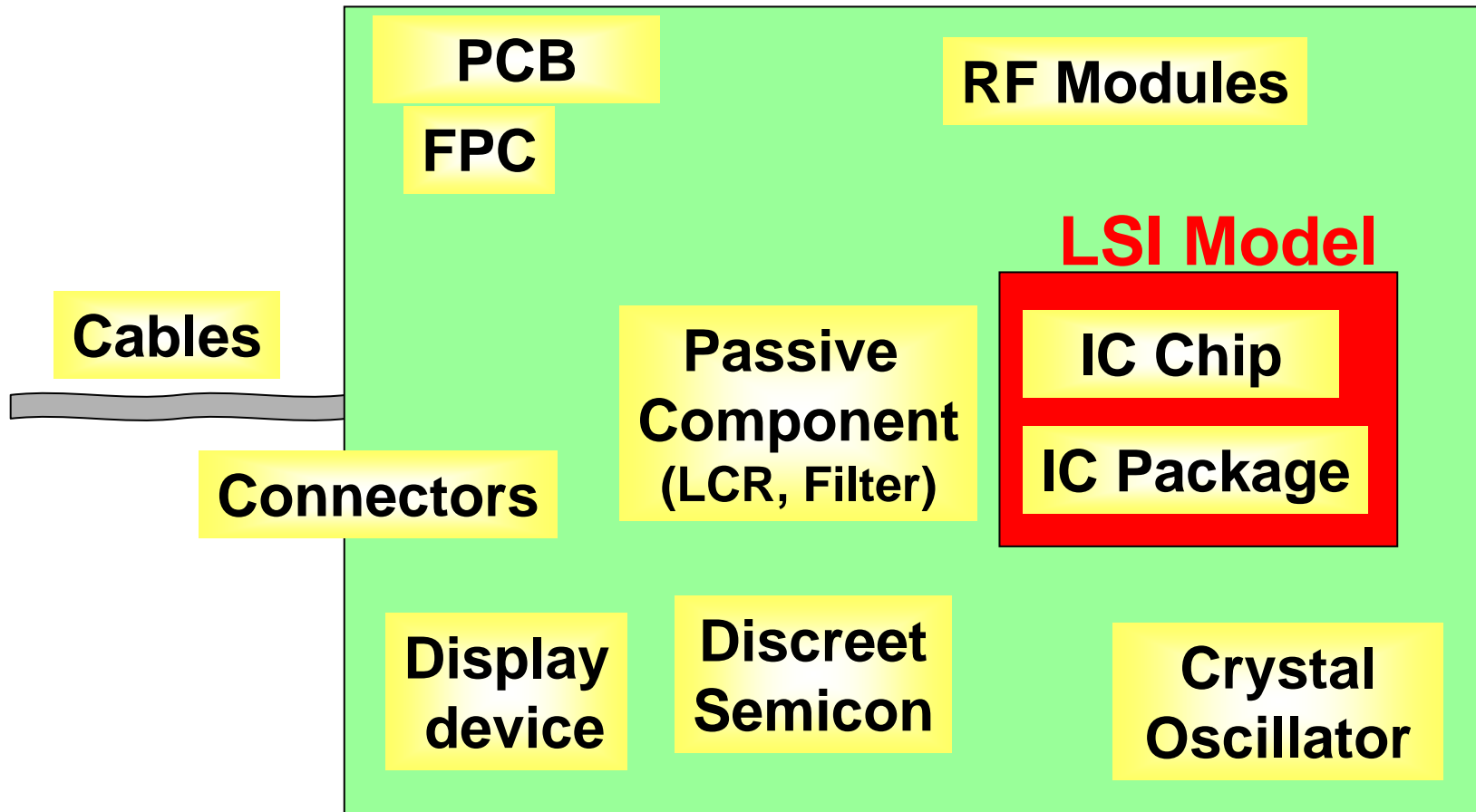
LSI: IBIS, Spice, etc.

Passive component: Interconnect Model, etc.

PCB: Dependent on EDA tool

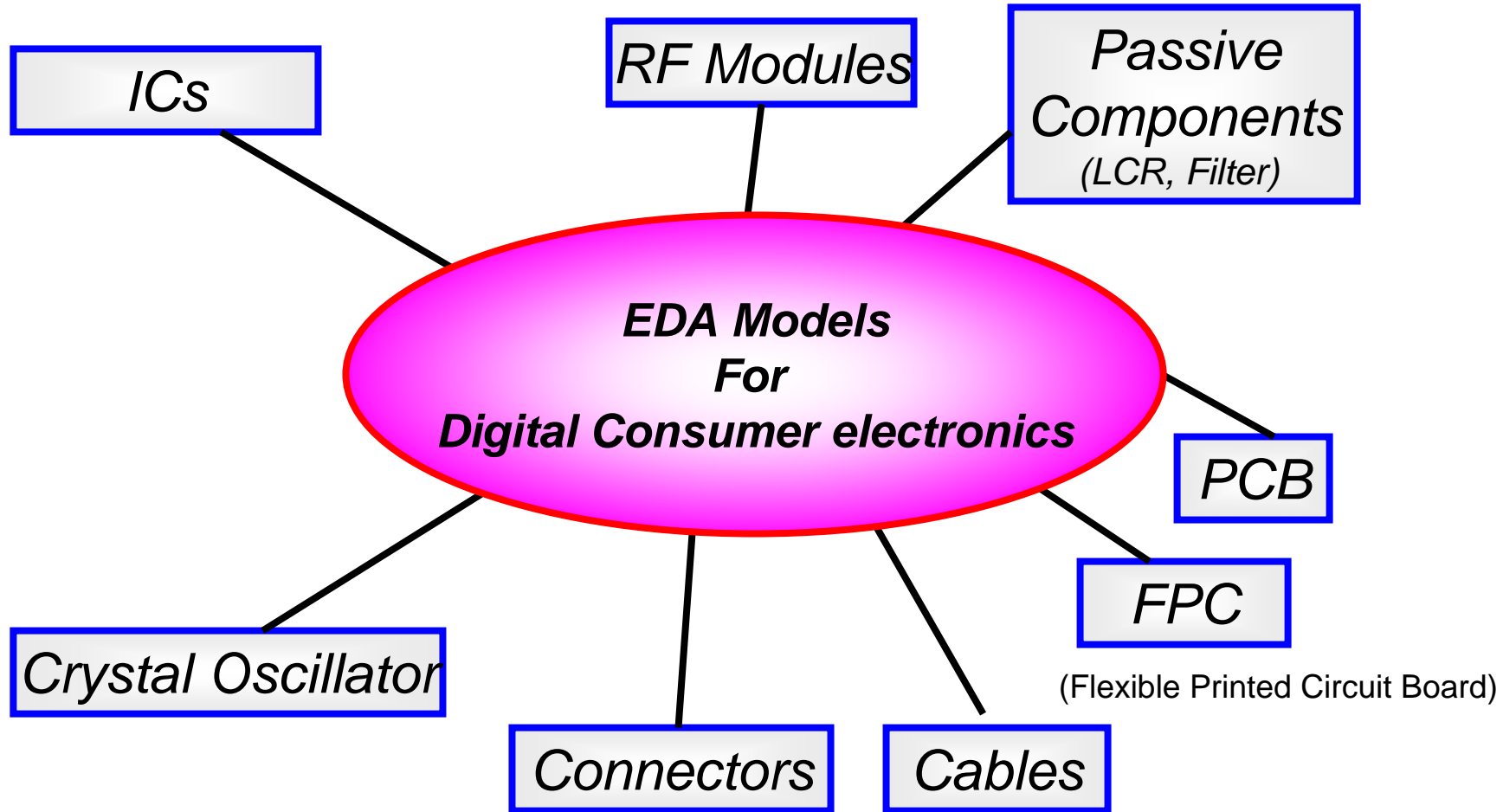
# EDA Model for EMI, SI and PI Simulation

## PCB whole level Simulation



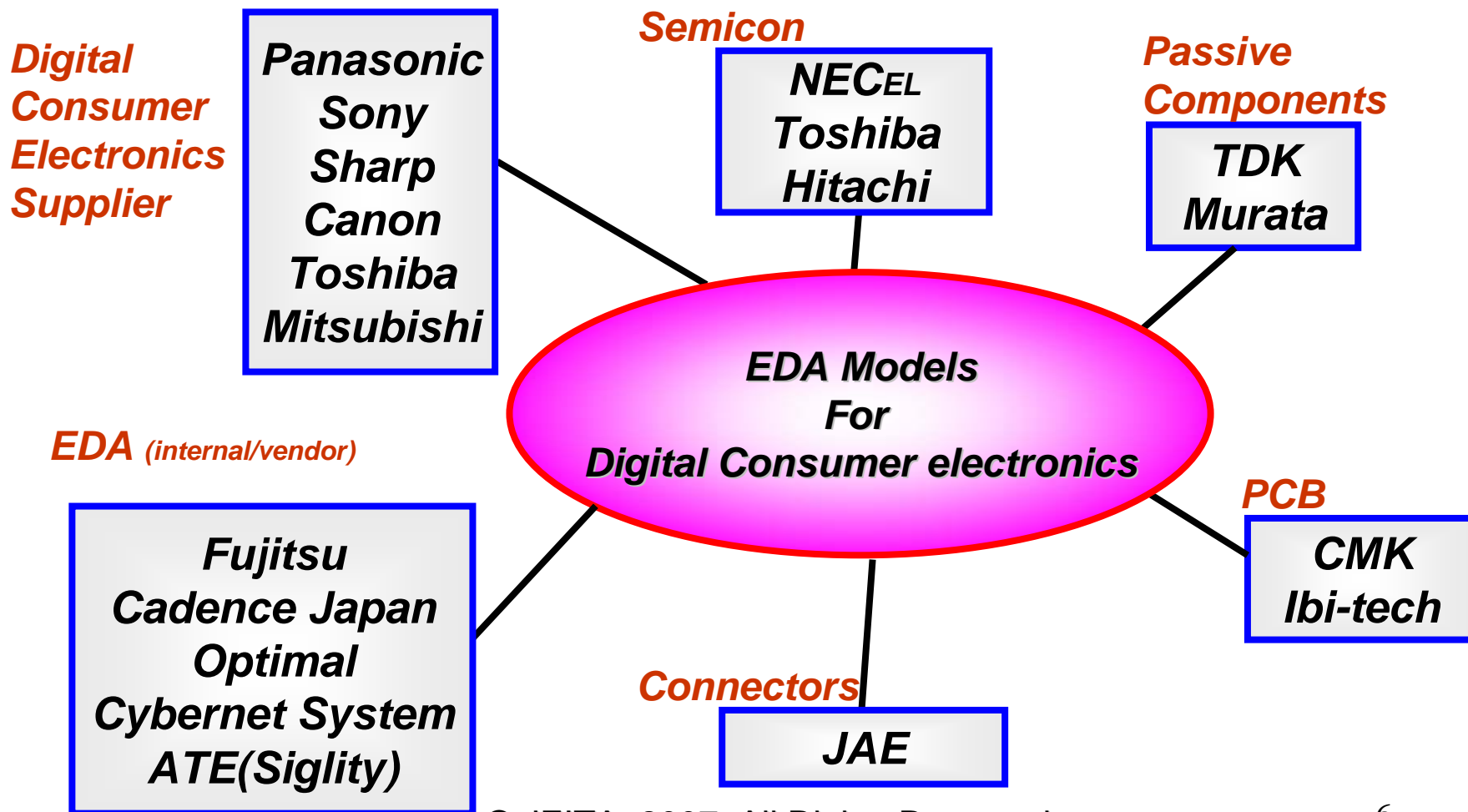
# Focus of EDA Model for Simulation

## 8 components



# JEITA EDA-WG Member

## 16 Major Companies



## 2. Short Term Direction of JEITA EDA WG

<Standardization activity of EDA Model>

### SI Simulation environment <1GHz

- Study of Interconnect Model

  - Passive Components and Connector**

    - \*Study of Interconnect Model (Mea. and Sim.) and standardization activities on these Model

    - \*\*JP Comments on ICM Model Touchstone 2.0

- IBIS Model Quality

  - Investigate and analyze the problem,

  - Comment to EIA/IBIS Quality Task Group

- IBIS guidebook for SI Simulation

- Technology exchange

  - IBIS Summit Japan co-organized by EIA/IBIS and JEITA

## Study of Interconnect Model

### IBIS Model Quality

		EDA Model					EDA Tool (recommned)	Environment for the usage of EDA Model
		ICs	Passive Componets	Connectors	PCB board	Cable		
SI	<1Gbps	0	0	0	0	0	0	0
	>1Gbps	0	0	0	0	0	0	0
EMI	<3GHz	0	0	0	0	0	0	0
PI	<3GHz	0	0		0		0	0

**Next stage**

0 foremost task

**JEITA IBIS Model Portal site Plan**

**IBIS guidebook for SI**



**Thank you for all the help  
EIA/IBIS Committee!**