

# Understanding and Using ICM Models

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# Topics

- IBIS ICM Model Introduction
  - What's IBIS ICM Model
  - What can we do with ICM model
  - ICM model structure
- ICM model usage scenario
  - Black box model
  - Package model
  - S-parameter support
  - ICM swath model support
- Summary

# IBIS ICM

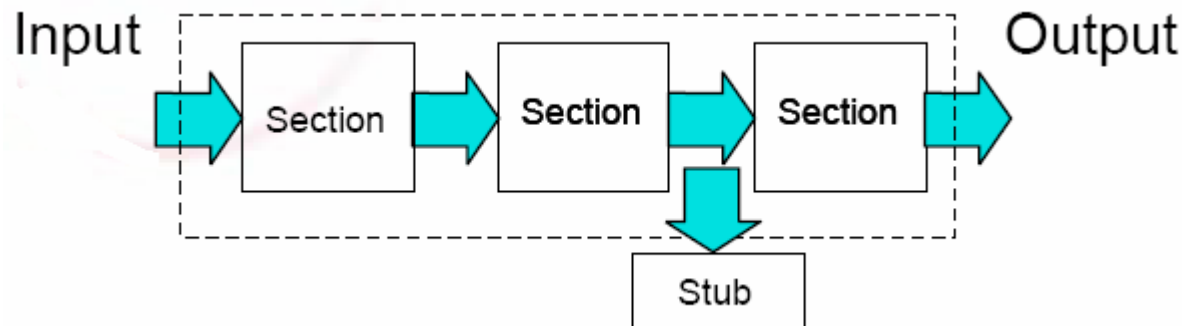
- **IBIS Interconnect Modeling Specification**
  - ICM stands for InterConnect Modeling
- **The goal of the ICM**
  - Provide a better, \*more accurate\*, non-proprietary interconnect data exchange format
    - Faster & **accurate** simulations
    - Smaller file size
- **ICM history**
  - Final Draft 1.0 released publicly May 16, 2003
    - See IBIS web site under “Connector Info”
  - Version 1.1 “ICM” specification approved in July 2005

# What can we do with ICM model

- ICM supports models for Connectors, PCB traces and IC-Packages
- ICM can include
  - RLGC Matrices
  - Swaths
  - S-parameters

# Section of ICM

- Each section is made up of a Single Line Model (SLM) or Multiple Line Model (MLM)
- A matrix section is a set of tables of numerical values that represent the electrical relationships between all conductors of a given geometry



- S-parameter can be used in place of RLGC matrix

## Section: ICM core unit structure

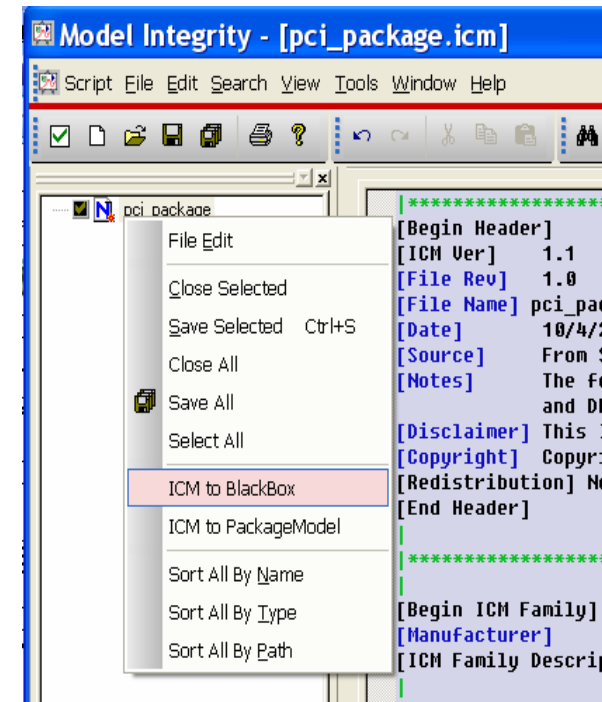
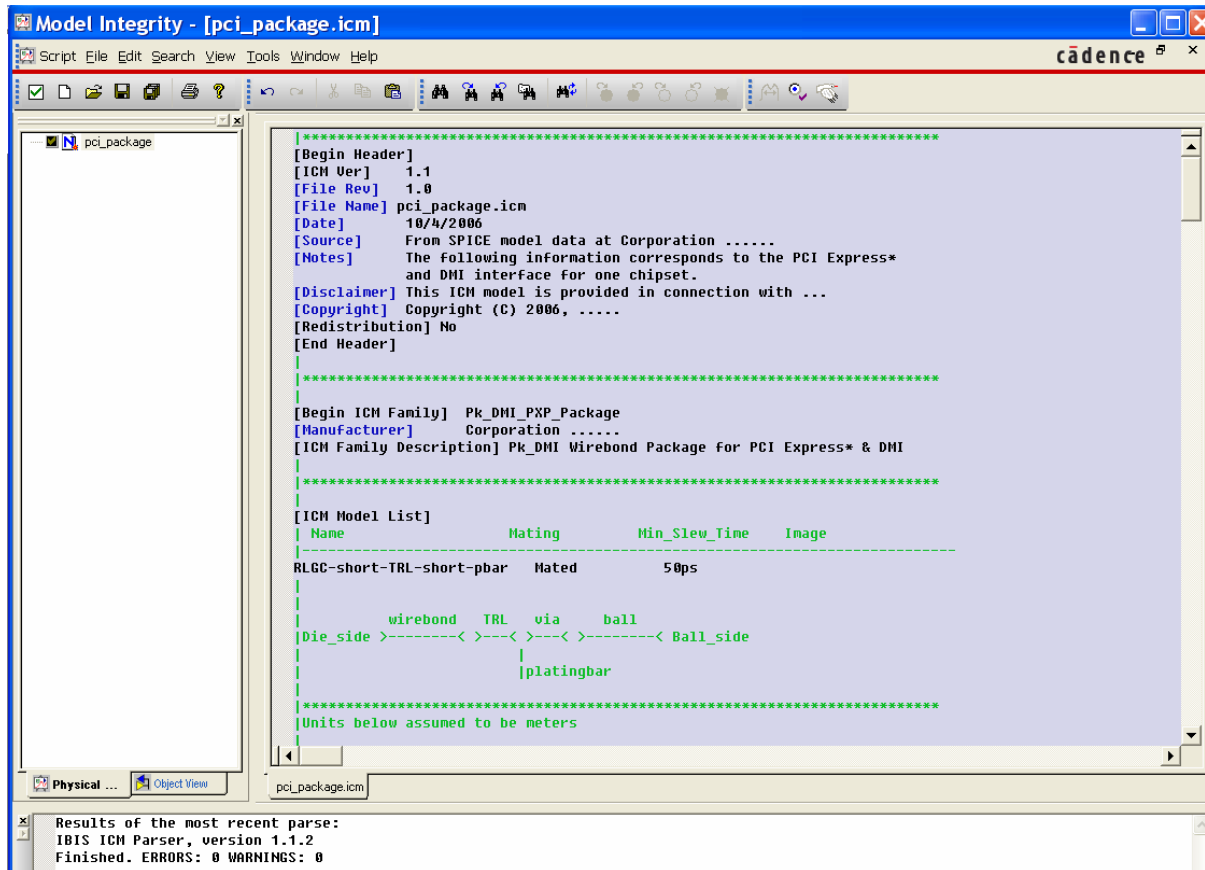
```
/--[Begin ICM Section]
|
|  --[Derivation Method]
|  --[Resistance Matrix]
|      /-- [Bandwidth]
|      |-- [Frequency]
|      \-- [Row]
|  --[Inductance Matrix]
|      /-- [Bandwidth]
|      |-- [Frequency]
|      \-- [Row]
|  --[Conductance Matrix]
|      /-- [Bandwidth]
|      |-- [Frequency]
|      \-- [Row]
|  --[Capacitance Matrix]
|      /-- [Bandwidth]
|      |-- [Frequency]
|      \-- [Row]
|
|  --[ICM S-parameter]
|      File_name
|      Port_assignment
|
|--[End ICM Section]
```

- Sections are basic units and core structure of one ICM model

# ICM model usage scenario

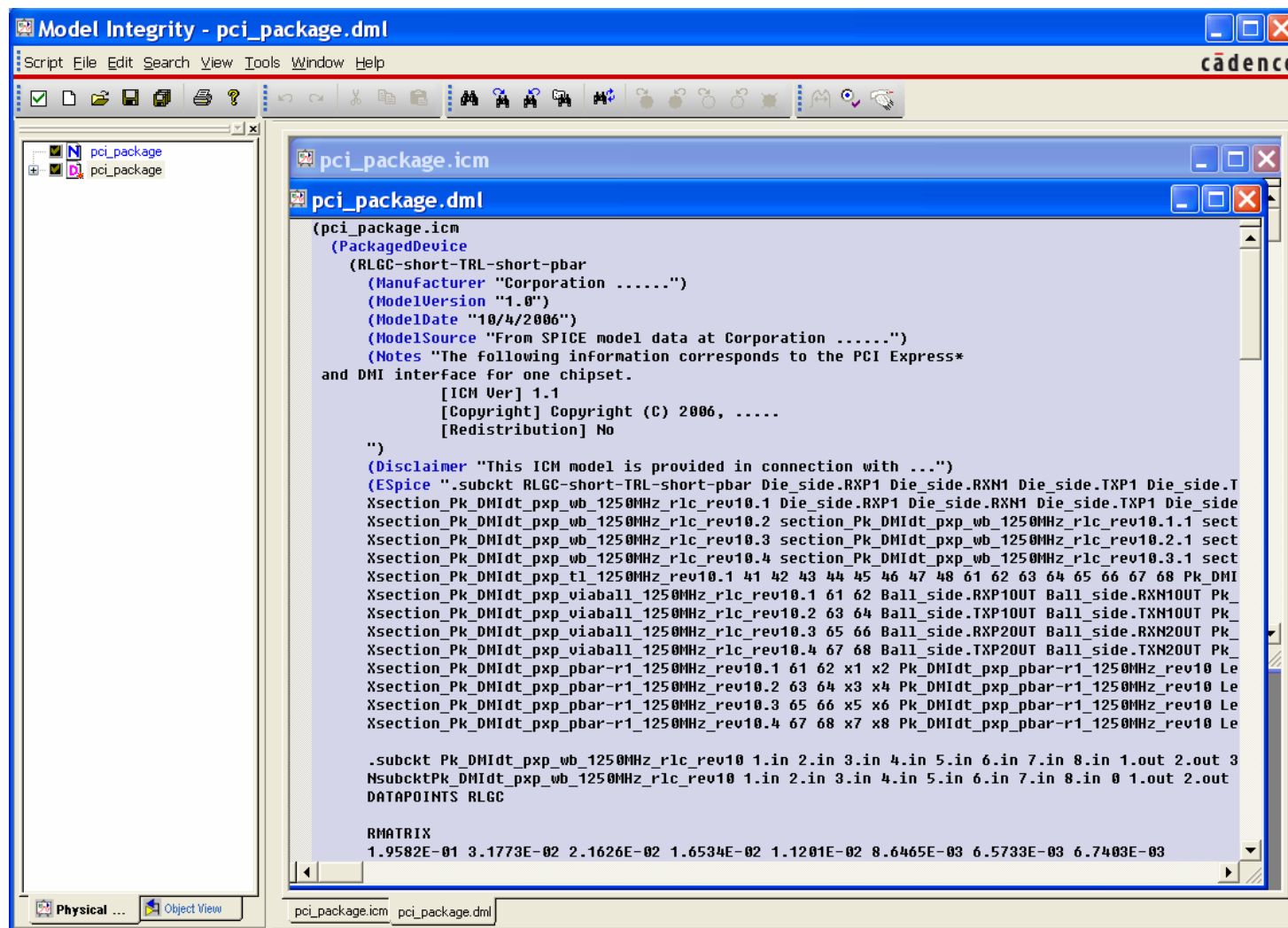
- ICM models can be used during pre-layout and post-layout analysis
- Two cases are presented
  - Case1: In pre-layout simulation, ICM model is used as a Black box model in a topology
  - Case2: In post-layout simulation, ICM package model is assigned to a component IBIS model on the PCB

# Example: ICM model of PCI express package



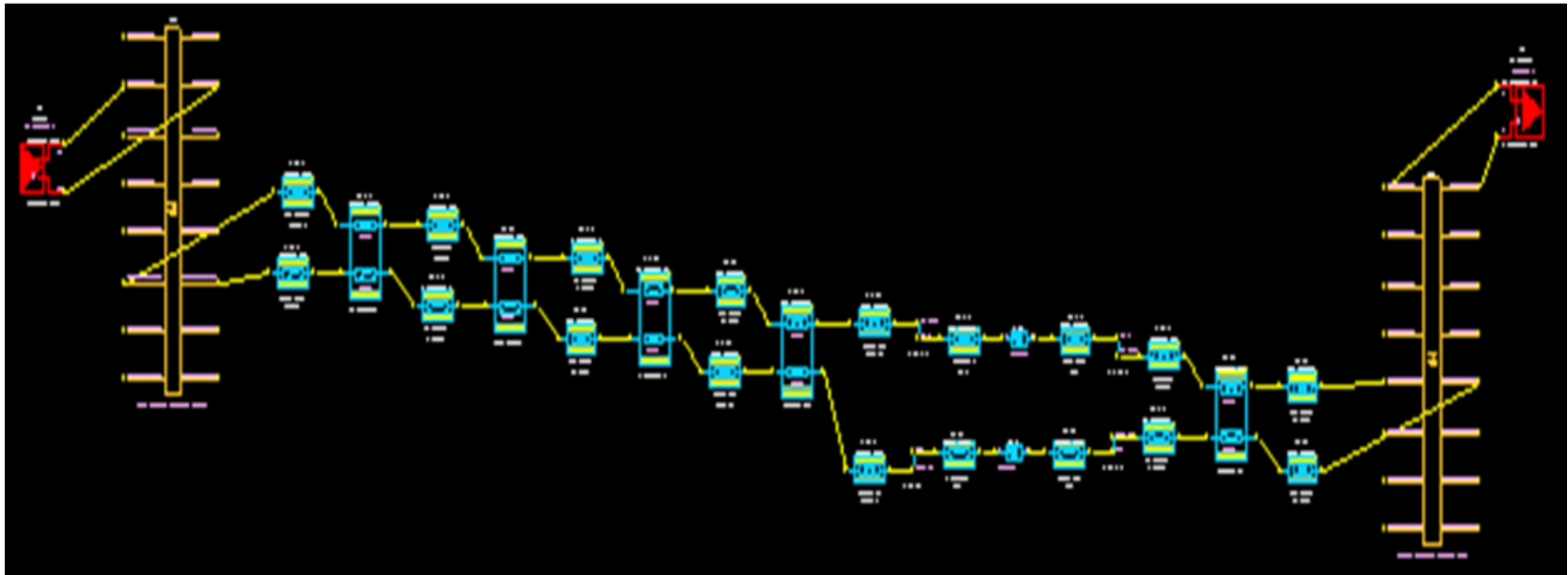


# Device model case (Black box model)

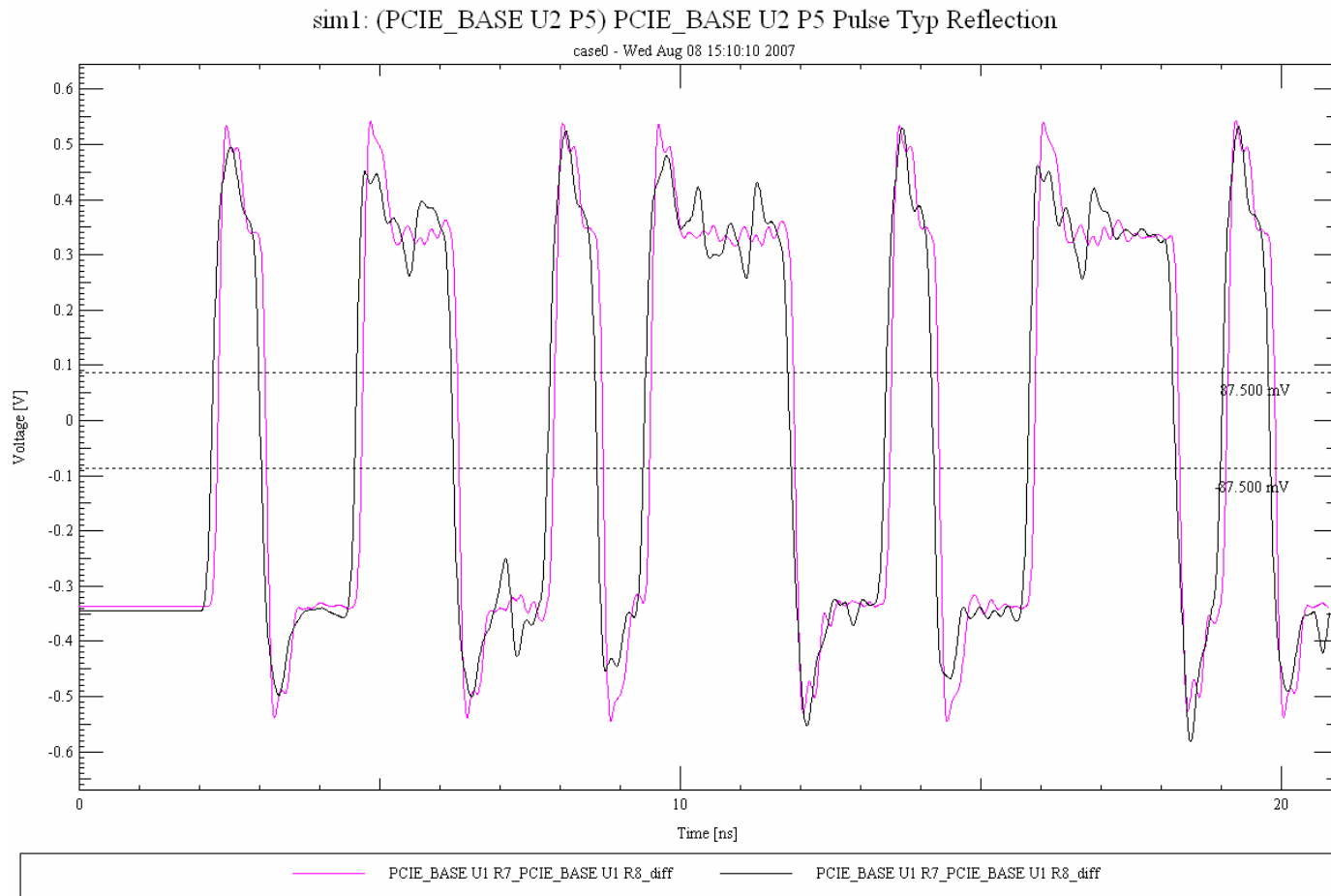


# Case 1: ICM acts as device model (Black box model)

- The package ICM model has been wrapped into one black box model, just like one connector



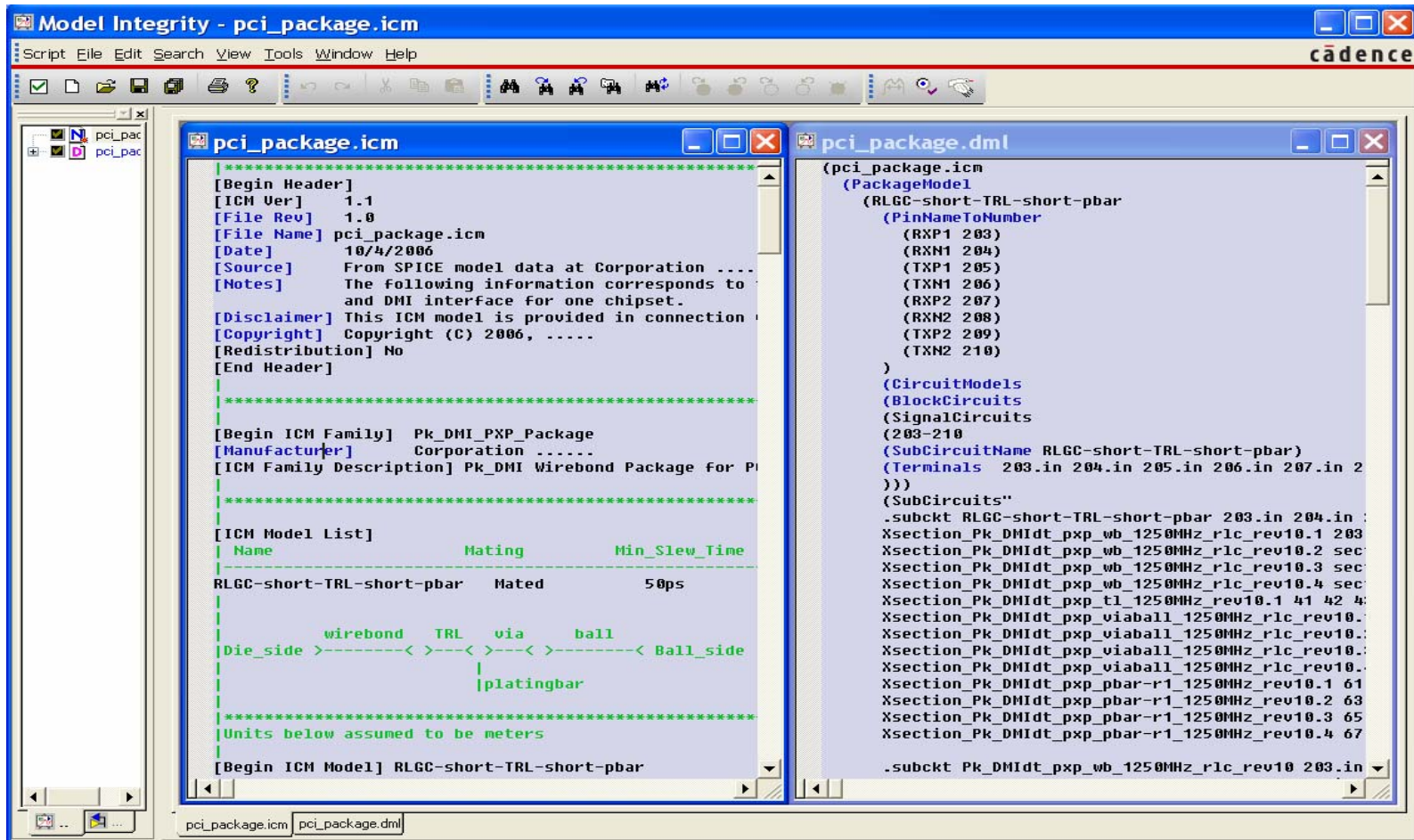
# Case 1: Simulation Results comparing (with/o ICM model)



The pink line represents the simulation with ICM model

The black line represents the simulation without ICM model

# Package model case (associating with its corresponding IBIS model)



The screenshot displays the Model Integrity application window with two files open: `pci_package.icm` and `pci_package.dml`.

**pci\_package.icm** content:

```
[Begin Header]
[ICM Ver] 1.1
[File Rev] 1.0
[File Name] pci_package.icm
[Date] 10/4/2006
[Source] From SPICE model data at Corporation ....
[Notes] The following information corresponds to
and DMI interface for one chipset.
[Disclaimer] This ICM model is provided in connection
[Copyright] Copyright (C) 2006, .....
[Redistribution] No
[End Header]

[Begin ICM Family] PK_DMI_PXP_Package
[Manufacturer] Corporation .....
[ICM Family Description] PK_DMI Wirebond Package for P

[ICM Model List]
-----
Name           Mating           Min_Slew_Time
-----
RLGC-short-TRL-short-pbar  Mated           50ps

wirebond  TRL  via  ball
Die_side >-----< >---< >---< >-----< Ball_side
          |
          |platingbar

Units below assumed to be meters

[Begin ICM Model] RLGC-short-TRL-short-pbar
```

**pci\_package.dml** content:

```
(pci_package.icm
(PackageModel
(RLGC-short-TRL-short-pbar
(PinNameToNumber
(RXP1 203)
(RXN1 204)
(TXP1 205)
(TXN1 206)
(RXP2 207)
(RXN2 208)
(TXP2 209)
(TXN2 210)
)
(CircuitModels
(BlockCircuits
(SignalCircuits
(203-210
(SubCircuitName RLGC-short-TRL-short-pbar)
(Terminals 203.in 204.in 205.in 206.in 207.in 2
))
(SubCircuits"
.subckt RLGC-short-TRL-short-pbar 203.in 204.in
Xsection_Pk_DMIdt_pxp_wb_1250MHz_rlc_rev10.1 203
Xsection_Pk_DMIdt_pxp_wb_1250MHz_rlc_rev10.2 sec
Xsection_Pk_DMIdt_pxp_wb_1250MHz_rlc_rev10.3 sec
Xsection_Pk_DMIdt_pxp_wb_1250MHz_rlc_rev10.4 sec
Xsection_Pk_DMIdt_pxp_tl_1250MHz_rev10.1 41 42 4
Xsection_Pk_DMIdt_pxp_viaball_1250MHz_rlc_rev10
Xsection_Pk_DMIdt_pxp_viaball_1250MHz_rlc_rev10
Xsection_Pk_DMIdt_pxp_viaball_1250MHz_rlc_rev10
Xsection_Pk_DMIdt_pxp_viaball_1250MHz_rlc_rev10
Xsection_Pk_DMIdt_pxp_pbar-r1_1250MHz_rev10.1 61
Xsection_Pk_DMIdt_pxp_pbar-r1_1250MHz_rev10.2 63
Xsection_Pk_DMIdt_pxp_pbar-r1_1250MHz_rev10.3 65
Xsection_Pk_DMIdt_pxp_pbar-r1_1250MHz_rev10.4 67
.subckt Pk_DMIdt_pxp_wb_1250MHz_rlc_rev10 203.in
```

# Case 2: ICM acts as package model

The screenshot displays a PCB layout in the background with a package model represented by a grid of pins. Overlaid on the layout are four dialog windows:

- Signal Model Assignment**: A table showing signal model assignments for various components.
- IBIS Device Model Editor**: A window for editing the upstream device model.
- Signal Analysis Library Browser**: A window for selecting device library files.
- Model Browser**: A window for selecting a model from a library.

**Signal Model Assignment Table:**

DevType	Value/Refdes	Signal Model	Source Library
+	CAP0_1U 0.1U	0_1u_cap	CurrentDesign
-	DOWNSTREAM	downstream	CurrentDesign
-	U2	downstream	CurrentDesign
+	PWR_CONN		
-	UPSTREAM	upstream	CurrentDesign
-	U1	upstream	CurrentDesign

**IBIS Device Model Editor - Model Info:**

- Model Name : upstream
- Manufacturer : Telian
- Package Model : RLGC-short-TRL-shc

**Signal Analysis Library Browser - Device Library Files:**

- Working: devices.dml
- package\_pci.dml
- devices.dml

**Model Browser - Show Models From:** Selected Device Library

**Model Browser - Model Type Filter:** Any

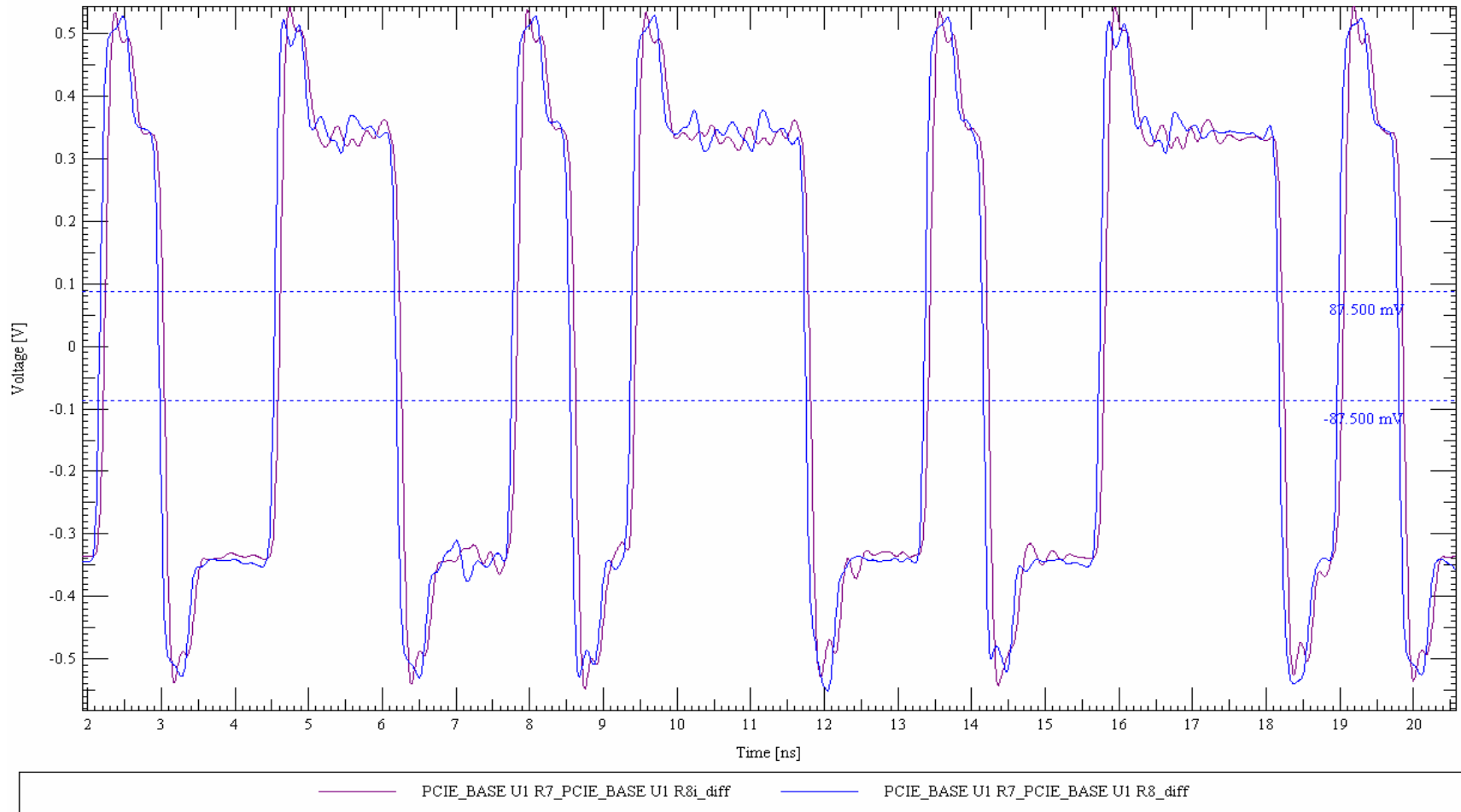
**Model Browser - Model Name Pattern:** \*

**Model Browser - ModelList:**

ModelName	ModelType
1 RLGC-short-TRL-short-pbar	PackageModel

ing device library 'D:/PV\_content/ModelIntegrity/16\_X/IBIS\_submit/pcb/devices.dml'  
ading SigNoise device libraries  
ing device library 'D:/PV\_content/ModelIntegrity/16\_X/IBIS\_submit/pcb/devices.dml'  
tion point

## Case 2: Simulation Results comparing (with/o ICM model)





# S-parameter support

The screenshot displays the Model Integrity software interface with three files open: test.icm, package.dml, and black\_box.dml. The test.icm file shows an ICM section for a connector, including port assignments and a list of ports (in1, in2, in3, in4, in5, out1, out2, out3, out4, out5). The package.dml file shows a single-line-connector model with terminals 1.in through 5.in and subcircuits for single-line-connector and connector. The black\_box.dml file shows a packaged device model with a single-line-connector and a connector subcircuit. All three files include a disclaimer and a table of port indices.

```
(test.icm
(PackageModel
(single-line-connector
(PinNameToNumber
(1 1)
(2 2)
(3 3)
(4 4)
(5 5)
)
(CircuitModels
(BlockCircuits
(SignalCircuits
(1-10
(SubCircuitName single-line-connect
(Terminals 1.in 2.in 3.in 4.in 5.in
)))
(SubCircuits"
.subckt single-line-connector 1.in
Xsection_connector.1 1.in 2.in 3.in

.subckt connector 1.in 2.in 3.in 4.
SSection_connector 2.in 1.out 4.out
DATAPOINTS SPARAM
R=50.000000 * IF R is missing the c
* The allowed data units are [HZ,KHZ,MHZ,
DATAUNIT=HZ * IF DATAUNIT is missin
* Note that the R and DATAUNIT statemen
* Each data point is in the real-imaginar
* !***** S-Parameters of a 10 p
* !
* ! PORT INDEX NO. ----> F
* ! 1 ----> 2
* ! 2 ----> F
* ! 3 ----> J
* ! 4 ----> 3
* ! 5 ----> L
* ! 6 ----> 5
* ! 7 ----> L
* ! 8 ----> L

[End ICM Family]
*****
[Begin ICM Section] connector
[Derivation Method] Lumped
[ICM S-parameter]
File_name test.s8p *in fact, the file na
Port_assignment
*Port Node
1 in2
2 out1
3 out4
4 out3
5 in4
6 out5
7 in1
8 in5
9 out2
10 in3
[End ICM Section]
*****
[End]

*****Modified by Cadence Design Systems
[ibis2signoise]
| VERSION= v16-1-39A
| INPUT= D:\PV_content\ModelIntegrity
| EXECUTED AT= Thu August 9 10:03:4
| FILE_MOD_TIME= Thu Aug 09 10:00:33
| OUTPUT= D:\PV_content\ModelIntegrity
| OPTIONS= -icm -u
|[icmchk.exe v16-1-39A]
| EXECUTED AT= Thu August 9 10:00:33

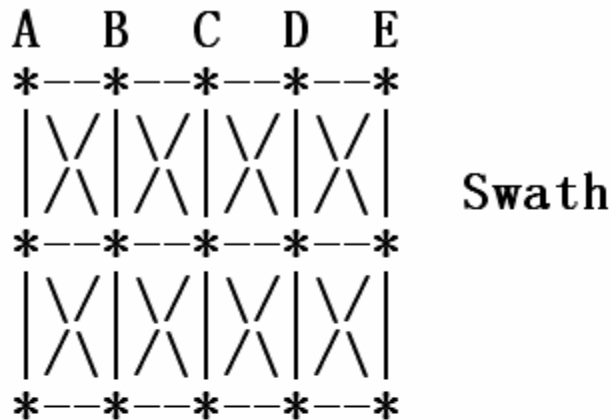
package.dml
(test.icm
(PackageModel
(single-line-connector
(PinNameToNumber
(1 1)
(2 2)
(3 3)
(4 4)
(5 5)
)
(CircuitModels
(BlockCircuits
(SignalCircuits
(1-10
(SubCircuitName single-line-connect
(Terminals 1.in 2.in 3.in 4.in 5.in
)))
(SubCircuits"
.subckt single-line-connector 1.in
Xsection_connector.1 1.in 2.in 3.in

.subckt connector 1.in 2.in 3.in 4.
SSection_connector 2.in 1.out 4.out
DATAPOINTS SPARAM
R=50.000000 * IF R is missing the c
* The allowed data units are [HZ,KHZ,MHZ,
DATAUNIT=HZ * IF DATAUNIT is missin
* Note that the R and DATAUNIT statemen
* Each data point is in the real-imaginar
* !***** S-Parameters of a 10 p
* !
* ! PORT INDEX NO. ----> F
* ! 1 ----> 2
* ! 2 ----> F
* ! 3 ----> J
* ! 4 ----> 3
* ! 5 ----> L
* ! 6 ----> 5
* ! 7 ----> L
* ! 8 ----> L

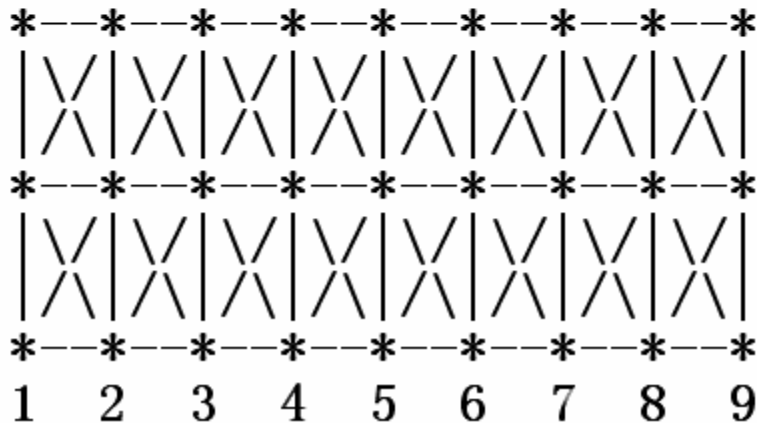
black_box.dml
(test.icm
(PackageDevice
(single-line-connector
(Manufacturer "Cadence HST
(ModelVersion "5.0")
(ModelDate "Sep/05/2006")
(ModelSource "Constructed
(Notes "Shanghai HSTC Team
if you have any questions, plea
[ICM Ver] 1.0
[Copyright] Copyri
[Redistribution] S
[Redistribution Te
")
(Disclaimer "This ICM mode
No license, express or implied,
otherwise, to any intellectual
by this document.")
(ESpice ".subckt single-li
Xsection_connector.1 plug.

.subckt connector 1.in 2.in
SSection_connector 2.in 1.
DATAPOINTS SPARAM
R=50.000000 * IF R is miss
* The allowed data units are [HZ
DATAUNIT=HZ * IF DATAUNIT
* Note that the R and DATAUNIT s
* Each data point is in the real
* !***** S-Parameters
* !
* ! PORT INDEX NO
* ! 1
* ! 2
* ! 3
* ! 4
* ! 5
* ! 6
* ! 7
* ! 8
```

# ICM Swath model support



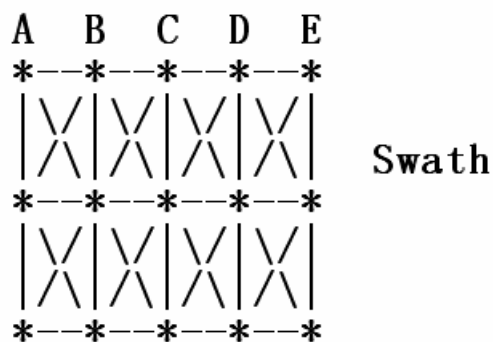
- Swath model
  - Is a method of using a small matrix section to define a much larger and variable size section of a connector
  - This facilitates faster simulation, smaller file size, and makes the creation of a family of connectors much easier



Full Interconnect



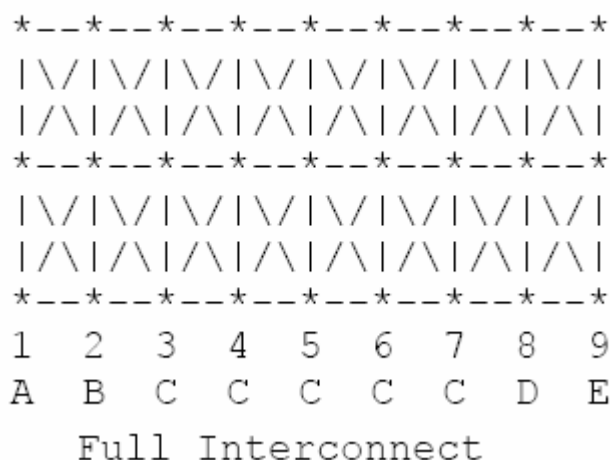
# Expanding the swath matrix



- **Three methods can be used to expand a swath matrix into a full-sized interconnect**

1. Centering the Swath around the pins of interest
2. Expansion and Centering: Expanding the Swath matrix into a larger sized Swath matrix and centering it about the paths of interest
3. Expansion to Full Sized Interconnect: Expanding the swath matrix to the full sized interconnect matrix

Mapping of the swath data





# Summary

- **ICM models offer open, non-proprietary way for vendors to provide interconnect models to their customers**
- **ICM models can be accurate for simulation at higher frequencies \*they can include coupling\***



Thanks!

**cā dence<sup>TM</sup>**

A decorative graphic at the bottom of the slide. It consists of a large, dark purple triangle on the left that tapers to a point on the right. A red vertical bar is positioned at the bottom right, partially overlapping the tip of the purple triangle.