

*Asian IBIS Summit*

# Modeling and Simulation for Multi-Gigabit Interconnect System

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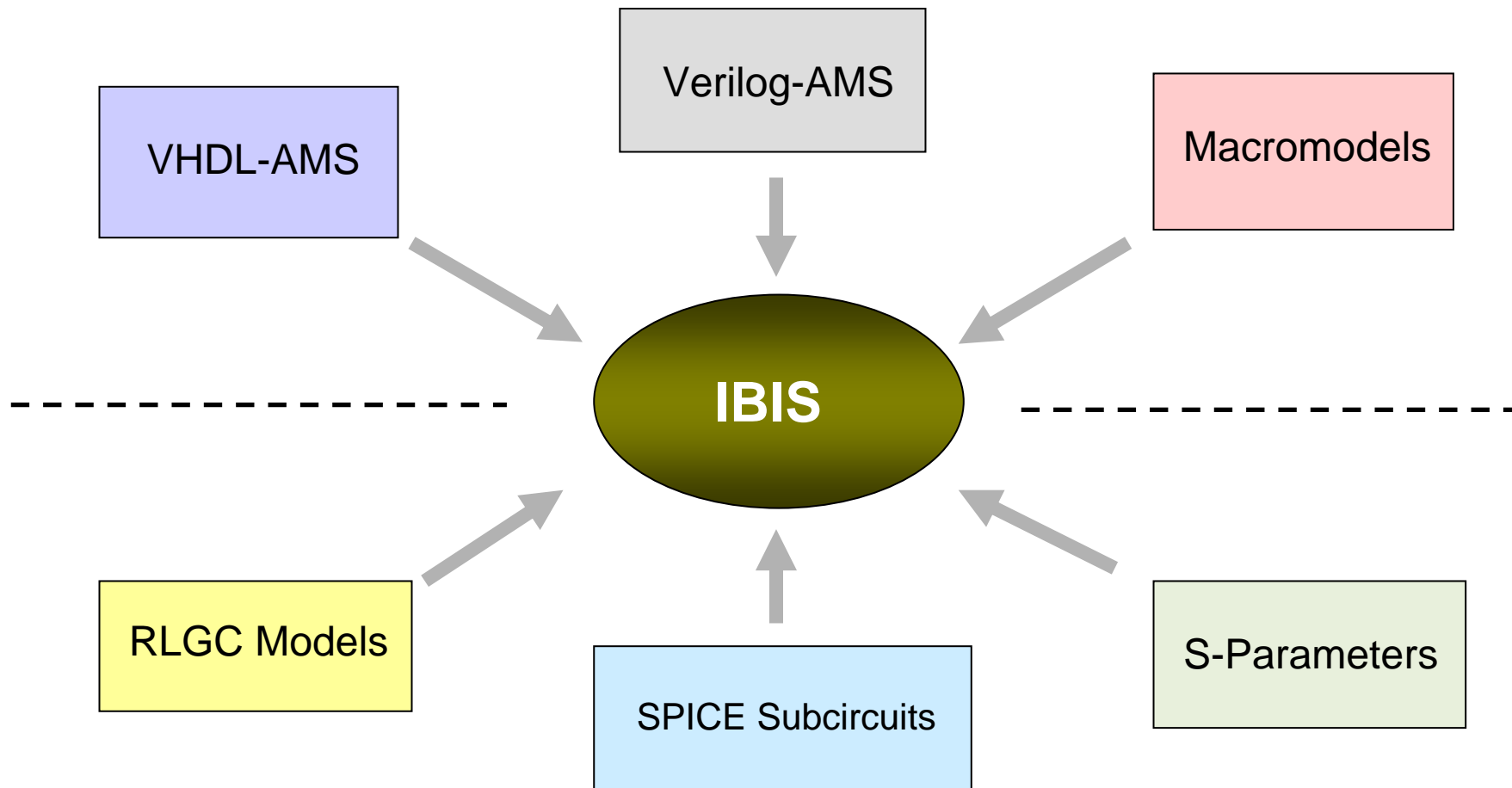
# Agenda |

- Modeling Methodologies
- Behavioral-level Interconnect Modeling
- Lab Correlation for Macromodels and S-parameters
- Eye diagram analysis and design margin budget
- Conclusions

# Modeling Methodologies

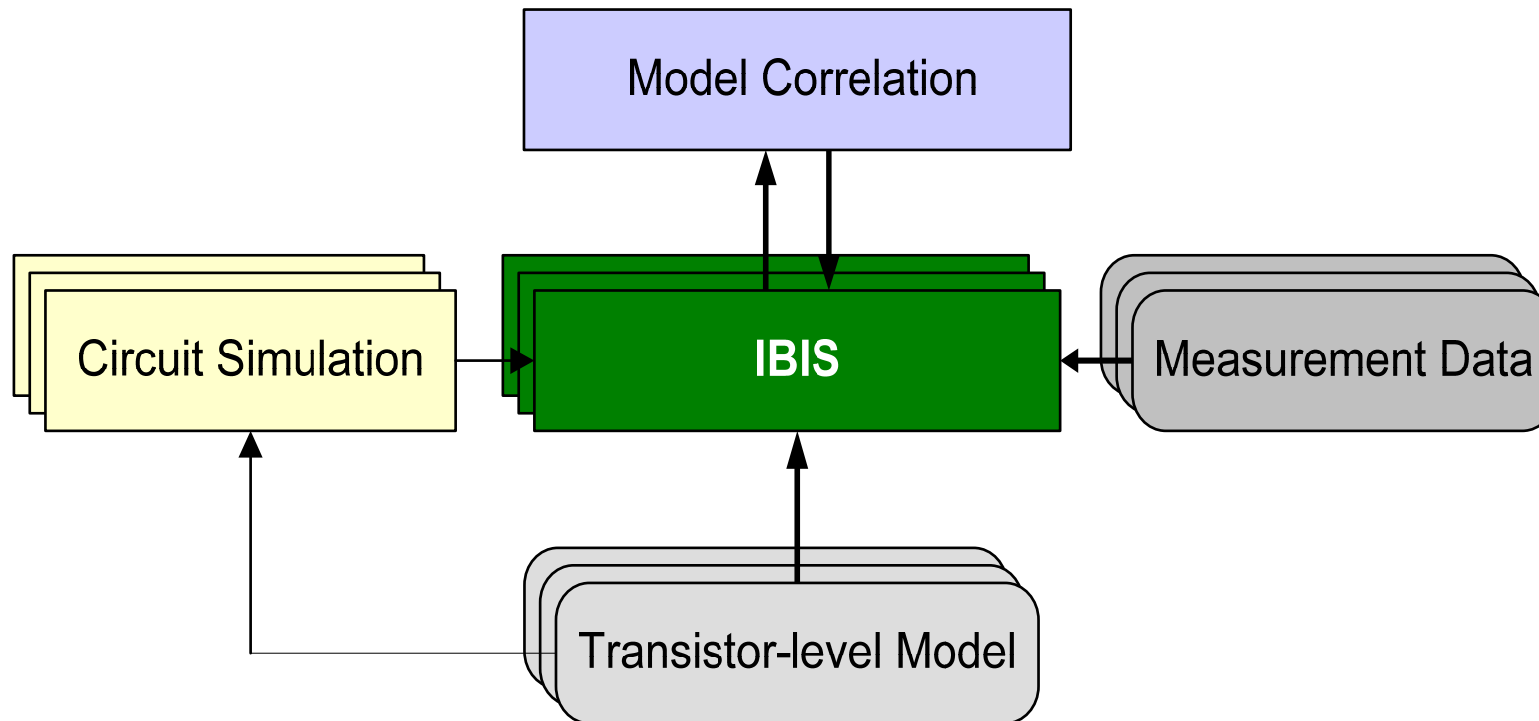
- There are behavioral IBIS and structural Spice modeling for active devices. Spice model is appropriate for demanding situations, while IBIS model is often used in system and board level simulation.
- Choose an appropriate modeling method is critical for simulation. Otherwise simulation may not be accurate enough or too complex and time consuming.
- For multi-gigabit interconnect system design, behavioral-level model enables much faster simulation time than transistor-Level spice model.
- Modeling covers active devices as well as passive devices, such as package, transmission line, connector, via, and plane etc..
- Modeling methods have tradeoffs and are suitable for different applications. Multi-Gigabit Interconnect System design requires that the interconnect modeling must be valid over a wide bandwidth.
- For behavior-level modeling, correlation is necessary.

# IBIS Multi-lingual Modeling

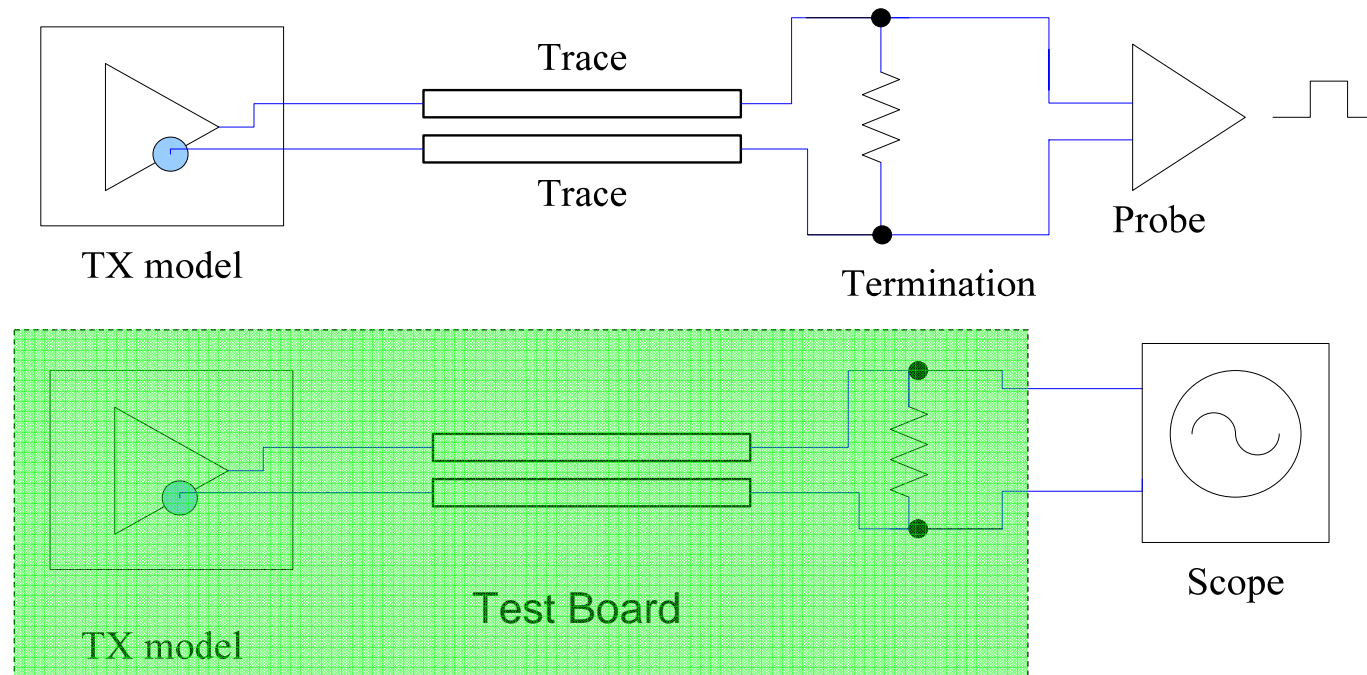


Passive interconnects modeling

# Modeling and its Correlation Flow



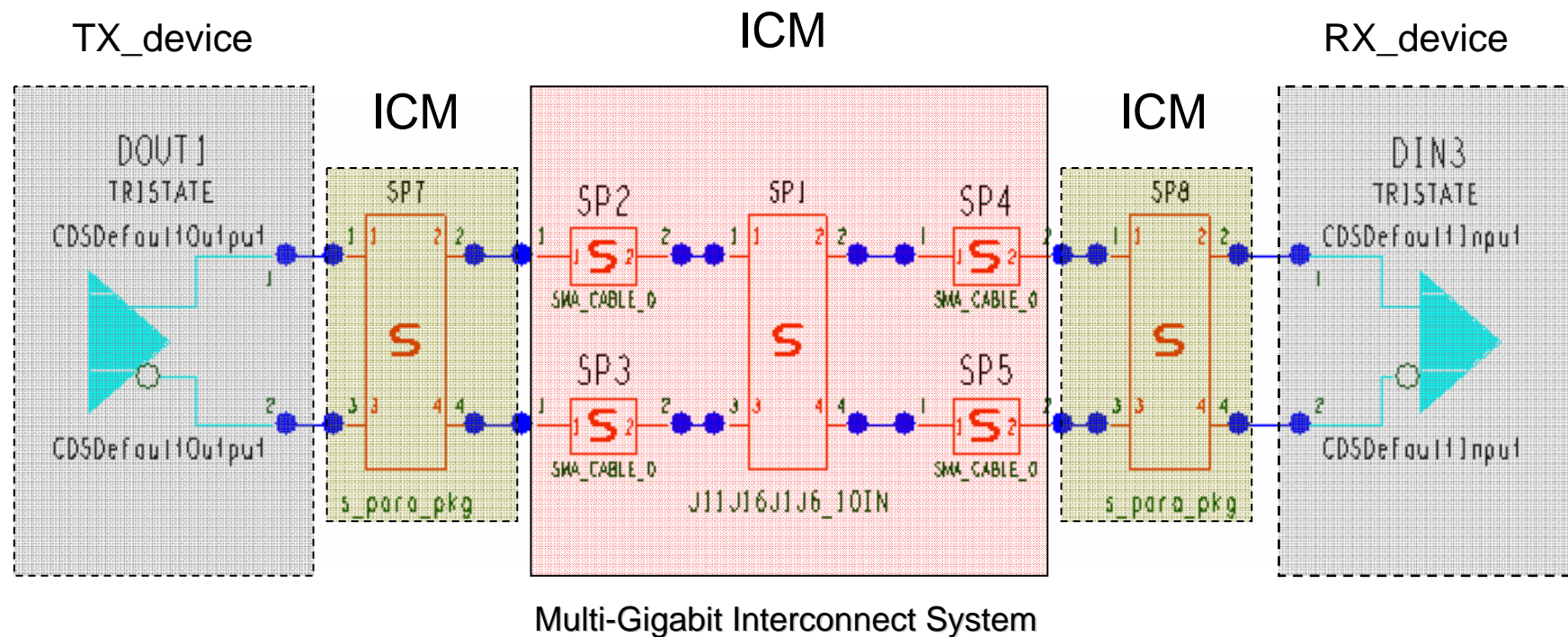
# Model Validation Setup



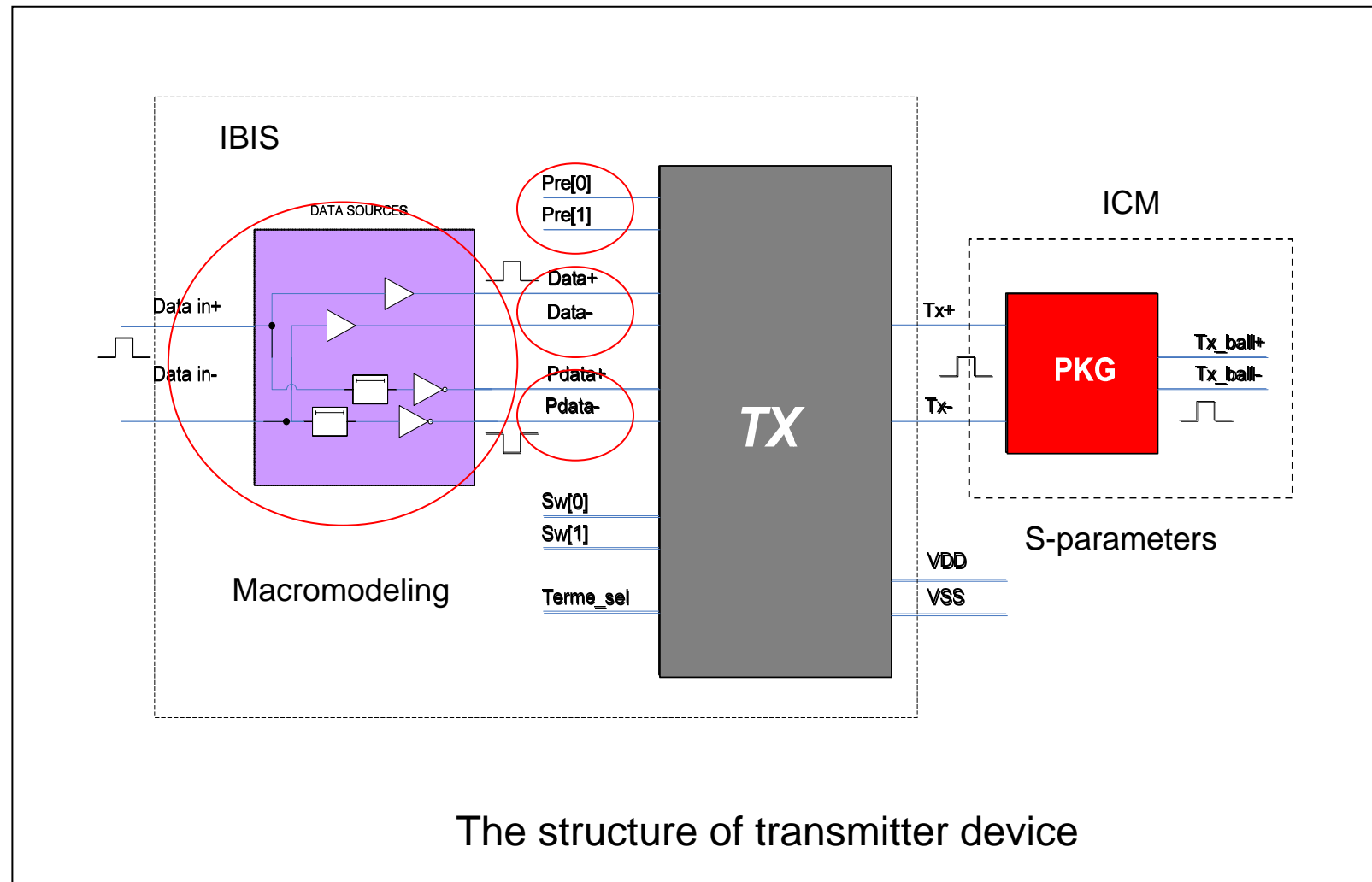
Correlations with lab measurements and HSPICE simulations

# Behavioral-level Interconnect Modeling

- Transceiver Buffer Modeling
- Transceiver Package Modeling
- Interconnect (Traces, Vias, Connectors) Modeling
- Lab Correlation

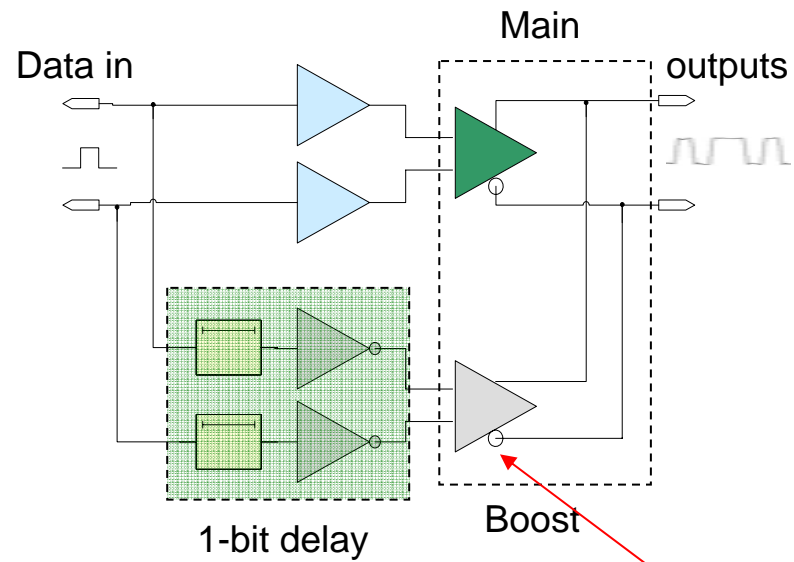


# Behavioral-level Modeling of SERDES

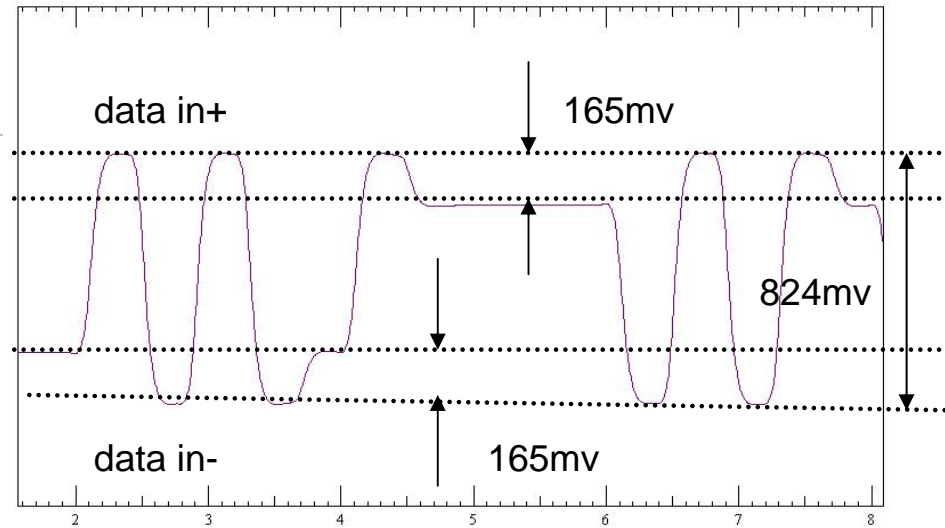




# Pre-emphasis



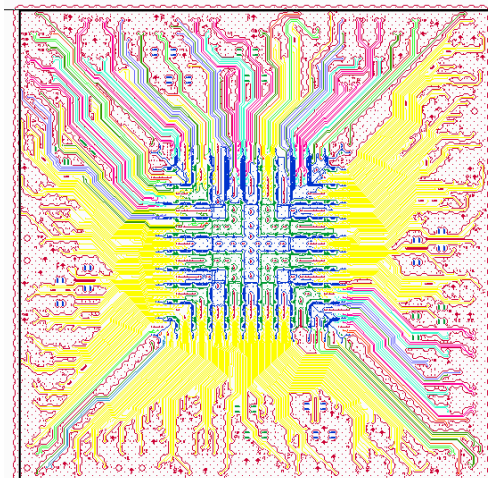
Pre-emphasis output



UI=400ps Scale=824mv Eqdb=165mv

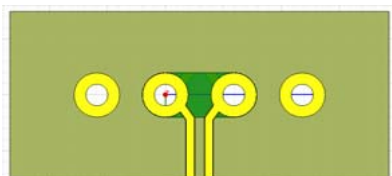
# Package Modeling using S-parameters

```
("../../../../Pkg_models/s_para_pkg.dml"  
(PackagedDevice  
  (s_para_pkg  
    (ESpice ".subckt s_para_pkg 1 2 3 4  
Xs_para_pkg_4Port 1 3 2 4  
  
.subckt s_para_pkg_4Port_Data 1 2 3 4  
S1 1 2 3 4 algorithm=default  
DATAPOINTS SPARAM  
R=50.000000  
DATAUNIT=HZ  
FREQUENCY=0.000000e+000  
  
. END SPARAM  
.ends s_para_pkg_4Port_Data  
.ends s_para_pkg_4Port" )  
  (PinConnections  
  
    (NumberOfPorts 4 )  
    (SubType SPARAM ) ) )  
(LibraryVersion 136.2 ) )
```

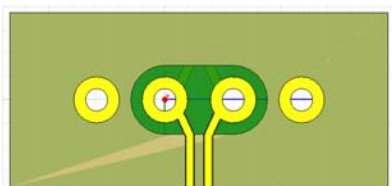


S-parameters can be added to Cadence DML file.

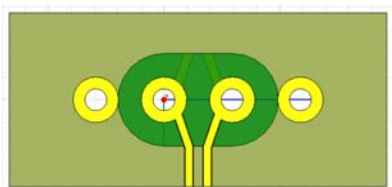
# Vias Modeling and Optimization



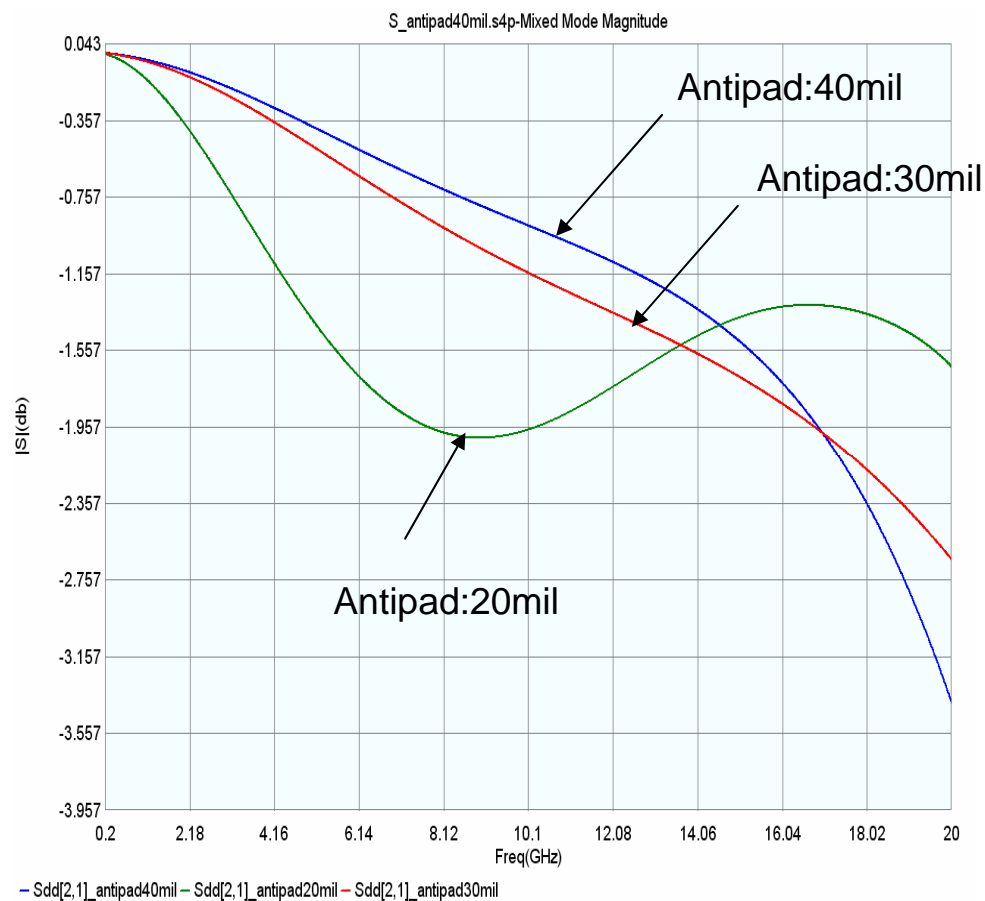
Antipad:20mil



Antipad:30mil

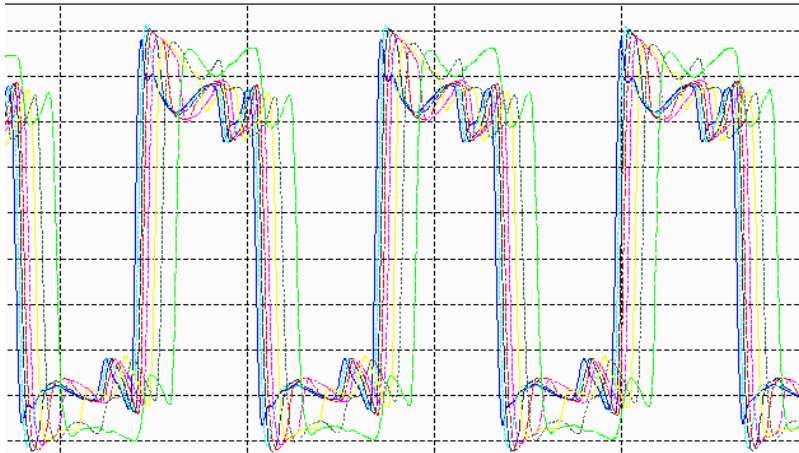
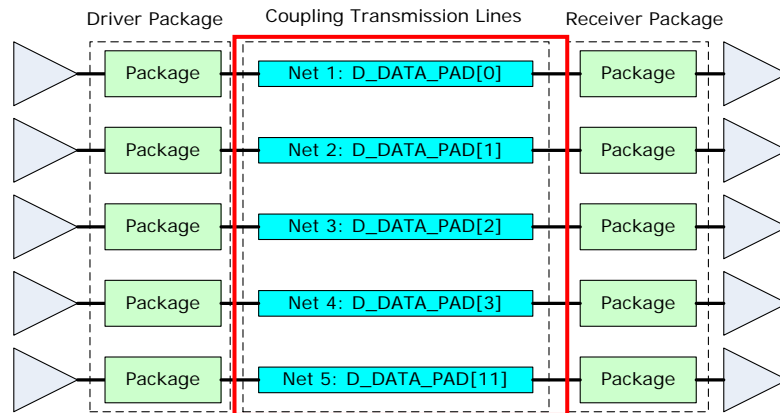


Antipad:40mil



# Traces Modeling and Optimization

## ■ Extracting S-parameters using 2D/3D EM field solver



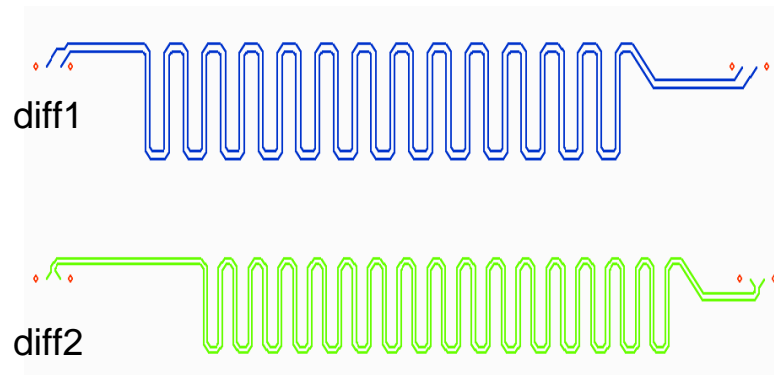
```
.alter change transmission line length = 38.1mm
.param len=38.1mm
.alter change transmission line length = 50.8mm
.param len=50.8mm
.alter change transmission line length = 62.5mm
.param len=62.5mm
.alter change transmission line length = 76.2mm
.param len=76.2mm
.alter change transmission line length = 88.9mm
.param len=88.9mm
.alter change transmission line length = 101.6mm
.param len=101.6mm
.alter change transmission line length = 127mm
.param len=127mm
```

```
.param lo=0v
.param hi=1.32v
.param dl=1ns
.param tr=30ps
.param ui=25.72ns
```

```
VA a 0 pulse 0 hi dl tr tr 'ui/2-tr' ui
```

Time domain simulation and optimization using S-parameters.

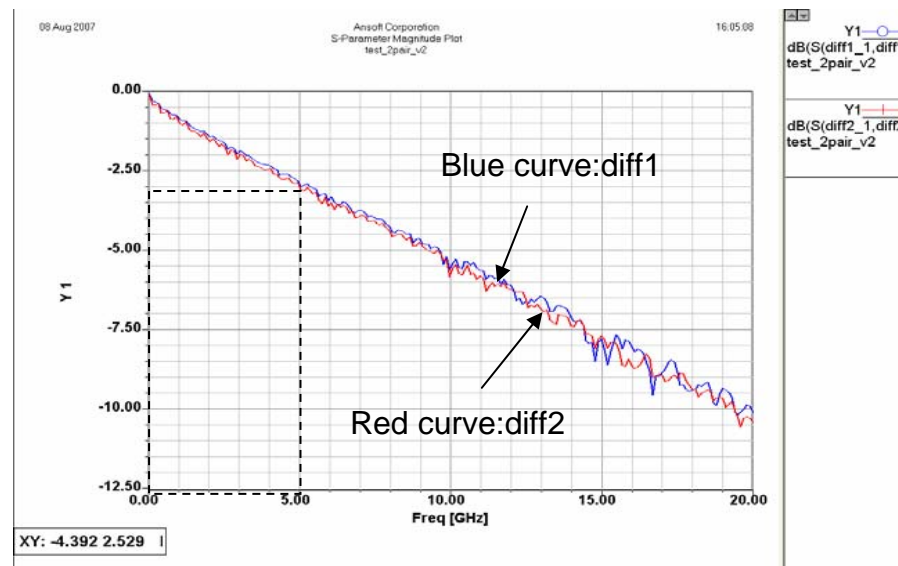
# Traces Modeling and Optimization



Trace width : 10mil

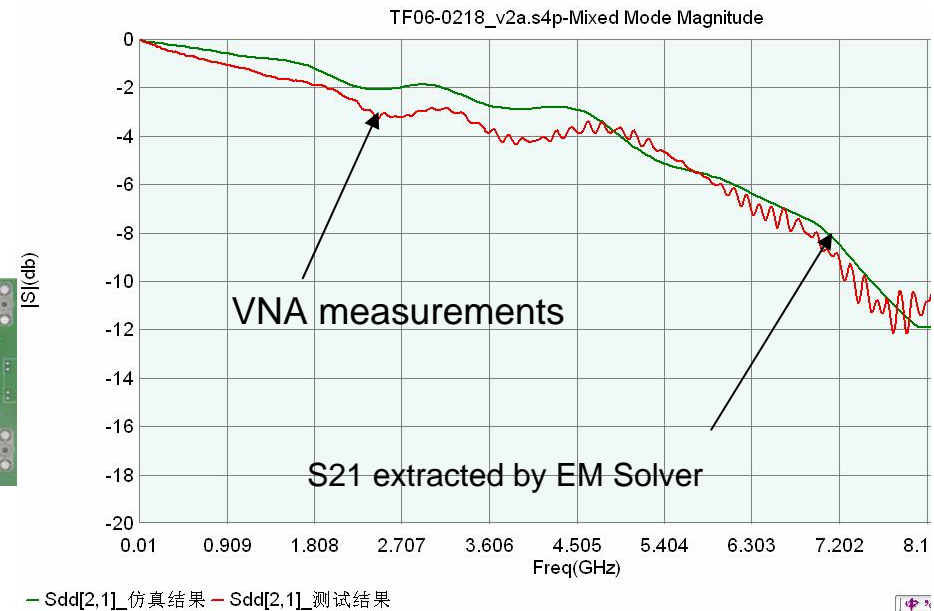
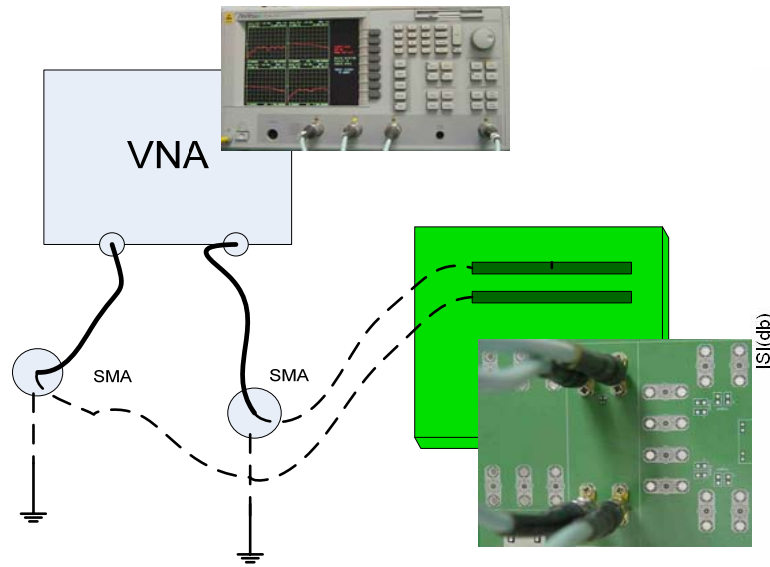
Trace width : 8mil

→	01TOP 0.5oz+plating
14mil	→ 02G01P 1oz
CORE 14mil	→ 03IS01 1oz
14mil	→ 04G02P 1oz
CORE 14mil	→ 05IS02 1oz
14mil	→ 06BOTTOM 0.5oz+plating



# Lab Correlation for S-parameters

## ■ Correlation based on VNA measurements



# Lab Correlation for Macromodels

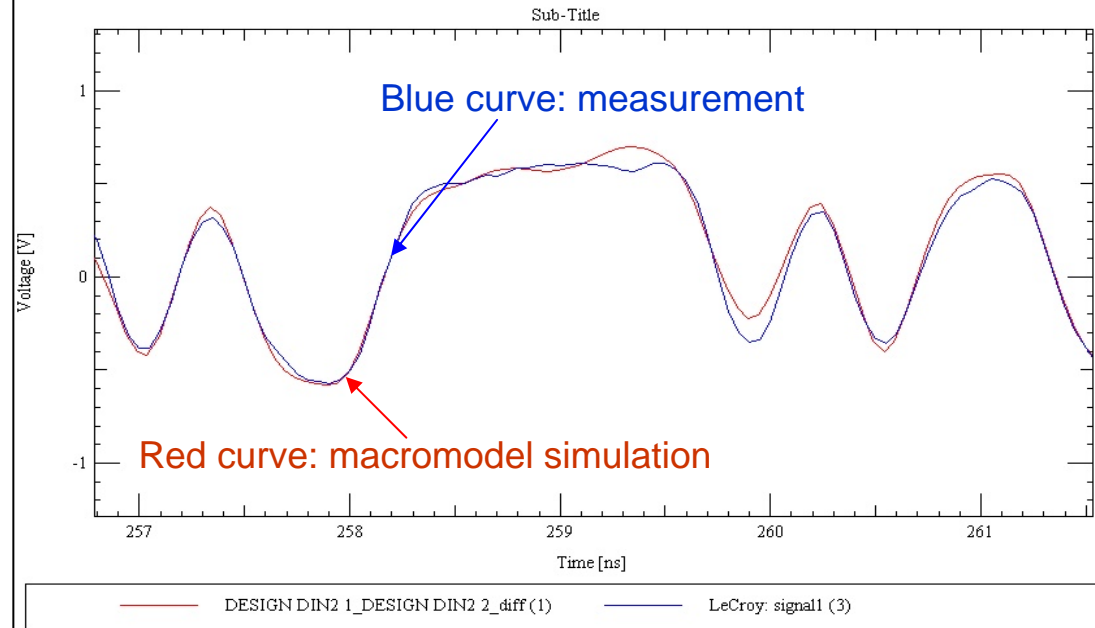
\* This is the top-level subcircuit for this MacroModel.  
\* It MUST have the same name as the IOCell, or it will not work.

```
.subckt Tx nvdd outp ngnd in en pcl gcl  
outn BUFF=BUFF ibis_file=ibis_models.inc  
+ bitp=400p  
+ inv0=0  
+ inv1=1  
+ scale=1  
+ eqdb=-0.5  
+ cf0=1  
+ rt=50
```

\* Some parameters are derived for use in the MacroModel.

```
.param adj='eqdb*0.58'  
.param eqf='1.0 - (10.0 ^ (adj/20.0))'  
.param cf1='cf0 * eqf'
```

For behavior-level modeling,  
correlation is necessary.



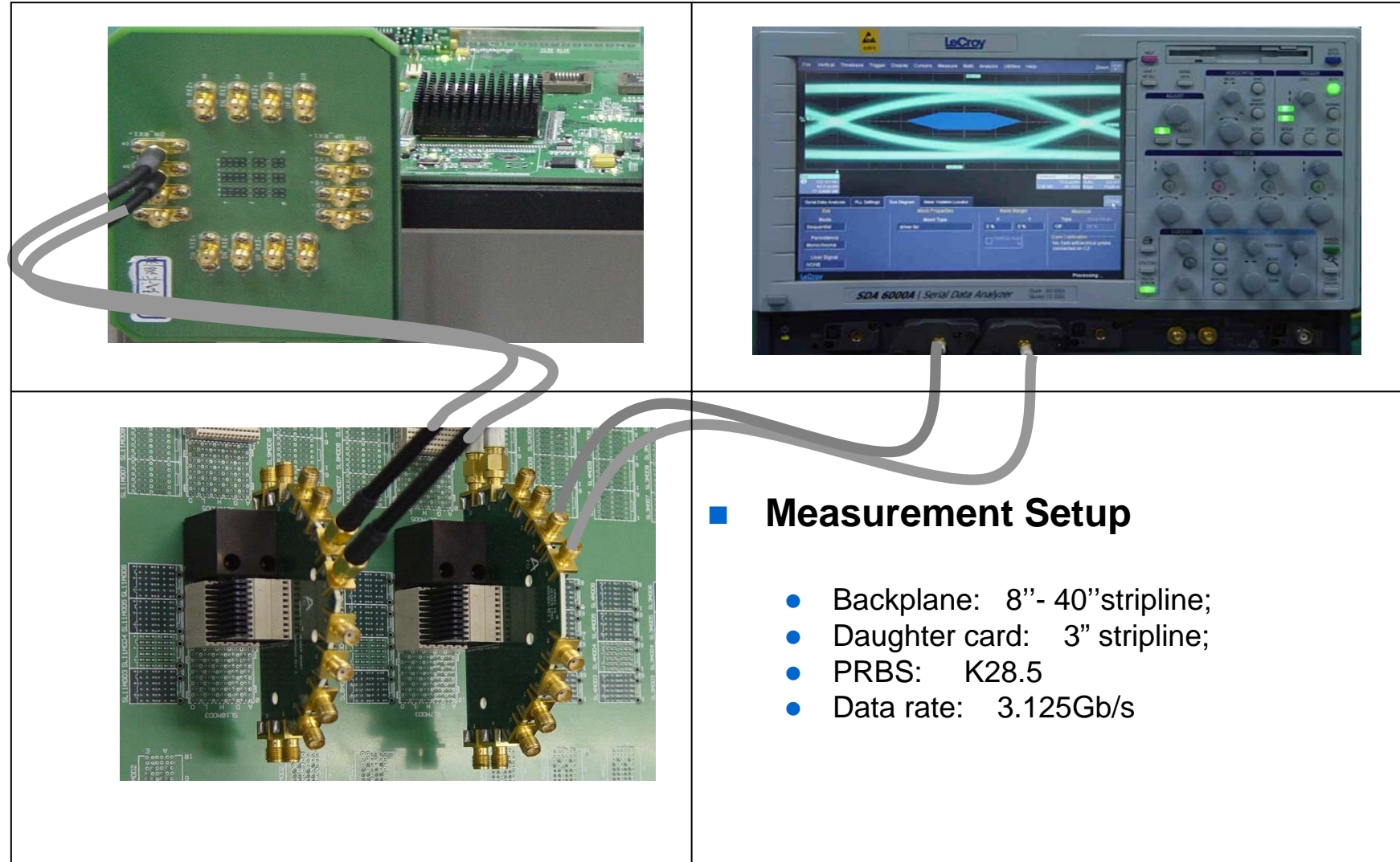
10% Pre-emphasis

## Lab Correlation Steps:

1. Simulation using HSPICE models
2. Simulation using macromodels
3. Correlate with laboratory measurement

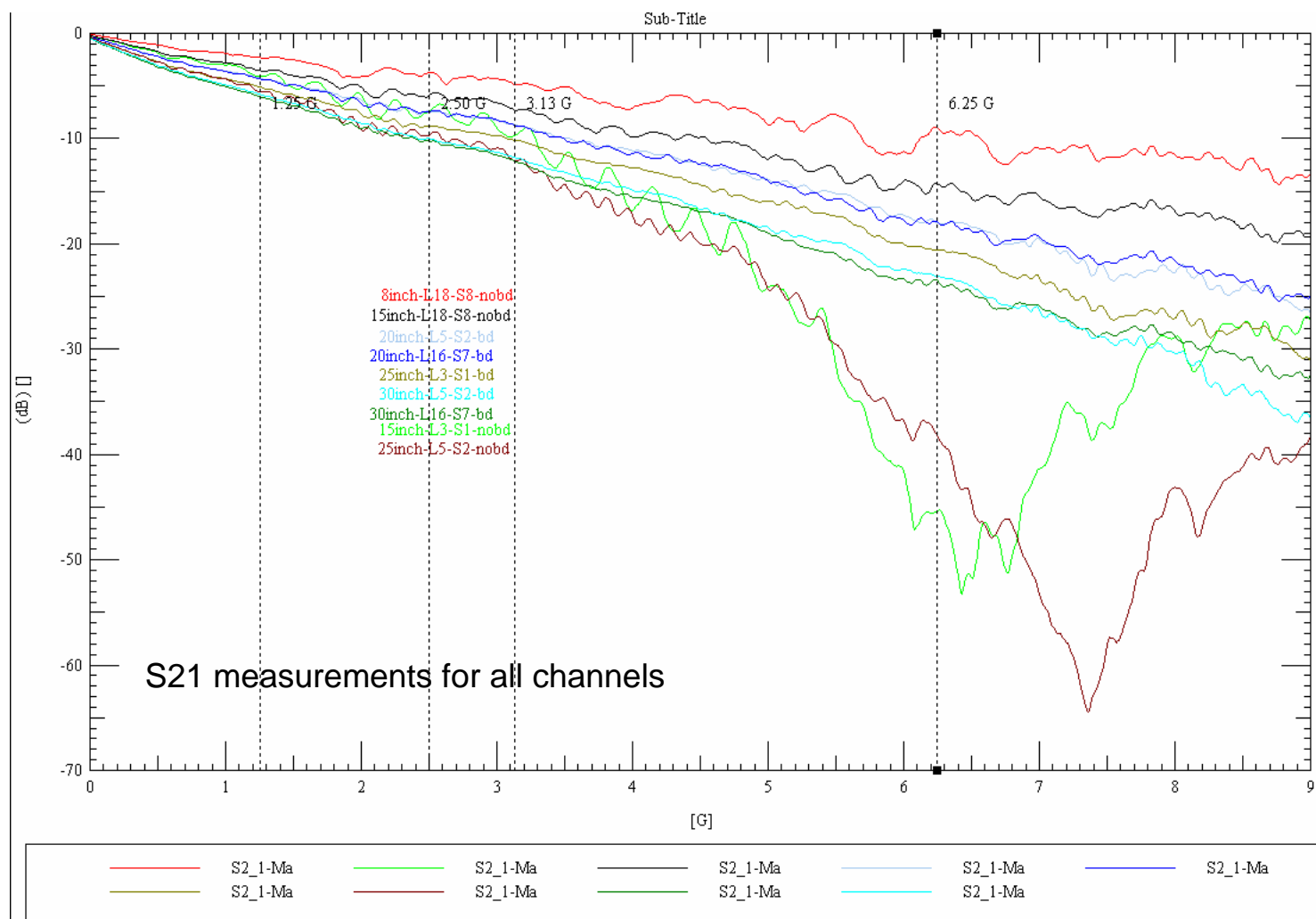


# Lab Correlation and Multi-gigabit System Measurement

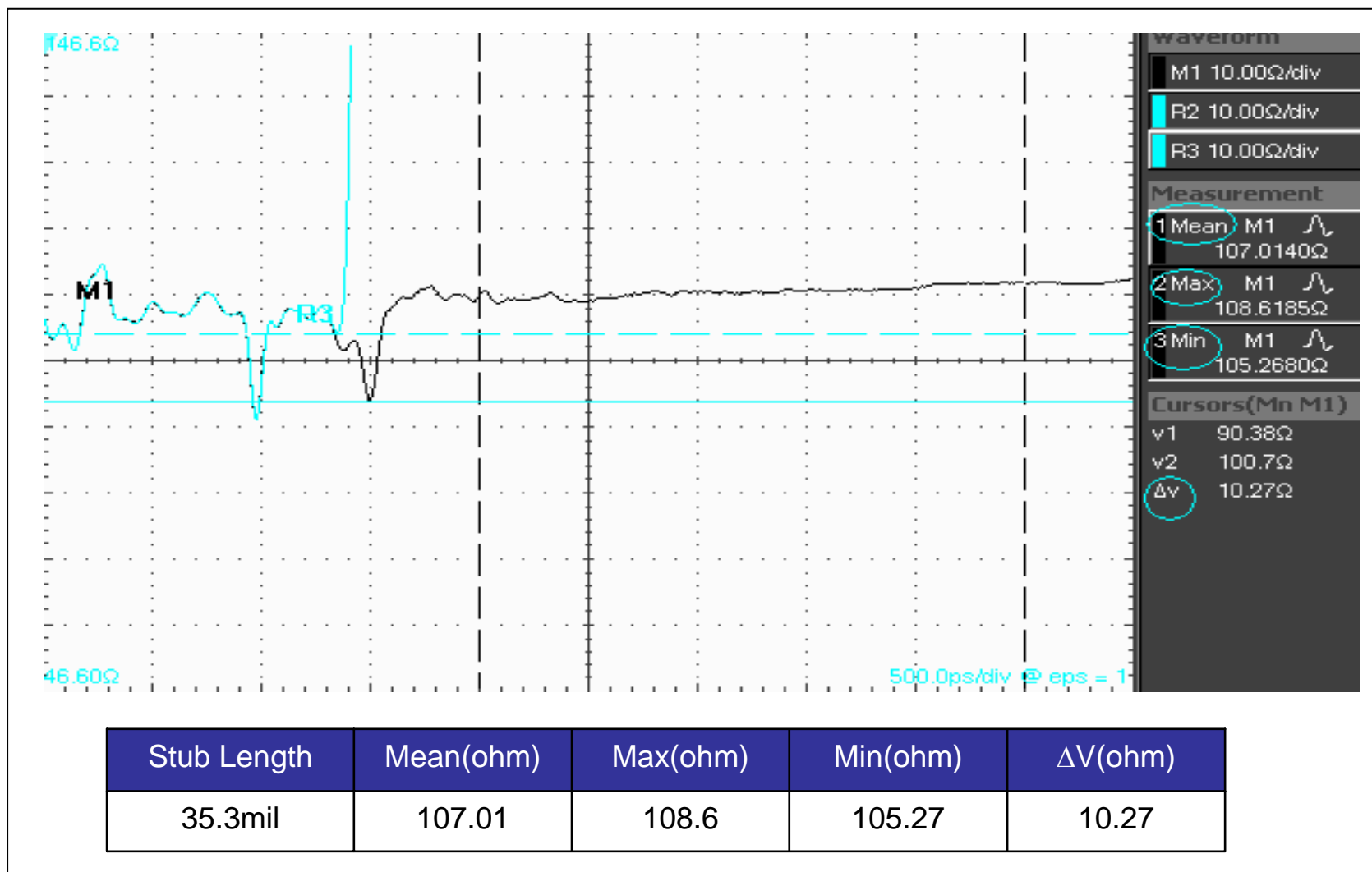




# S-parameters Measurement for Channels

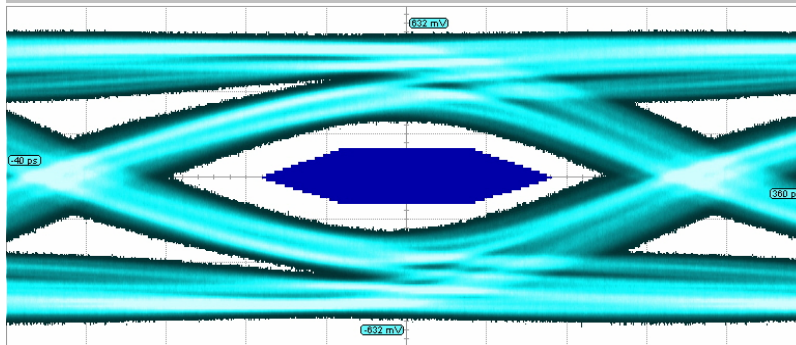


# TDR Measurement

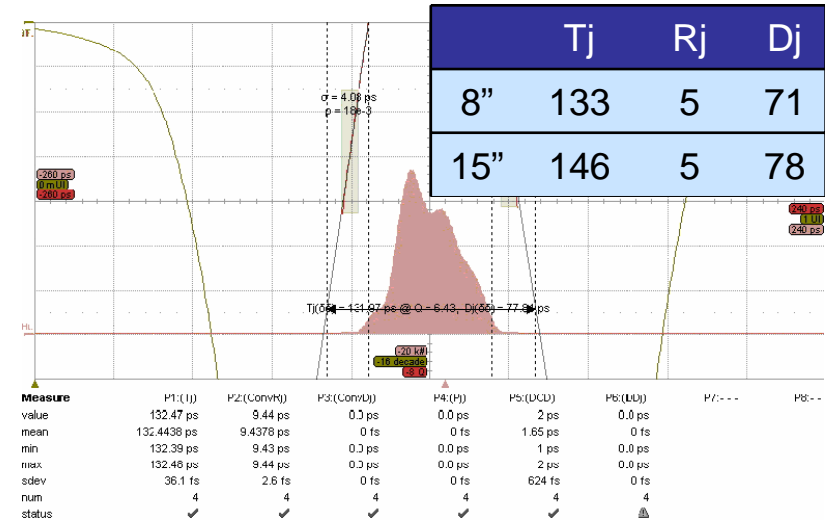


# Eye Diagram Analysis and Design Margin Budget

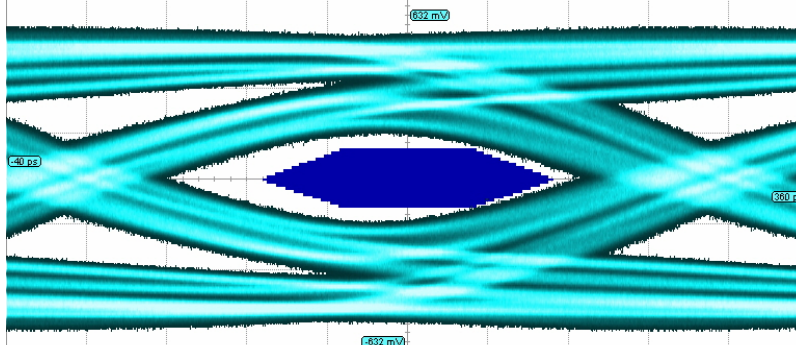
8" stripline Stub=34mil



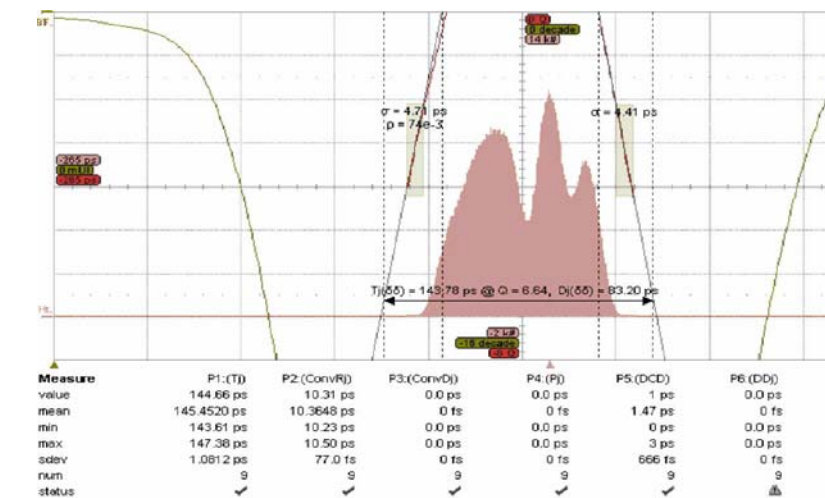
No pre-emphasis



15" stripline Stub=34mil



No pre-emphasis



## Conclusions

- For Multi-gigabit channel optimization, it is a good practice to use macromodels for active devices and EM solver derived S parameter models for passive elements, provided the behavioral models have been correlated by lab measurement.
- Measurement correlated MacroModel enables much shorter simulation time than transistor-level spice model for pre-emphasis simulation and fine tuning.
- S-parameter is an accurate and efficient way for interconnect modeling. They can be used with confidence after being generated from EM solver and correlated with VNA measurement.

# Thanks

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