Issues Combining Buffer and Interconnect Model Formats

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Agenda

- The System Viewpoint
- Buffer Model Formats
- Package and Interconnect Model Formats
- Combining Components into a System
  - Summary of Today's Industry Options
- Steps Toward a Unified Solution

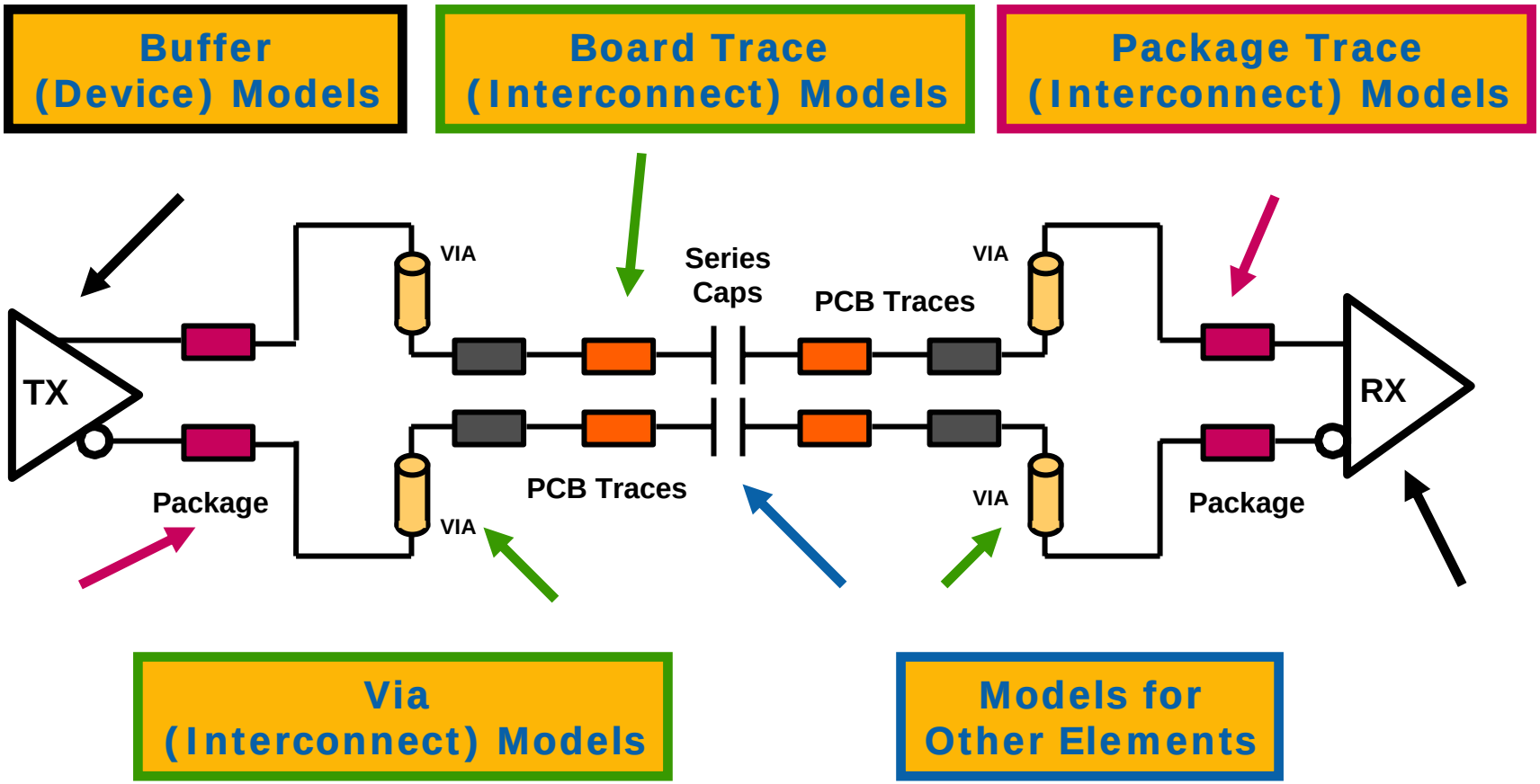
The Number of Model Formats is Increasing!

- IC designers can model buffers in many ways
  - Proprietary SPICEs (transistor or behavioral)
  - Traditional IBIS (3.2/4.0): table-based
  - Verilog-A (for analog-only simulation)
  - Verilog-AMS/VHDL-AMS (for mixed-signal)
  - Multi-lingual IBIS 4.1/4.2 (IBIS+*-AMS, IBIS+Verilog-A, IBIS+SPICE)
- There are just as many ways to model packages & interconnects
  - Proprietary SPICEs (lumped-element, RLGC)
  - Traditional IBIS (3.2/4.0) for packages
  - S-parameters (Touchstone*, CITI*)
  - ICM (RLGC or Touchstone*)
- … and many ways to combine these models in a system
  - Both system and IC vendors simulate system designs
  - System sims involve all of the above plus other components

How well do all these options work together?

SI Models - The System View

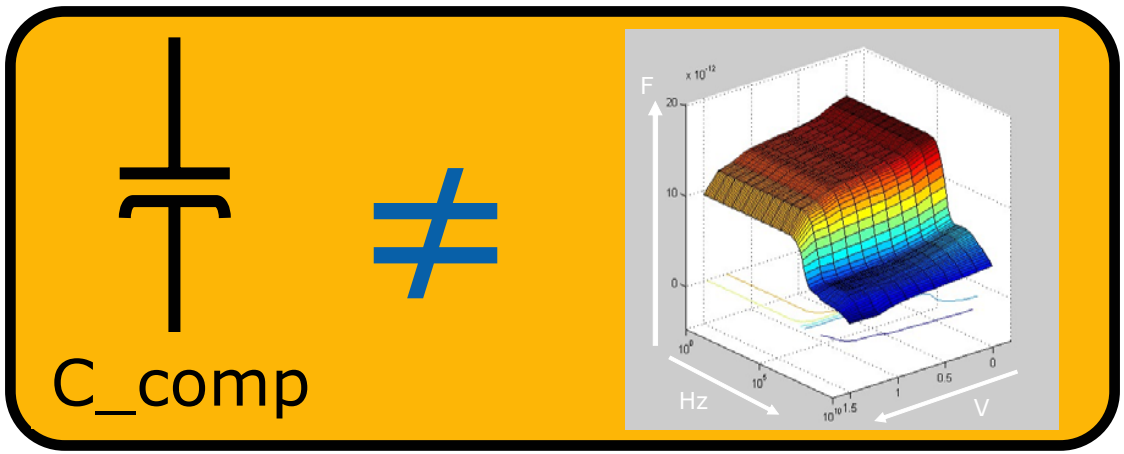
SerDes Example



… plus the language or format that connects them all

Buffer Models

- "Traditional" table-based IBIS 3.2/4.0 has some advantages
  - Standard and enjoys widespread support
  - Fast (behavioral) and protects IP
  - Supports integration with layout (pin and signal information)
  - Free syntax checking (IBIS Golden Parser)
  - Reasonably simple to learn
- Format has increasing issues



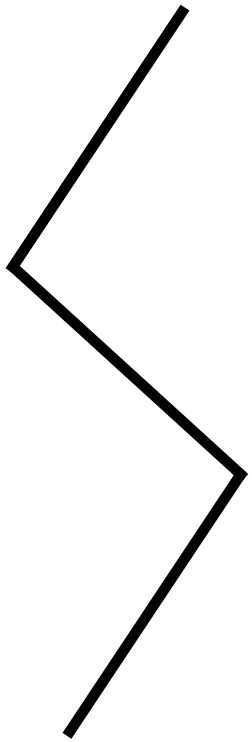
  - Best for single-ended, time-domain design
  - Frequency-domain support is weak (e.g., C_comp as buffer capacitance)
  - Also weak for SerDes: equalization, frequency-dependence, jitter

"SPICE" vs. "AMS" vs. Algorithmic Models

- Several options exist to improve buffer model support

SPICE

- Can be used behaviorally
- Familiar to most engineers
- Versions implemented in most EDA tools
- Not standard
- A format, not a language
- Analog-only
- Not suited to algorithmic modeling
- Still data-driven



"AMS"

- VHDL-AMS, Verilog-AMS
- Mixed-signal (digital + analog)
- Also Verilog-A (analog-only)
- Industry standard
- Languages, not just formats
- More familiar to IC designers than SI/system designers
- Expensive to implement for lower-cost EDA tools
- Languages are not easily cross-ported
- HDLs, not general purpose mathematical languages

IBIS 4.2 supports Verilog-AMS, VHDL-AMS, Verilog-A and (Berkeley) SPICE;
IBIS-ATM working on SerDes algorithmic models

Package modeling through IBIS 4.2

- [Package] keyword
  - Required for each component
  - Contains corner values for R_pkg, L_pkg and C_pkg

- [Pin] keyword
  - Each pin can have a distinct R_pin, L_pin or C_pin value
  - Only a single value can be used (no corners)

- [Package Model] keyword (also Electrical Board Description)
  - Can reference an external file or data within the same .IBS file
  - Two methods available currently in IBIS
    - *Coupled, single-matrix RLC description (full, banded, and sparse matrix formats available)*
    - *Uncoupled multi-section description using RLC, length*

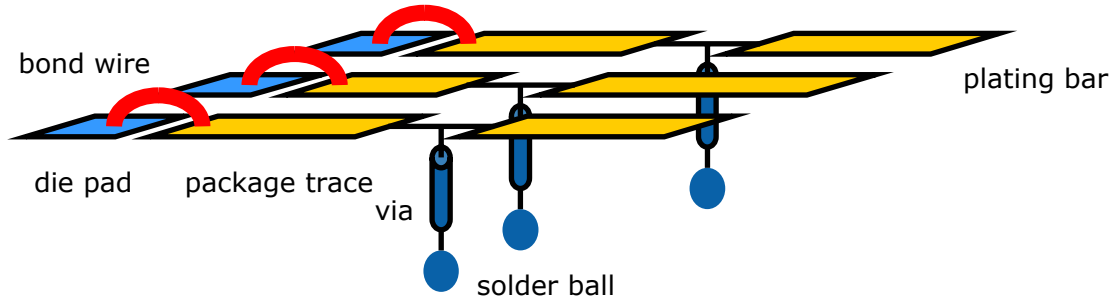
No coupling for multi-section packages, no AC loss

Not suitable for today's fastest designs!

BGA Package Structure

Drawing courtesy A. Muranyi

- A typical application



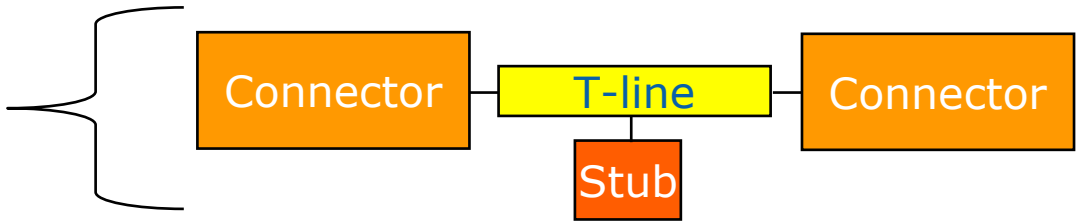
- BGA (Ball Grid Array) Package structure
  - **Bond wire (usually gold): connects die pad to traces**
  - **Package trace: lossy routing path in package FR4**
  - **Via: connects trace to solder ball**
  - **Solder ball: attach point for device to PCB**
  - **Plating par: lossy stub left from separation of packages**

Can we describe this today
using EBD, IBIS or PKG?
Not with adequate loss and coupling.

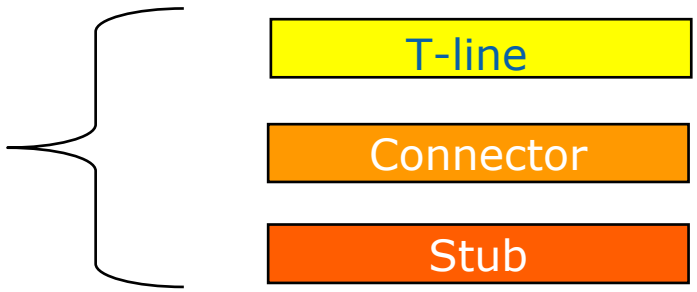
SPICE and ICM

- Many vendors use SPICE to address IBIS package shortcomings
  - Most SPICEs support lumped or distributed RLGC
  - Proprietary! One model set may not work across multiple tools
- ICM (IBIS Interconnect Modeling specification) available but new
  - Standard, with industry support picking up
  - A separate specification – no direct connection to IBIS yet
  - Not intended to support series components (e.g., series capacitance)

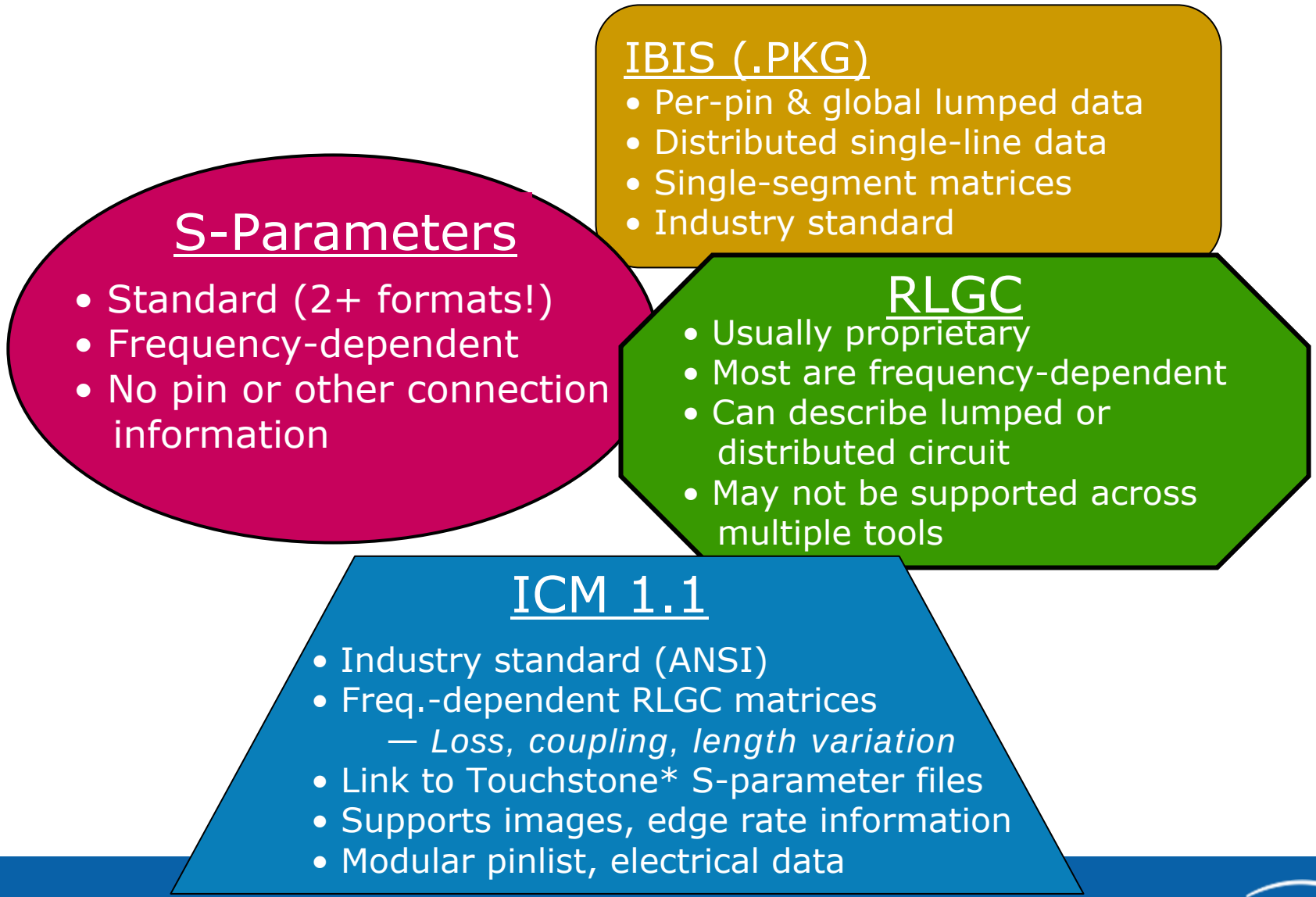
Described by
[Begin ICM Model]
…
(path description)
…
[End ICM Model]



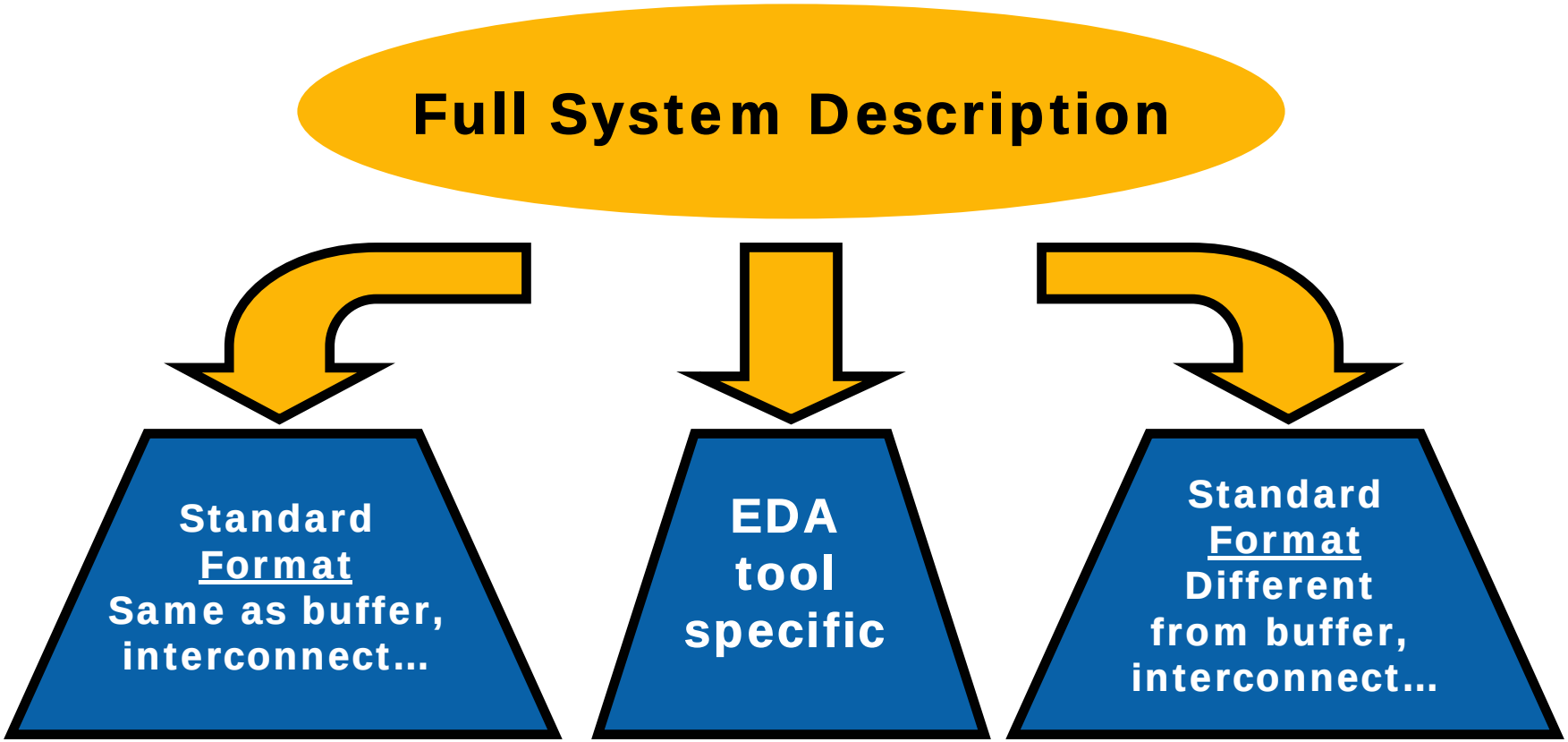
Described by
[Begin ICM Section]
…
(RLGC or S-params)
…
[End ICM Section]



Package & Interconnect Formats



Combining Models – A Dilemma



Can one format support all elements of the system?

Do you create a new description for each tool? How many tools?

How many formats do you have to learn? How many do your tools support?

SPICE as a Topology Format

- Some IC vendors want to provide complete system "decks"
- Using proprietary SPICEs is popular, but faces several issues
  - Inconsistency in format
    - *SPICE is not standard! Elements and features vary across SPICEs*
    - *Some analysis functions are proprietary (e.g., S-parameters)*
  - Lack of expandability
    - *Users cannot define new elements or analyses, only new subcircuits*
  - Inconsistency in results
    - *With different engines, the same model can give different results*
  - Integration with layout is not automatic

All are barriers to using SPICE
to represent systems across tools

Models in Combination

Model Type	Buffer	Interconnect (Board, Package, etc.)	"System Assembly"
Behavioral SPICE	Which SPICE? Frequency-dependent interconnect? Features compatible across several tools?		
Traditional IBIS	Weak C_comp, no core-side information…	No distributed, frequency-dependent interconnect	☒ not intended
IBIS 4.2 + Berkeley SPICE	✓	No distributed, frequency-dependent interconnect	☒ not intended
IBIS 4.2 + *-AMS	✓	Need custom transmission line libraries	☒ not intended
ICM 1.1	☒ not intended	✓	No active models, limited series components
Verilog-A	✓	Need custom transmission line libraries	✓

Steps Toward a Unified Solution

- Options exist for a unified buffer+interconnect+system format
  - e.g., Verilog-A can be treated as a SPICE-like standard analog language
  - Standard transmission line libraries would be required to support interconnects under Verilog-A
- The IBIS Open Forum is addressing several of these issues
  - IBIS-ATM is adding algorithmic model support for SerDes
  - IBIS-ICM links are being developed for a future version of IBIS
  - A standard SPICE superset syntax has been proposed
    - *"The 3S Proposal" – http://www.eda.org/ibis/summits/feb07/mirmak.pdf*
- Market forces will determine the most popular combination
  - e.g., IBIS 4.2 + ICM 1.1 + Verilog-A might be possible, but it might not be least expensive or easiest to learn

Make your preferences known!