Serial Link Analysis and PLL Model

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Agenda

High-speed serial link simulation

- Current simulation method overview
- Simulation with AMI model

PLL model

- Jitter introduced by PLL
- Jitter simulation with PLL model

High-speed Serial Link Simulation

- Simulation purpose:
  - ✓Evaluating bit error rate performance of high-speed serial link.
  - ✓Checking whether the bit error rate of link could meet the specification of standard or requirements of product.

- More factors considered in simulation, more accurate the simulation is.

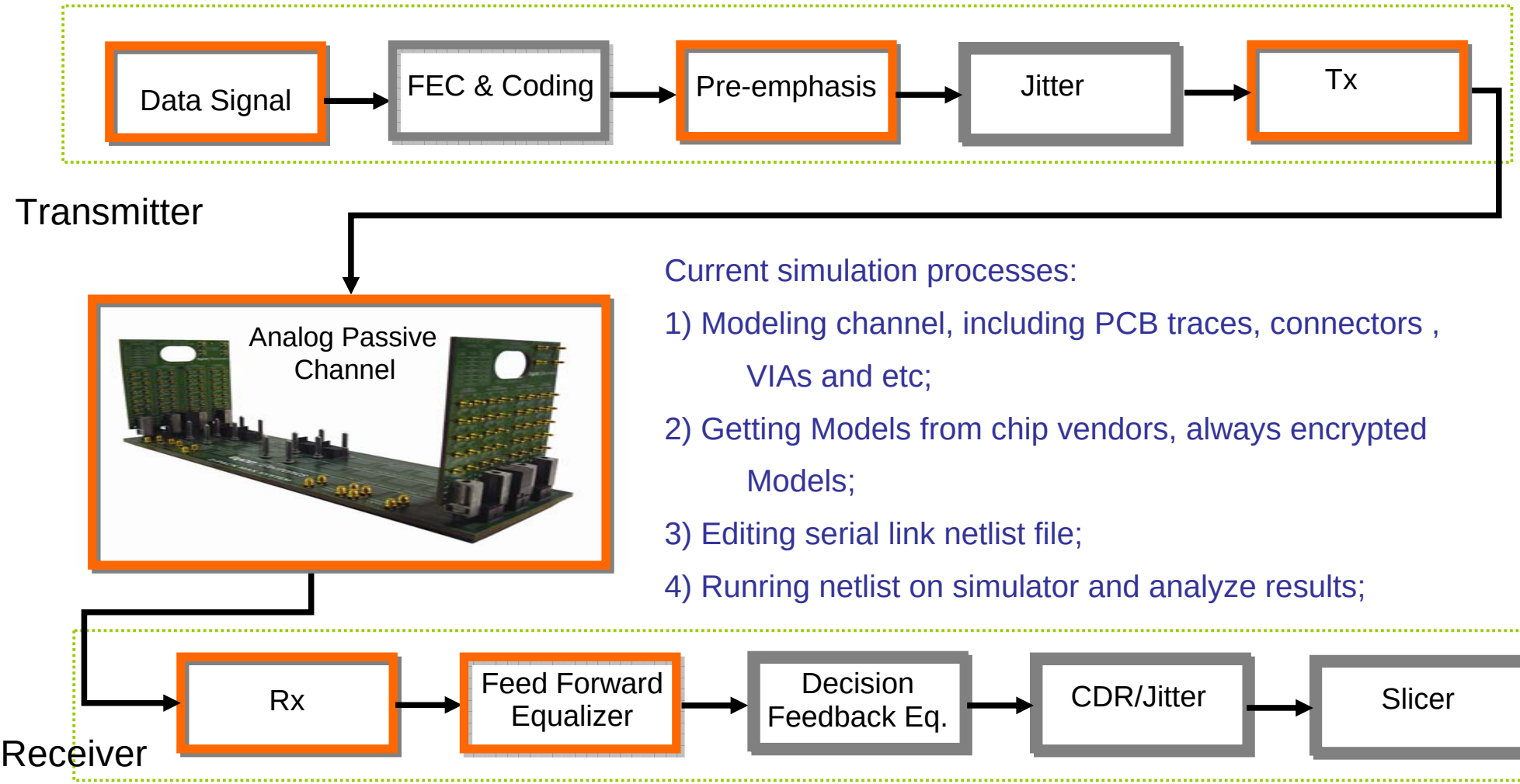
- Due to problems of model availability, simulation technology ability and limited analysis time, it's difficult, if not impossible, for SI engineers to consider all factors in system simulation.

- Serial link simulation technologies lag behind serial link development.
  SI engineers are struggling with models in hand to get reliable results.

Current Simulation Method Overview

- Simulation with encrypted model is mostly used method.

  Dark block is normally not supported by current simulation method.



Current simulation processes:

1) Modeling channel, including PCB traces, connectors , VIAs and etc;
2) Getting Models from chip vendors, always encrypted Models;
3) Editing serial link netlist file;
4) Runring netlist on simulator and analyze results;

Simulation Example

- Current simulation method with encrypted model is extremely difficult to modulate jitter on serial data or statistically post-process waveform.
- Encrypted model simulation is a time-consuming work.

Here is a very simple sample netlist for 2.5Gbps high-speed serial data.

40 minute simulation time to get only 132 bit results!

Add Jitter?

```
*********************************************************************************
* driver model
*********************************************************************************
*        CA0=A0  CA1=A1  CA2=A2  CA3=A3    AC_DC    AV25     CB0=B0  CB1=B1   CB2=B2  CB3=B3
XDRIVER1 DRV1GND DRV1GND DRV1VDD DRV1VDD  DRV1VDD  DRVAV25   DRV1GND DRV1GND  DRV1GND  DRV1GND
* CLK_N    CLK_P      D0       D1             OUT       OUTN
+ CLK_1N   CLK_1P data_a  data_b      DRV1OUTP  DRV1OUTN
*   PWR0    PWR1    PWR2          TERM_75_IN  VBGAP    VDD     VSS     AVTT    ZDI
+ DRV1VDD DRV1VDD DRV1VDD         DRV1GND    DRVBG    DRV1VDD DRV1GND  DRV1VTT  ZDI1 ULF4S8ADV1TX

*********************************************************************************
* Channel Model, simple RLGC model used here
*********************************************************************************
W1 drv1outp drv1outn gnd drv1inp1 drv1inn1 gnd n=2 rlgcfile=diff100_5_5.rlgc l=1000mil

*********************************************************************************
* Receiver model, 50ohm Termination resistance used here
*********************************************************************************
rterm1 drv1inp1 DRV1VTT 50
rterm2 drv1inn1 DRV1VTT 50

 .TRAN  35ps  52.8ns
```

Table 37. System Jitter Numbers for 2.125 Gbps Operation (Worst Case)

Core Function	Deterministic Jitter DJ ps, p-p	Random Jitter RJ (1-Sigma) ps, rms	Total Jitter (1E-12) ps, p-p (at specified BER)
Transmitter Jitter Output	58	3.3	104
Receiver Internal Jitter	44	3.3	120
Receiver Jitter Tolerance	-	-	350

Note: Transmitter output jitter and receiver internal jitter are the same as above when half rate mode is selected (HRATEx = '1').

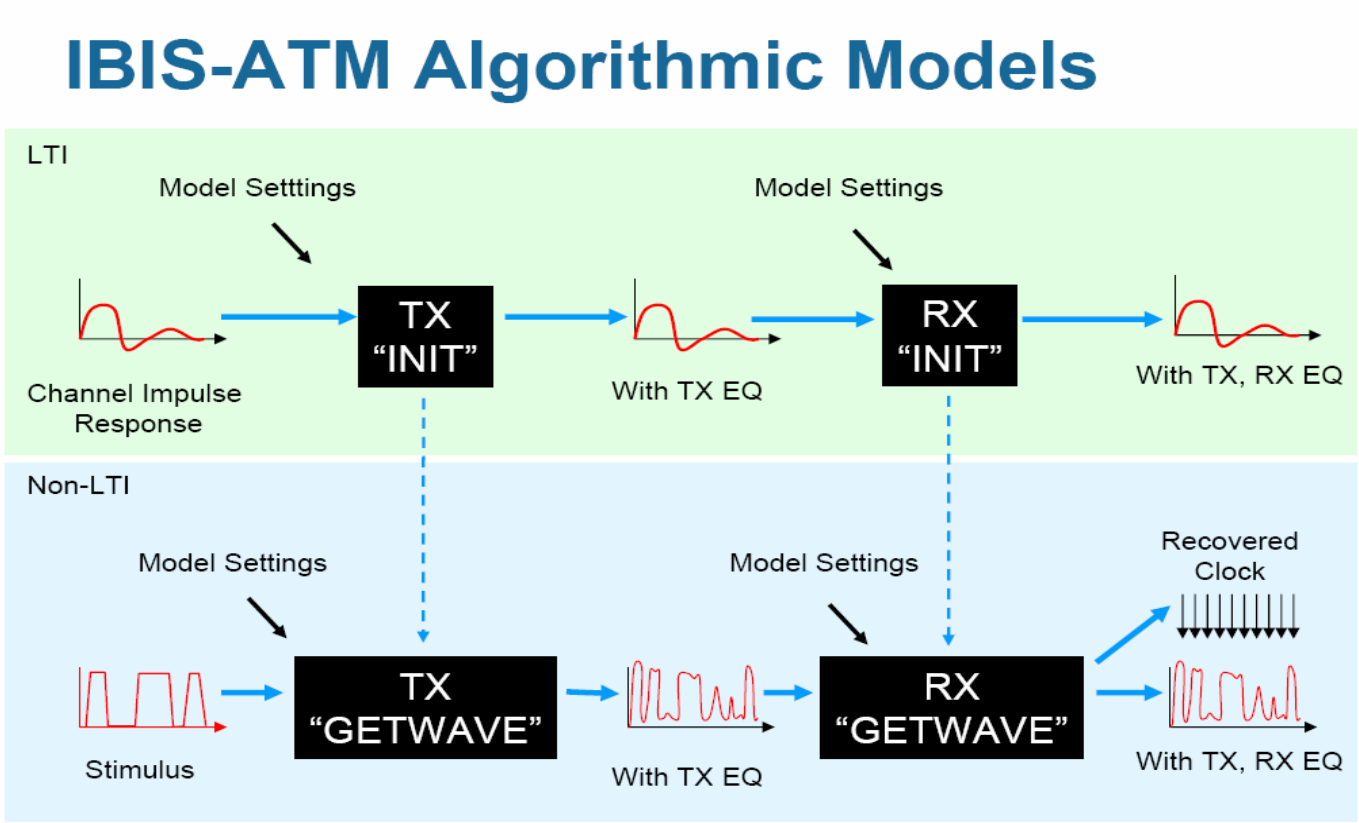
Jitter Parameters

```
total cpu time       2479.65 seconds
job started at  15:22:37  07/20/2007
job ended   at  16:04:03  07/20/2007
```

IBIS AMI Model

IBIS-ATM is working at improving simulation technique and proposing Algorithmic Modeling API (AMI) in IBIS.

- Mainly focus on emphasis, equalization and CDR modeling problems.
- LTI model and Non-LTI model



Picture reference from "SerDes Modeling and IBIS" at DAC_2007_IBIS_Summit

Simulation with AMI Model

Some welcoming features of IBIS-AMI :

1) Non-linear component Components, like DFE and CDR could be included in simulation

2) Jitter parameters defined in AMI model, permitting jitter simulation with AMI model.

3) Rx_Receiver_Sensitivity parameter defined in AMI, slicer performance is also included in simulation.

4) Simulation with AMI model will be much faster than simulation with encrypted model. Global equalization optimization becomes possible.

5) In theory, AMI can do the job of modeling new emerging algorithm.

- IBIS AMI model makes a giant step on improving serial link simulation techniques.
- AMI model still needs time to prove itself a successful solution.

Agenda

High-speed serial link simulation

- Current simulation method overview
- Simulation with AMI model

PLL model

- Jitter introduced by PLL
- Jitter simulation with PLL model

Jitter Parameters in AMI model

Jitter parameters in AMI model

1)Tx_Jitter
Tx_Jitter Info Float Gaussian <mean> <sigma>
Tx_Jitter Info Float Dual-Dirac <mean> <mean> <sigma>
Tx_Jitter Info Float DjRj <minDj> <maxDj> <sigma>
Tx_Jitter Info Float Table <time> <probability> <data> <data> EndTable
2)TX_DCD
Tx_DCD Info Float Range <type> <min> <max>
3)Rx_Clock_PDF
Rx_Clock_PDF Info Float Gaussian <mean> <sigma>
Rx_Clock_PDF Info Float Dual-Dirac <mean> <mean> <sigma>
Rx_Clock_PDF Info Float DjRj <minDj> <maxDj> <sigma>
Rx_Clock_PDF Info Float Table <time> <probability> <data> <data> EndTable

Quoted from “AMI_BIRD_DRAFT_1.0”

Jitter parameter of TX and RX may be not enough for analysis.

- **It covers single value DJ, dual-dirac DJ, uniform DJ and user-defined PDF data;**
- **These jitter parameters are used to describe jitters at transmitter and at receiver;**

Shortage of Jitter Parameter Alone

Jitter parameters alone are not enough for serial link analysis

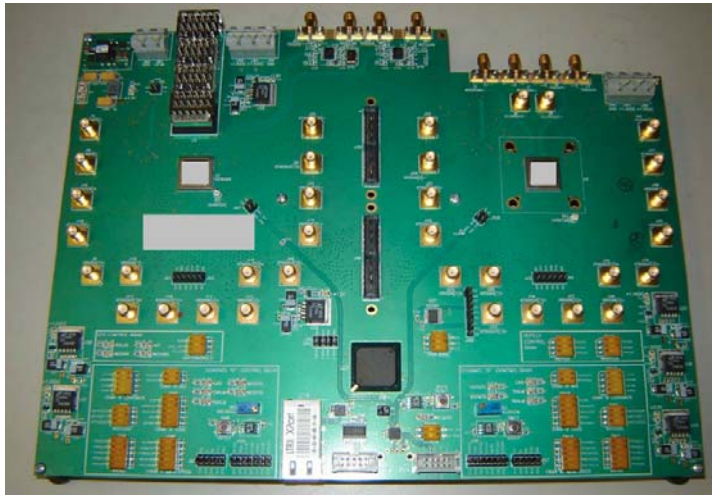
- Jitter parameters in AMI model are mostly measured on evaluation board by chip vendors;
- Omitting differences between evaluation board and product board;
- Jitter is a matter sensitive to environment noise;
- Simulation should carefully consider the jitter introduced by PLL from environment noise;
- Via PLL, environment noise generates a lot of jitter in serial link

  1) Phase noise of reference clock;

  2) Power noise at PLL power pins;
- Especially, power noise is an important contributor to worsen link BER;

Environment Noise Difference

- Working environment of card board is much different from that of evaluation board;
- Power noise is depending on the system design;
- Power on evaluation board is much more clean than that on card board;
- Clock chain on card board may be different from that on evaluation board;



Evaluation board

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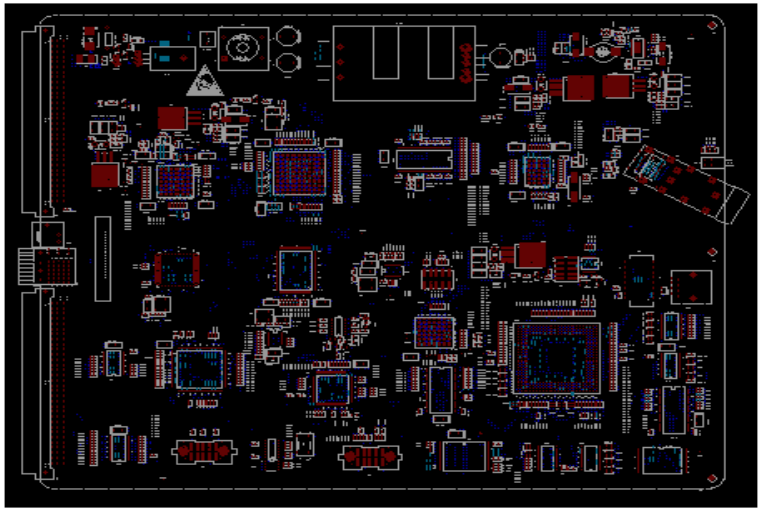


Card board

Jitter Introduced from PLL

At Transmitter

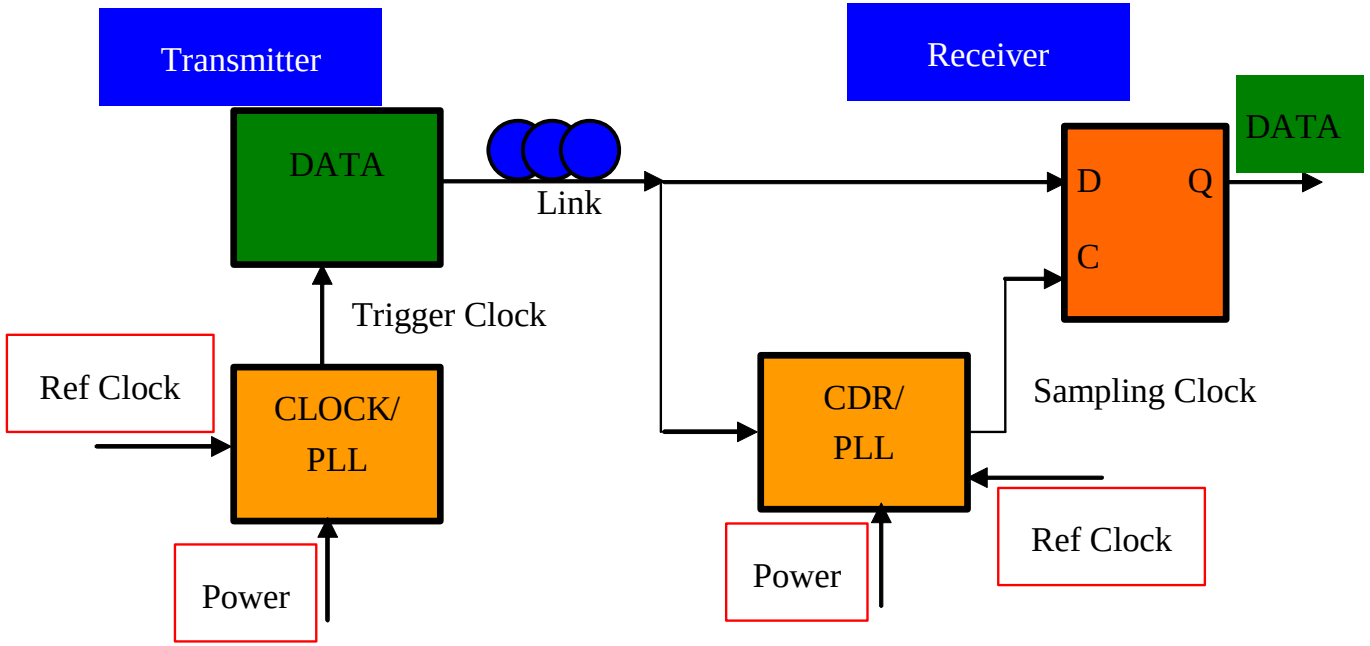
Phase noise of reference clock introduces jitter of trigger clock.

Power noise transfers into output jitter of trigger clock.

At Receiver

Phase noise of reference clock introduces jitter of sampling clock.

Power noise transfers into output jitter of sampling clock.



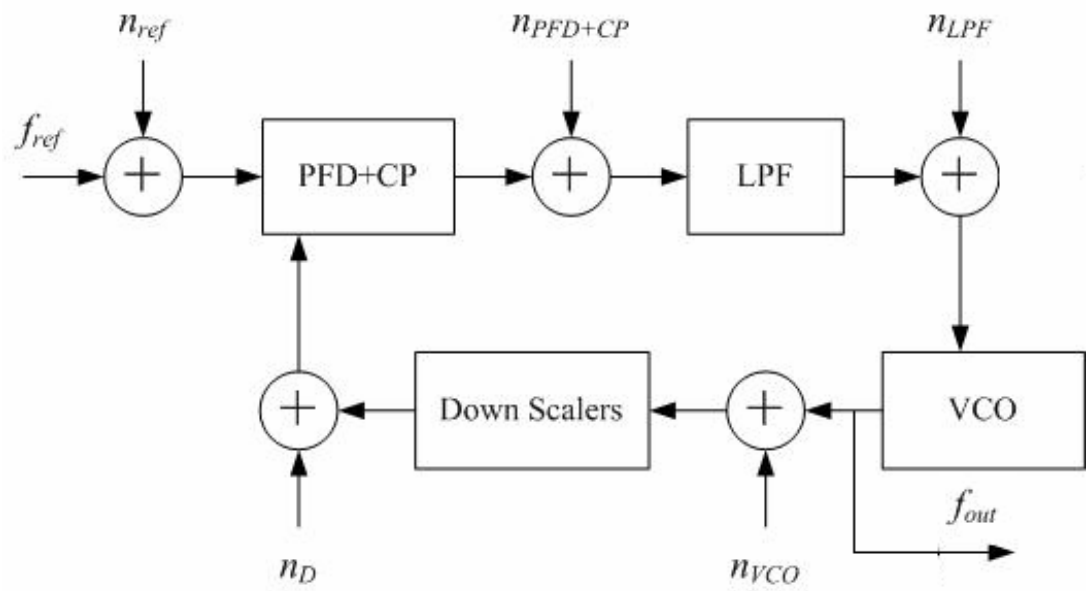
PLL Noise Model

- High-speed serial link contains PLL/DLL at both transmitter and receiver.
- PLL is a phase synchronous system, which is mainly composed of

  1) Phase Detector

  2) Low Pass Filter

  3) VCO



PLL model should include two relations:

- Jitter Transfer Function: relation between input clock jitter and output clock jitter;
- Jitter Sensitivity: relation between power noise and output clock jitter;

Jitter Simulation of PLL Model

PLL model analysis is based on the following assumptions:

- Each noise are statistically independent;
- Jitter introduced by all noises could be expressed as sum of each noise impacting jitter;
- Amplitude of noise and interference is within the linear working area of loop;
- Jitter transfer in PLL behaves like LTI system

Jitter from two noises could be estimated by convolution equation

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$

Here h(t) could be jitter transfer function and could be jitter sensitivity of power supply

Steps of PLL Jitter Analysis

Jitter simulation of PLL model is composed of

1) Getting Jitter Sensitivity and Jitter Transfer relation of PLL;

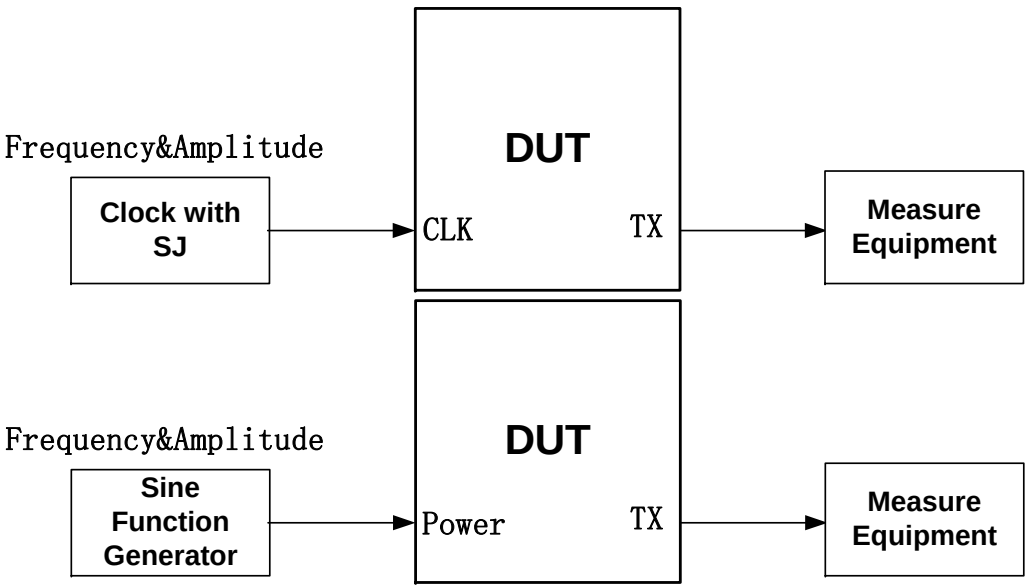
2) Estimating power noise on board;

3) Simulating Reference Clock Jitter;

4) Calculating Jitter introduced from PLL;

1. Getting Jitter Transfer and Jitter Sensitivity

- Modulating jitter at input clock and measuring jitter at output data to get jitter transfer function;
- Injecting noise at power and measuring jitter at output data to get jitter sensitivity relation;
- It's more easy to measure jitter transfer and jitter sensitivity at TX side.
- At RX, depending on loopback mode, different methods are used to measure the relation.

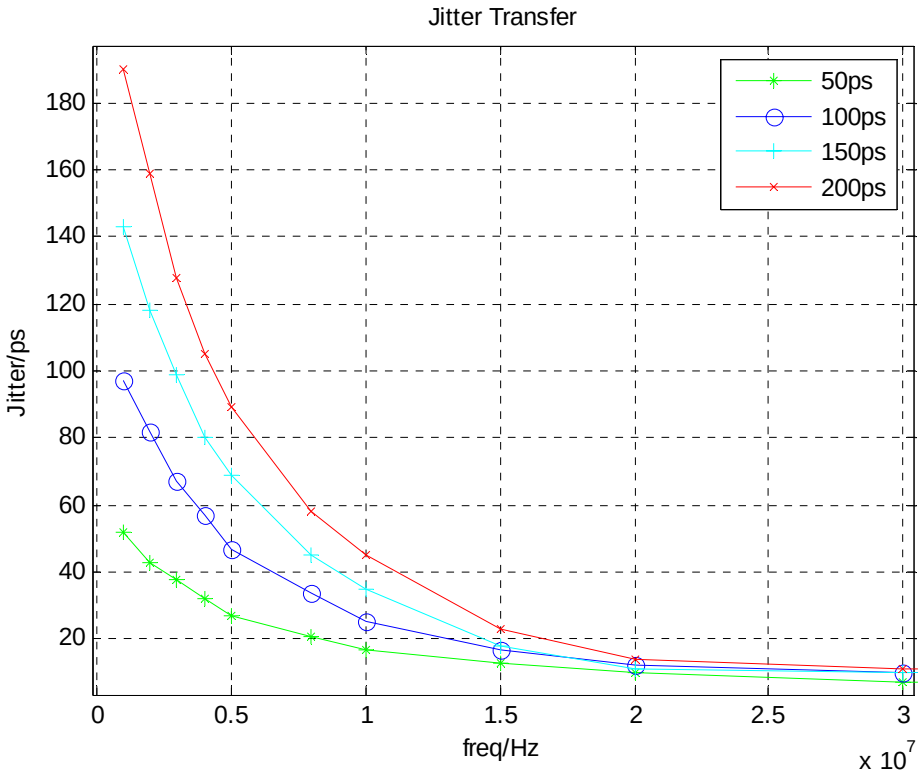


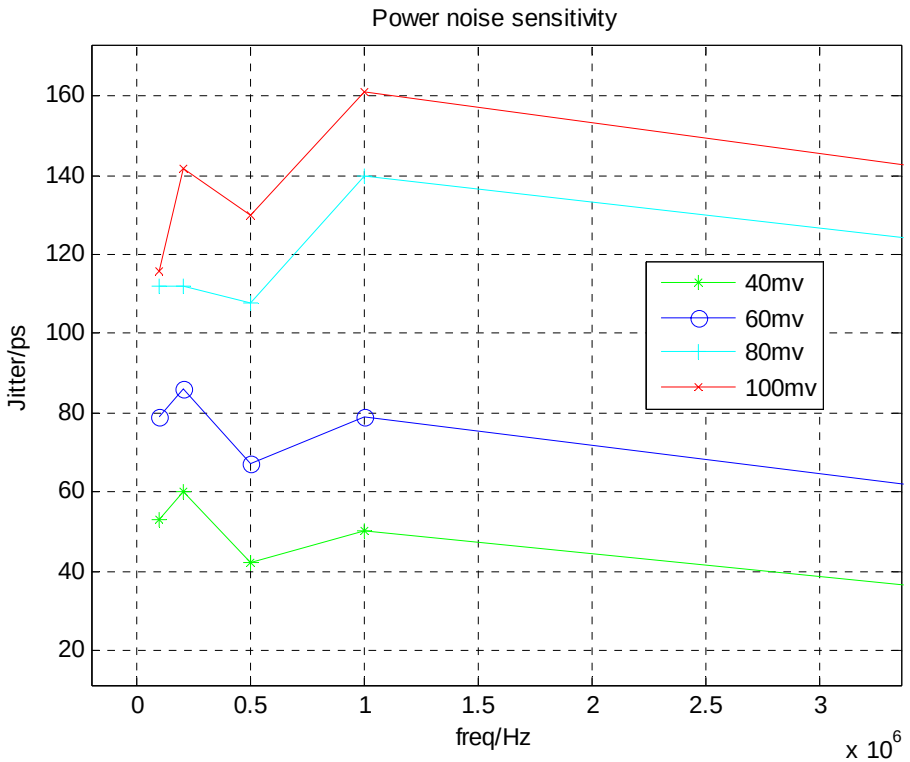
Jitter transfer measurement at TX

Jitter sensitivity measurement at TX

Jitter Transfer and Jitter Sensitivity Example

- A PLL characteristics derived by measurement;
- Left picture is showing the jitter transfer relation;
- Right picture is showing the jitter sensitivity relation;





2. Power Noise Simulation Method

How to get power noise at PLL

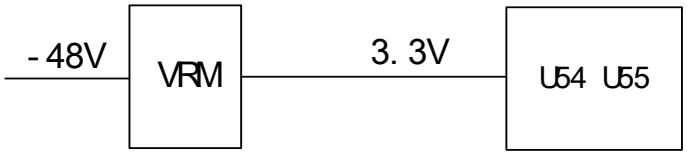
- PI analysis method could be borrowed here to analyze power noise at PLL power pin;
- PI analysis method should have the ability to predict and analyze the power noise at desired points on PCB board.

PI analysis flow in Huawei has three steps:

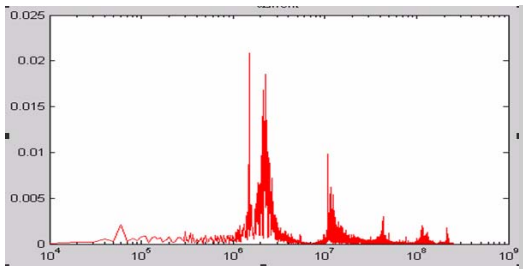
- Getting PI component models including capacitor, inductor, VRM, IC noise current and P/G plane;
- Getting impedance of PDS with PI component models;
- Predicting voltage noise magnitude of PDS in time domain.

Power Noise Analysis Example

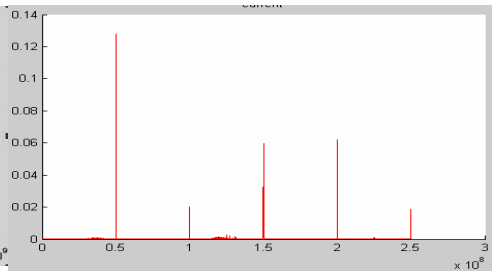
➢3.3V power example:



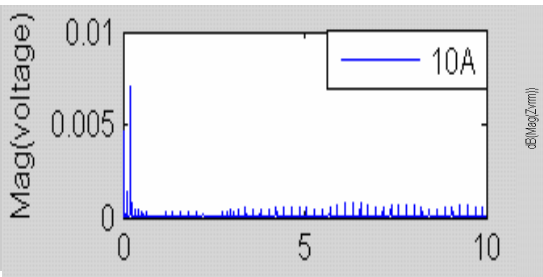
➢Models in frequency domain:



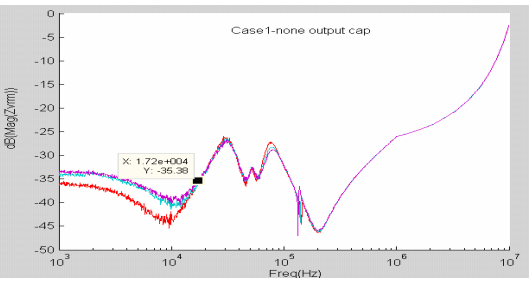
The noise current model of u55



The noise current model of u54

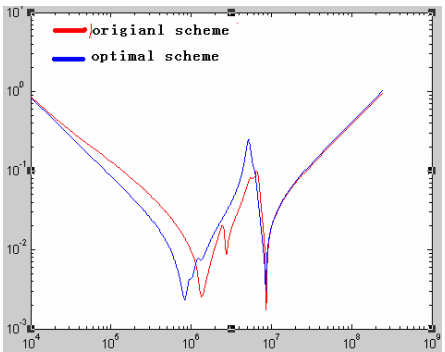


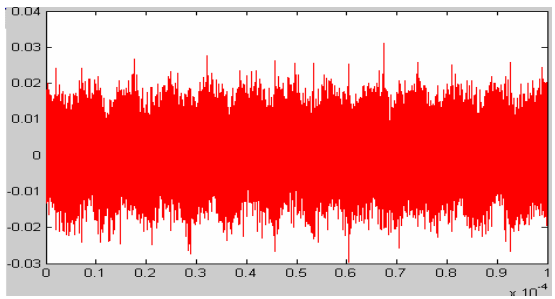
The noise current model of VRM



The impedance model of VRM

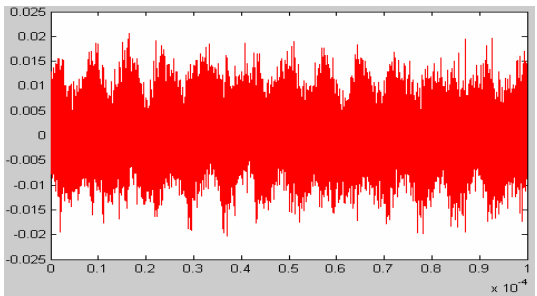
➢ Impedance simulation of PDS





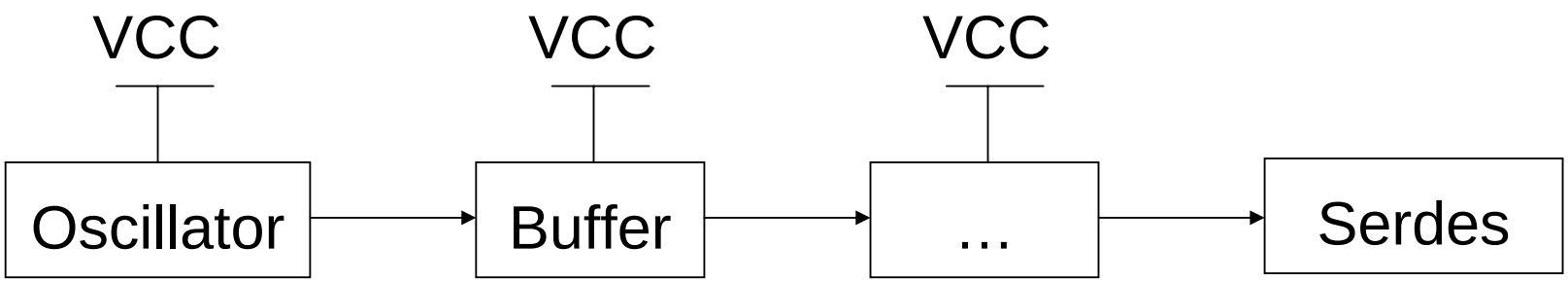
Original

Optimal



3. Simulating Reference Clock Jitter

- Supposing that jitter transfer function and power noise sensitivity function of each component on clock chain are known;
- Jitter transfer function and jitter sensitivity of power supply of clock chain component could be derived by measurement;
- Power noise of VCC can be obtained from PI analysis;
- Similar analysis method with PLL jitter analysis, jitter could be calculated node by node;



4. Calculating Jitter Introduced from PLL

- Convolution Equation could be transformed into frequency domain;
- When jitter transfer function is known, jitter introduced from input clock could be calculated;

  Jitter(f) = transfer_function(f)*jitter_clock_in(f)
- When jitter sensitivity profile is known, jitter introduced from power noise could be calculated;

  Jitter(f) = jitter_sensitivity(f)* power_noise(f)
- Jitter transfer and jitter sensitivity may not contain phase information. The jitter result could be handled as PDF.

1) PCIE has used similar method to simulate and analyze the clock jitter transfer on serial link.
2) Rambus Ralf Schmitt gave the analysis of supply noise induced jitter in his designcon 2007 papper.

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Next Step

- Try the whole analysis method step by step and find some flaws inside it.
- Improving current measurement method to measure jitter transfer function and jitter sensitivity at RX side;
- Correlating the simulated results and measured results;

Summary of PLL model

An initial idea about how to analyze PLL effects presented here, including power noise and clock jitter transfer;

- PLL model should at least include jitter sensitivity of power noise and jitter transfer function;
- Jitter relationship in PLL may be expressed as function of LTI system or subsection linear system;
- PI analysis method is used to estimate power noise;
- Jitter analysis method is used to predict jitter on clock chain;

It is never too early for us to consider the PLL model problem in AMI model