WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Open Forum, I would like to welcome our presenters and guests to our third annual IBIS Summit in China.

We continue to appreciate the growth of the IBIS events in China and are pleased at the advanced technical materials presented and discussed. We are especially grateful to our sponsors Huawei Technologies, Agilent Technologies, Ansoft Corporation, Cadence Design Systems, Intel Corporation, Mentor Graphics Corporation, Signal Integrity Software (SiSoft), Sigrity, Synopsys and ZTE Corporation.

Our thanks to you for participating and best wishes for a successful summit.

Sincerely,

Michael Mirmak
Chair, EIA IBIS Open Forum

我代表缓冲器信息标准化(IBIS)论坛,欢迎你,主持人和来宾,参加我们的第三届研讨会议在中国召开.

我们很高兴的看到 IBIS 在中国的继续成长,并很高兴能在这里就各项先进技术进行再次进行介绍和讨论.我们也特别感谢我们的赞助商华为技术有限公司, 安捷伦技术公司, Ansoft 公司, Cadence 设计系统公司, 英特尔公司, Mentor Graphics 公司,信号完整性软件公司(Sisoft), Sigrity, Synopsys 公司和中兴通讯为此会议做出的贡献。

再次感谢您,也预祝会议的圆满成功。

迈克尔 莫马克
马梦宽
IBIS 委员会主席

WELCOME FROM JIANG, XIANGZHONG, HUAWEI TECHNOLOGIES

Since the year of 2005, IBIS Group has achieved its original target, that is to enhance the communication of high speed design and modeling technology within China by holding its annual meeting here. And by now its annual meeting has become our most influential domestic trade meeting. It is certain that the meeting this time will be another successful meeting held by IBIS in China.

XiangZhong Jiang
Huawei Technologies

2005 年以来，IBIS 组织在中国一年一度的会议达到了最初在中国促进高速电路设计和模型技术交流的目的，并成为中国国内有影响力的行业会议。毫无疑问，本次大会将是 IBIS 在中国的又一次成功的盛会。

姜向中
华为公司

Shenzhen 2005

Shanghai 2006

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open

9:00 Welcome and Keynote Comments
- Jiang, XiangZhong
  (Huawei Technologies, China)
- Mirmak, Michael
  (Chair., EIA IBIS Open Forum, Intel Corporation, USA)
- Invited Chinese Representative Remarks

9:30 **Wang Algebra and Interconnects 5**
Ross, Bob (Teraspeed Consulting Group, USA)

9:50 **IBIS-ATM Update: SerDes Modeling in IBIS 13**
Westerhoff, Todd (Signal Integrity Software (SiSoft), USA)

10:15 BREAK (Refreshments)

10:30 **Serial Link Analysis and PLL Model 20**
Huang, ChunXing (Huawei Technologies, China)

11:00 **A Review of Existing Multi-Gbps Serial Channel 32**
Analysis Methods and the Evolution of the Proposed
ATM Algorithmic Modeling Standard
Dodd, Ian*, Ward, Richard** and Gupta, Sanjeev*
(*Agilent Technologies, USA and **Texas Instruments, USA)

11:30 **An Overview of High-Speed Serial Bus Validation 41**
Techniques
Muranyi, Arpad and Dmitriev-Zdorov, Vladimir
Mentor Graphics Corporation, USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables
- Press Luncheon for IBIS Officers and Sponsors

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

Wang Algebra and Interconnects

Bob Ross
Asian IBIS Summit
Beijing, CHINA
September 11, 2007
bob@teraspeed.com

鲍伯若什
亚洲 IBIS 技术研讨会
中国北京
2007年09月11日

TERASPEED CONSULTING GROUP

Wang Algebra – 70+ Years Ago

K.T. Wang, "On a new method of analysis of electrical networks," in Memoirs 2, *Nat. Res. Inst. Eng. Academia Sinica*, pp. 1-11, 1934

S.L. Ting, "On the general properties of electrical network determinants," *Chinese J. Physics*, vol 1, pp. 18-40, 1935

C.T. Tsai, "Short cut methods of Wang algebra of network problems," *Chinese J. Physics*, vol. 3, pp. 141-181, 1939

R.J. Duffin and T.D. Morley, "Wang algebra and matriods," IEEE Trans Circuit and Systems, vol CAS-25, no 9, pp. 755-762, Sept., 1978

W.K. Chen, Graph Theory and Its Engineering Applications (ch. 5, sect. 4, "The Wang-algebra formulation"), World Scientific Publ., 1997

Wang Algebra:

$$\begin{matrix} XX = 0 \\ X+X = 0 \\ XY = YX \end{matrix} \quad = \quad *W*$$

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Wang Algebra

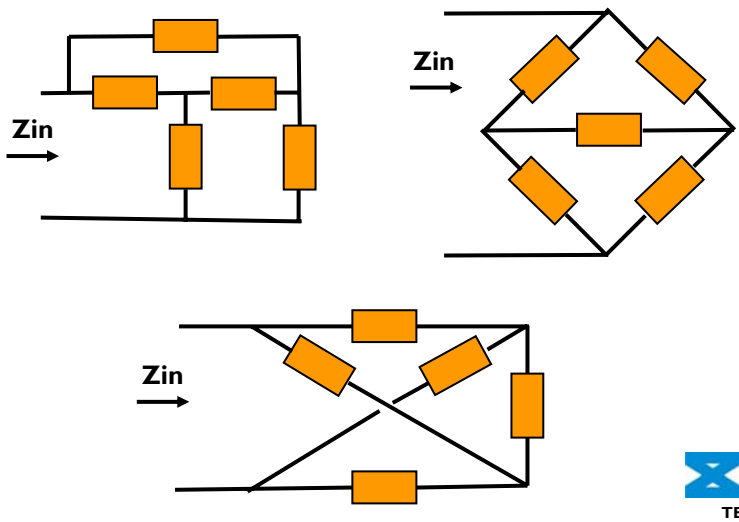
"K. T. Wang managed an electrical power plant in China, and in his spare time sought simple rules for solving the network equations. Wang's rules were published in the reference indicated below [5]. Wang could not write in English so his paper was actually written by his son, then a college student. Raoul Bott and I recognized that Wang's rules actually define an algebra. We restated the rules as three postulates for an algebra:

$$xy = yx,\ x + x = 0,\ xx = 0.$$

R.J. Duffin, "Some Problems of Mathematics and Science," Bulletin of the American Mathematical Society, Nov. 1974, p. 1060, web link: http://www.ams.org/bull/1974-80-06/S0002-9904-1974-13610-4/S0002-9904-1974-13610-4.pdf

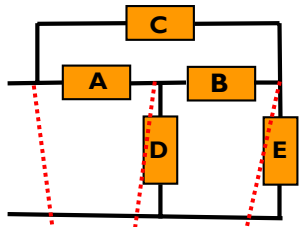
("[5]" is the K.T. Wang reference on slide 2)

Easy General Solutions (Including Difficult Topologies)



Solving [I]=[Y][V] for Zin (Traditional Method)

Zin=1/E



Nodal Equations:

A … E are admittances

E = 1/R

$$[\mathrm{I}] = [\mathrm{Y}][\mathrm{V}] = \begin{bmatrix} \mathrm{Iin} \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} A+C & -A & -C \\ -A & A+B+D & -B \\ -C & -B & B+C+E \end{bmatrix} \begin{bmatrix} \mathrm{Vin} \\ \mathrm{V_D} \\ \mathrm{V_E} \end{bmatrix},$$

$$\mathrm{Zin} = \frac{\mathrm{Vin}}{\mathrm{Iin}} = \frac{\begin{vmatrix} A+B+D & -B \\ -B & B+C+E \end{vmatrix}}{\begin{vmatrix} A+C & -A & -C \\ -A & A+B+D & -B \\ -C & -B & B+C+E \end{vmatrix}} = \frac{AB+AC+AE+BC+BD+BE+CD+DE}{ABD+ABE+ACD+ACE+ADE+BCD+BCE+CDE}$$

(18 initial terms yields 8 final denominator terms)

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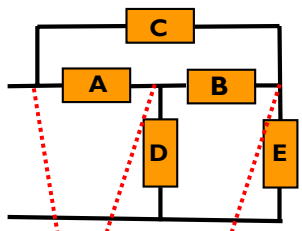
Solving [I]=[Y][V] for Zin = R (Wang Algebra)

Zin=1/E



Nodal Equations:

A … E are admittances

E = 1/R

$$\mathrm{Zin} = \frac{\text{numerator}}{\text{denominator}} = \frac{(A+B+D)*\mathrm{W}*(B+C+E)}{(A+C)*\mathrm{W}*(\text{numerator})} = \frac{1}{E}$$

XX=0 →

X+X=0 → (after XX=0)

$$= \frac{AB+AC+AE+\cancel{BB}+BC+BE+BD+CD+DE}{\cancel{ABC}+ABE+ABD+ACD+ADE+\cancel{ABC}+ACE+BCE+BCD+CDE}$$

$$= \frac{AB+AC+AE+BC+BD+BE+CD+DE}{ABD+ABE+ACD+ACE+ADE+BCD+BCE+CDE}$$

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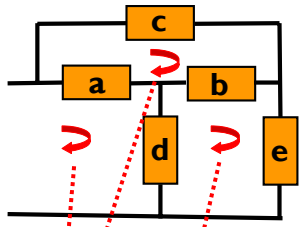
Solving [V]=[Z][I] for Zin= 1/Yin = R (Wang Algebra)

Yin=1/e



Loop Equations:

a … e are impedances

e = R

$$\text{Yin} = \frac{\text{numerator}}{\text{denominator}} = \frac{(a+b+c)*\boxed{W}*(b+d+e)}{(a+d)*\boxed{W}*(\text{numerator})} = \boxed{\frac{1}{e}}$$

XX=0 →

X+X=0 → (after XX=0)

$$= \frac{ab + ad + ae + bb + bd + be + bc + cd + ce}{abd + abe + abc + acd + ace + abd + ade + bde + bcd + cde}$$

$$= \boxed{\frac{ab + ad + ae + bd + be + bc + cd + ce}{abc + abe + acd + ace + ade + bde + bcd + cde}}$$

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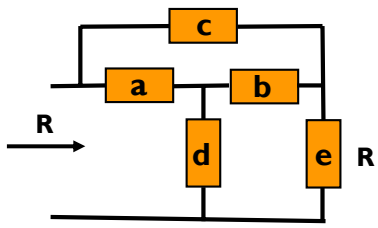
Constant R Constraint



General

$$d(a+b) + ab + \mathrm{R}(a-b) - \mathrm{R}^2 - \frac{\mathrm{R}^2(a+b)}{c} = 0$$

Symmetric (a = b)

$$2da + a^2 - \mathrm{R}^2 - \frac{2\mathrm{R}^2 a}{c} = 0$$

Substitute impedances and equate powers of the Laplace variable "s" for constant R relationships

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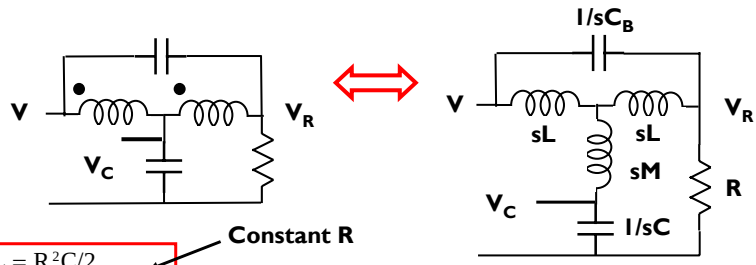
(Constant R) T-coil Example



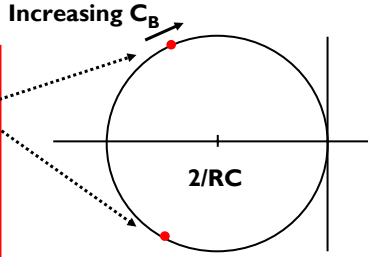
Constant R

$$L = R^2C/2$$

$$M = R^2C_B - L/2$$

$$\frac{V_C}{V} = \frac{1}{R^2CC_Bs^2 + \frac{RC}{2}s + 1}$$

$$\frac{V_R}{V} = \frac{R^2CC_Bs^2 - \frac{RC}{2}s + 1}{R^2CC_Bs^2 + \frac{RC}{2}s + 1}$$



Poles 30 degrees for maximally flat envelope delay (MFED)

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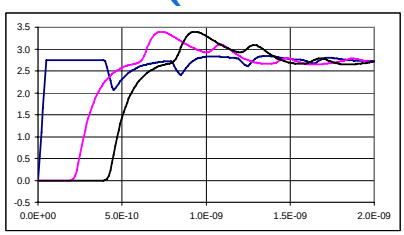
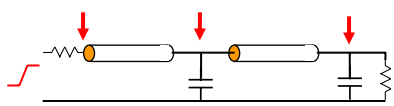
T-coil Improvement (Terminated Multi-drop Line)

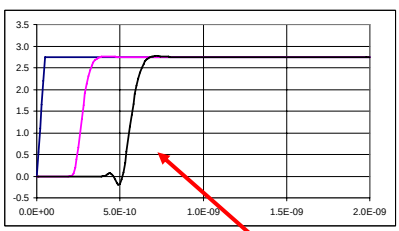


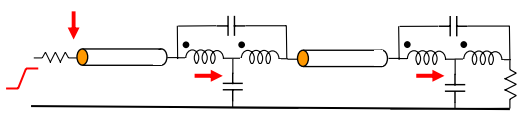


Rsource = 10 Ω, Rload = 50 Ω

C = 2 pF, TL = 50 Ω, 200 ps

Vin = 0 to 3.3 V, 50 ps ramp





Cleaner and faster responses, but with more delay

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Historical Applications (1)

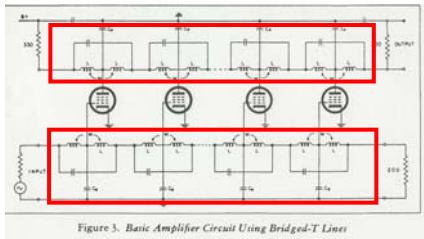
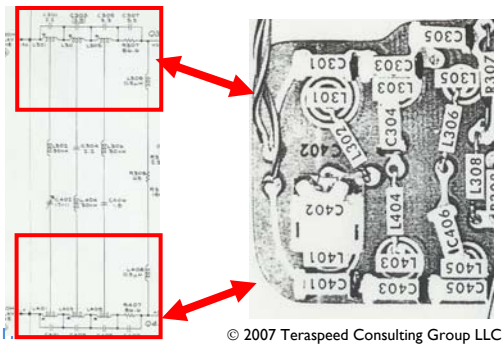


Figure 3. Basic Amplifier Circuit Using Bridged-T Lines

High speed (traveling wave) distributed amplifier in 1940's (Similar to GTL and source synchronous control)



Dual input delay line phase equalization using cascaded printed circuit board T-coils in 1960's

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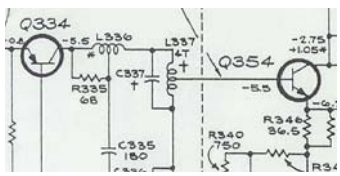
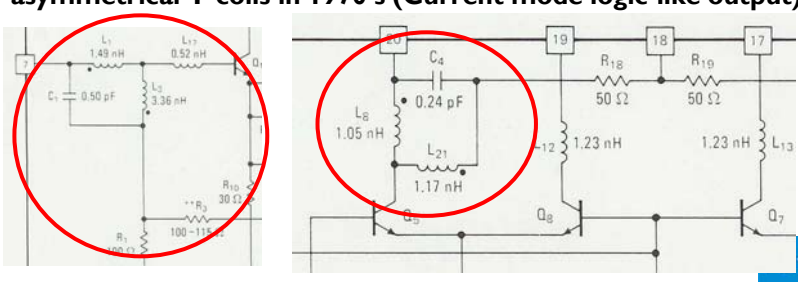
Historical Applications (2)



Parasitic bandwidth switch compensation and cascaded interstage peaking in 1960's

One-half of hybrid IC differential 50 Ω input and 50 Ω output with asymmetrical T-coils in 1970's (Current mode logic-like output)



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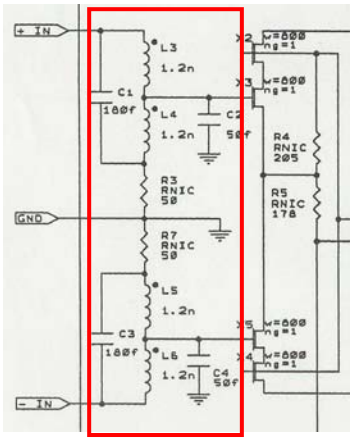
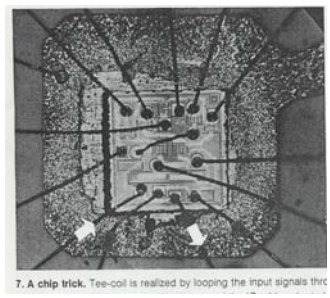
Historical Applications (3)



High speed 50 Ω input for FET hybrid IC and with metalization (not shown) for T-coils in 1990's



7. A chip trick. Tee-coil is realized by looping the input signals thro

Package bond wire compensation with T-coil trick in 1970's

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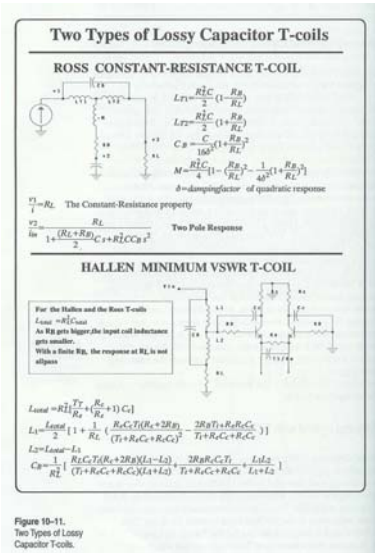
Original and General Lossy Derivations Used Wang Algebra



Two Types of Lossy Capacitor T-coils

ROSS CONSTANT-RESISTANCE T-COIL

HALLEN MINIMUM VSWR T-COIL

Figure 10-11. Two Types of Lossy Capacitor T-coils.

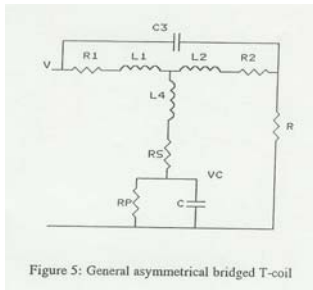


Figure 5: General asymmetrical bridged T-coil

B. Ross, "Generalizaton of T-Coil Equations," Proceeding of the Third Electrotechnical and Computer Science Conference ERK'94 (in Slovenia) Sept. 26-28, 1994, pp. 39-43.

Tuned for bipolar transistor technology

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T-coils, Interconnect, Terminators

- T-coil summary
  - Constant R provides ideal load or termination
  - MFED: 2.73 bandwidth improvement over RC
  - MFED: 0.4% overshoot for ideal step input
  - Complexity reduction (poles/zero cancellation): usually produces second order function for easier design
  - Lossless case: ideal MFED, double terminated thru path
- Interconnects and terminators
  - Older high-speed analog design ideas apply to current high-speed digital interconnects
  - Constant R target yields many benefits

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Wang Algebra

- Useful "trick" for easy calculations
  - Regular algebra plus xx=0, x+x=0 for on-going simplification
  - Numerator calculation first
  - Denominator from numerator result
  - Listing "xx" cancelled terms unnecessary
  - Accurate for larger, complex networks
- Used for T-coil technology advances

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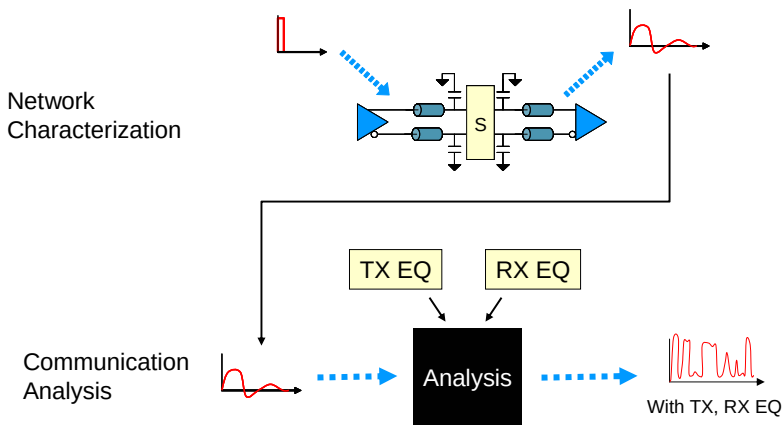
IBIS-ATM Update: SerDes Modeling and IBIS

Presented by: Todd Westerhoff, SiSoft
twesterh@sisoft.com

IBIS Summit
Beijing, China
September 11, 2007

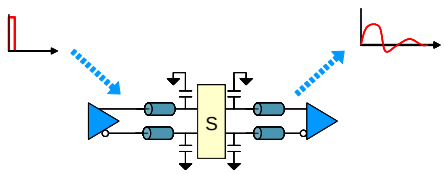
Typical SerDes Analysis Flow



Why Two Analysis Steps?

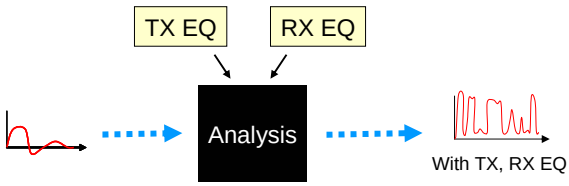
- Performance
  - Communications analysis processes ~ 1,000,000 bits per minute
  - SPICE-based analysis throughput is much less
- Leverage existing tools and techniques
  - Communications methods & algorithms established in other domains
  - Equalization and clock recovery well suited to algorithmic description
  - Modeling/analysis algorithms are suitable for commercial numerical computation tools

Network Characterization



- Uses circuit analysis techniques to determine network behavior under reference conditions
- Characterization can take multiple forms
  - Impulse / step / pulse response (time-domain)
  - Transfer function (frequency-domain)

Communications Analysis



- Uses circuit characterization data to predict link behavior
- Many methods exist – fundamental concepts are similar, but implementation details vary
  - Commercial numerical computation tools
  - Collaboration efforts (StatEye)
  - In-house SerDes vendor solutions
  - Commercial systems-level analysis tools

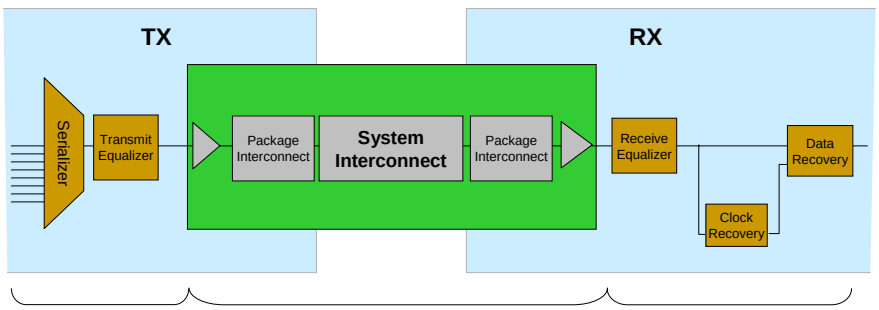
SerDes Analysis

- Serial Links present new analysis requirements
  - Model SerDes TX/RX equalization
  - Model RX clock recovery behavior
  - Predict link behavior over >> 10^7 bits
  - Predict link bit error rate
  - Protect SerDes vendor IP
- Serial Link analysis often combines analytical methods
  - Circuit analysis (network characterization)
  - Communications analysis (equalization, clock recovery modeling)
- Modeling standards are *essential*, there can be no interoperable models or analysis tools without them

IBIS-ATM SerDes Task Group

- Goal: SerDes Rx/TX model interoperability
  - Multiple EDA platforms
  - Multiple SerDes vendor models
  - Protect SerDes vendor IP
- IBIS-ATM committee participation
  - EDA: Agilent, Cadence, Mentor, SiSoft
  - Semiconductor: IBM, Intel, Micron, ST-Micro, TI, Xilinx
  - System: Cisco
- Two part modeling standard
  - Characterization model: existing IBIS syntax models TX / RX analog characteristics
  - Algorithmic model: equalization, clock recovery, device optimization algorithms

IBIS-AMI Serial Link Analysis



TX EQ
LTI or non-LTI

- TX Equalization
- TX Optimization

Channel & Analog I/O
Linear, Time-Invariant

- Channel Characterization (Impulse response)

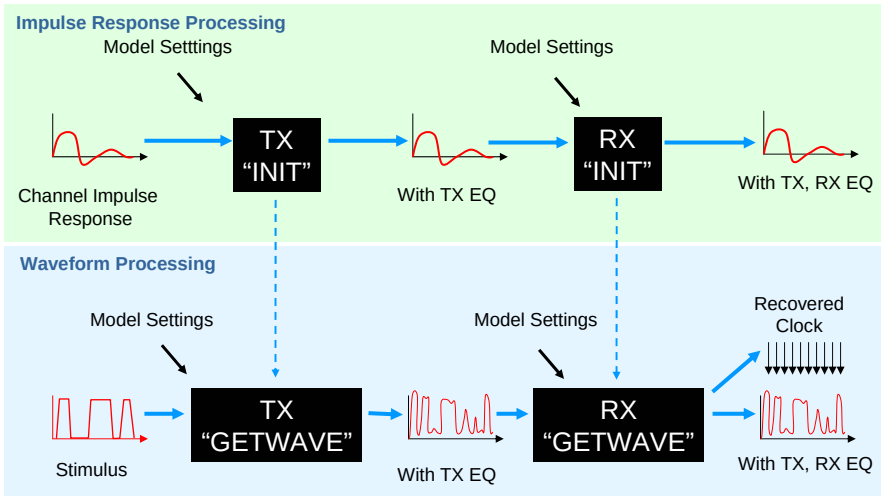
RX EQ, CDR
LTI or non-LTI

- RX Equalization
- RX Clock Recovery
- RX Optimization

IBIS-ATM Algorithmic Models

- Communication models provided as [binary] code
  - Fast, efficient execution
  - Protects vendor IP
  - Extensible modeling capability
  - Allows models to be developed in multiple languages
- Standardized execution interface
  - Module loading mechanism & call signature
  - Data input/output formats
- Standardized model parameter interface
  - "Reserved parameters" interpreted by EDA platforms
  - Model-specific parameters can be exposed to and set by end-users

IBIS-ATM Algorithmic Models



Executable (DLL) Call Arguments

- Init (impulse response processing)
  - Bit time
  - Number of waveform samples per bit
  - Number of crosstalk aggressors
  - Channel impulse response(s)
  - Model parameters and values
  - Pointers to free memory, data return area
- Getwave (waveform processing)
  - Input waveform(s)
  - Pointers to data return area
    - Equalized waveform
    - Clock times
    - Optimized parameters

Model Parameters

Additional data passed between executable model & simulator:

- Model-specific parameters
  - Allow IP vendors to define data required for / provided by a specific model
  - Defined parameter declaration and usage format
    - Allows end-users to set and display model-specific data
- Reserved parameters
  - Predefined parameter list used by EDA tools to alter analysis flow
  - Allows models to tell EDA platform what data the model does/doesn't provide

IBIS-ATM Status

- Original proposal submitted by Cadence & IBM
  - Current version authored by Cadence, Mentor, SiSoft
- First draft of BIRD approved by IBIS-ATM task group for prototype model & EDA platform development
  - Prove interoperability & refine proposal before bringing back to IBIS Open Forum
- Subcommittee work, presentations & BIRD available on-line:
  - http://www.vhdl.org/pub/ibis/macromodel_wip/
- Public TX/RX models, modeling "toolkits" will be available

Next Steps

√	Preliminary approval by IBIS-ATM subcommittee
√	Complete BIRD documentation
√	Develop sample models & prototype EDA integration; demonstrate interoperability
Target: Sep 2007	Refine BIRD based on prototype experience
Target: Oct 2007	Bring to IBIS-ATM task group for final approval
	Bring BIRD to IBIS Open Forum for approval
	Incorporate BIRD into updated IBIS specification

25. July 2007

Serial Link Analysis and PLL Model

September 11, 2007
Asian IBIS Summit, Beijing China

Huang Chunxing
huangchunxing@huawei.com

www.huawei.com

Agenda

High-speed serial link simulation

- Current simulation method overview
- Simulation with AMI model

PLL model

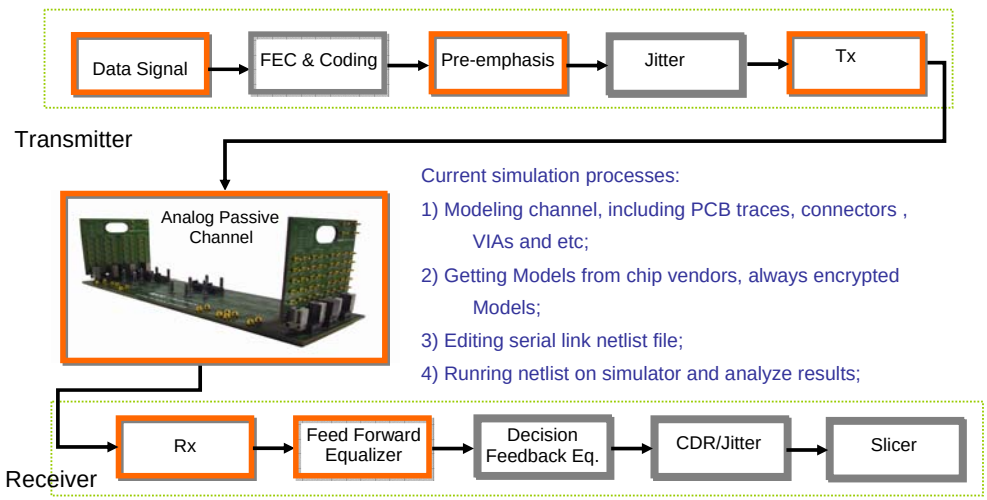
- Jitter introduced by PLL
- Jitter simulation with PLL model

High-speed Serial Link Simulation

- Simulation purpose:
  - ✓Evaluating bit error rate performance of high-speed serial link.
  - ✓Checking whether the bit error rate of link could meet the specification of standard or requirements of product.
- More factors considered in simulation, more accurate the simulation is.
- Due to problems of model availability, simulation technology ability and limited analysis time, it's difficult, if not impossible, for SI engineers to consider all factors in system simulation.
- Serial link simulation technologies lag behind serial link development. SI engineers are struggling with models in hand to get reliable results.

Current Simulation Method Overview

- Simulation with encrypted model is mostly used method.
  Dark block is normally not supported by current simulation method.



Current simulation processes:

1) Modeling channel, including PCB traces, connectors , VIAs and etc;
2) Getting Models from chip vendors, always encrypted Models;
3) Editing serial link netlist file;
4) Runring netlist on simulator and analyze results;

Simulation Example

- Current simulation method with encrypted model is extremely difficult to modulate jitter on serial data or statistically post-process waveform.
- Encrypted model simulation is a time-consuming work.

Here is a very simple sample netlist for 2.5Gbps high-speed serial data.

40 minute simulation time to get only 132 bit results!

Add Jitter?

```
*****************************************************************************
* driver model
*****************************************************************************
*       CA0=A0  CA1=A1  CA2=A2  CA3=A3     AC_DC     AU25      CB0=B0  CB1=B1   CB2=B2  CB3=B3
XDRIUER1 DRU1GND DRU1GND DRU1UDD DRU1UDD  DRU1UDD  DRUAU25    DRU1GND DRU1GND  DRU1GND  DRU1GND
* CLK_N    CLK_P      D0        D1              OUT       OUTN
+ CLK_1N   CLK_1P data_a  data_b       DRU1OUTP  DRU1OUTN
*   PWR0    PWR1    PWR2           TERM_75_IN  VBGAP    VDD     VSS     AUTT    ZDI
+ DRU1UDD DRU1UDD DRU1UDD          DRU1GND     DRUBG    DRU1UDD DRU1GND  DRU1UTT  ZDI1 ULF4S8ADU1TX

*****************************************************************************
* Channel Model, simple RLGC model used here
*****************************************************************************
W1 dru1outp dru1outn gnd dru1inp1 dru1inn1 gnd n=2 rlgcfile=diff100_5_5.rlgc l=1000mil

*****************************************************************************
* Receiver model, 50ohm Termination resistance used here
*****************************************************************************
rterm1 dru1inp1 DRU1UTT 50
rterm2 dru1inn1 DRU1UTT 50

.TRAN  35ps  52.8ns
```

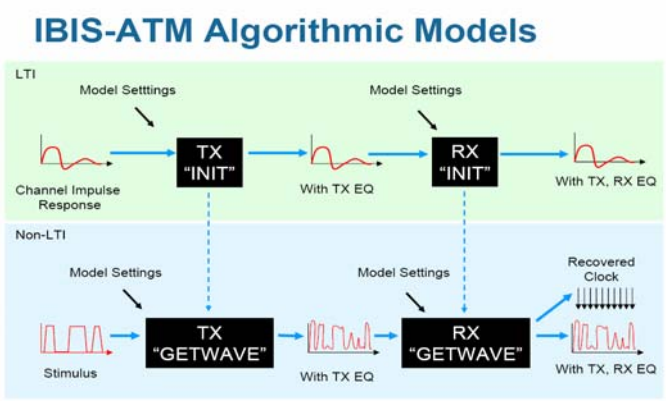
Jitter Parameters

```
total cpu time       2479.65 seconds
job started at  15:22:37  07/20/2007
job ended   at  16:04:03  07/20/2007
```


IBIS AMI Model

IBIS-ATM is working at improving simulation technique and proposing Algorithmic Modeling API (AMI) in IBIS.

- Mainly focus on emphasis, equalization and CDR modeling problems.
- LTI model and Non-LTI model



Picture reference from "SerDes Modeling and IBIS" at DAC_2007_IBIS_Summit

Simulation with AMI Model

Some welcoming features of IBIS-AMI :

1) Non-linear component Components, like DFE and CDR could be included in simulation
2) Jitter parameters defined in AMI model, permitting jitter simulation with AMI model.
3) Rx_Receiver_Sensitivity parameter defined in AMI, slicer performance is also included in simulation.
4) Simulation with AMI model will be much faster than simulation with encrypted model. Global equalization optimization becomes possible.
5) In theory, AMI can do the job of modeling new emerging algorithm.

- IBIS AMI model makes a giant step on improving serial link simulation techniques.
- AMI model still needs time to prove itself a successful solution.

Agenda

High-speed serial link simulation

- Current simulation method overview
- Simulation with AMI model

PLL model

- Jitter introduced by PLL
- Jitter simulation with PLL model

Jitter Parameters in AMI model

Jitter parameters in AMI model

1)Tx_Jitter
Tx_Jitter Info Float Gaussian <mean> <sigma>
Tx_Jitter Info Float Dual-Dirac <mean> <mean> <sigma>
Tx_Jitter Info Float DjRj <minDj> <maxDj> <sigma>
Tx_Jitter Info Float Table <time> <probability> <data> <data> EndTable
2)TX_DCD
Tx_DCD Info Float Range <type> <min> <max>
3)Rx_Clock_PDF
Rx_Clock_PDF Info Float Gaussian <mean> <sigma>
Rx_Clock_PDF Info Float Dual-Dirac <mean> <mean> <sigma>
Rx_Clock_PDF Info Float DjRj <minDj> <maxDj> <sigma>
Rx_Clock_PDF Info Float Table <time> <probability> <data> <data> EndTable

Jitter parameter of TX and RX may be not enough for analysis.

Quoted from "AMI_BIRD_DRAFT_1.0"

- **It covers single value DJ, dual-dirac DJ, uniform DJ and user-defined PDF data;**
- **These jitter parameters are used to describe jitters at transmitter and at receiver;**

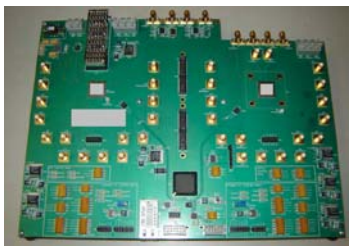
Shortage of Jitter Parameter Alone

Jitter parameters alone are not enough for serial link analysis

- Jitter parameters in AMI model are mostly measured on evaluation board by chip vendors;
- Omitting differences between evaluation board and product board;
- Jitter is a matter sensitive to environment noise;
- Simulation should carefully consider the jitter introduced by PLL from environment noise;
- Via PLL, environment noise generates a lot of jitter in serial link
  1) Phase noise of reference clock;
  2) Power noise at PLL power pins;
- Especially, power noise is an important contributor to worsen link BER;

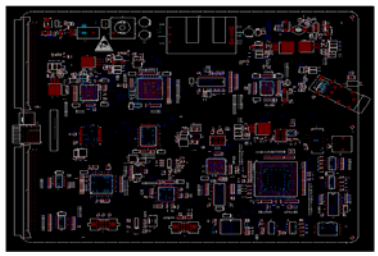
Environment Noise Difference

- Working environment of card board is much different from that of evaluation board;
- Power noise is depending on the system design;
- Power on evaluation board is much more clean than that on card board;
- Clock chain on card board may be different from that on evaluation board;



Evaluation board

≠



Card board

Jitter Introduced from PLL

At Transmitter

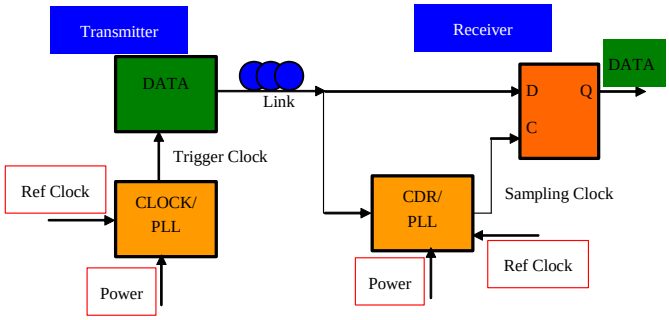
Phase noise of reference clock introduces jitter of trigger clock.

Power noise transfers into output jitter of trigger clock.

At Receiver

Phase noise of reference clock introduces jitter of sampling clock.

Power noise transfers into output jitter of sampling clock.



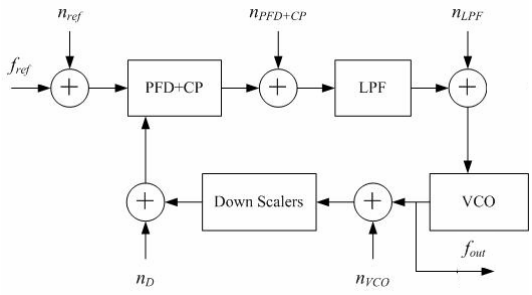
PLL Noise Model

- High-speed serial link contains PLL/DLL at both transmitter and receiver.
- PLL is a phase synchronous system, which is mainly composed of

  1) Phase Detector

  2) Low Pass Filter

  3) VCO



PLL model should include two relations:

- Jitter Transfer Function: relation between input clock jitter and output clock jitter;
- Jitter Sensitivity: relation between power noise and output clock jitter;

Jitter Simulation of PLL Model

PLL model analysis is based on the following assumptions:

- Each noise are statistically independent;
- Jitter introduced by all noises could be expressed as sum of each noise impacting jitter;
- Amplitude of noise and interference is within the linear working area of loop;
- Jitter transfer in PLL behaves like LTI system

Jitter from two noises could be estimated by convolution equation

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$

Here h(t) could be jitter transfer function and could be jitter sensitivity of power supply

Steps of PLL Jitter Analysis

Jitter simulation of PLL model is composed of

1) Getting Jitter Sensitivity and Jitter Transfer relation of PLL;

2) Estimating power noise on board;

3) Simulating Reference Clock Jitter;

4) Calculating Jitter introduced from PLL;

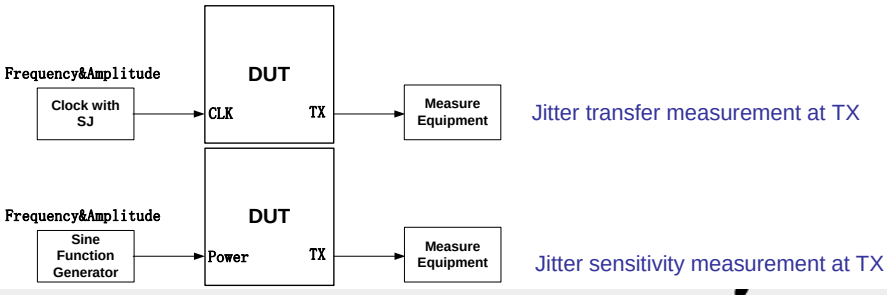
1. Getting Jitter Transfer and Jitter Sensitivity

➢Modulating jitter at input clock and measuring jitter at output data to get jitter transfer function;

➢Injecting noise at power and measuring jitter at output data to get jitter sensitivity relation;

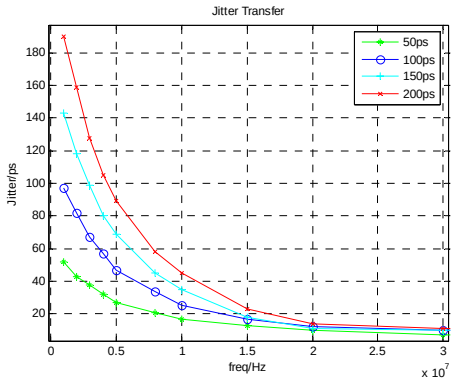
➢It's more easy to measure jitter transfer and jitter sensitivity at TX side.

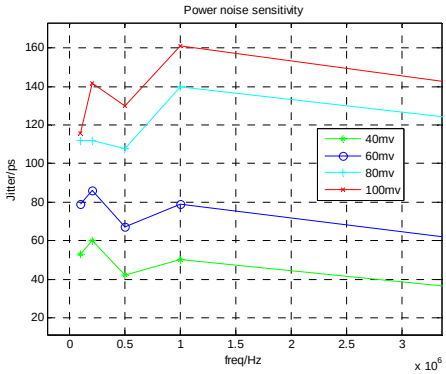
➢At RX, depending on loopback mode, different methods are used to measure the relation.



Jitter Transfer and Jitter Sensitivity Example

- A PLL characteristics derived by measurement;
- Left picture is showing the jitter transfer relation;
- Right picture is showing the jitter sensitivity relation;





2. Power Noise Simulation Method

How to get power noise at PLL

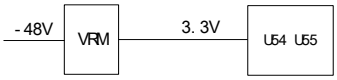
- PI analysis method could be borrowed here to analyze power noise at PLL power pin;
- PI analysis method should have the ability to predict and analyze the power noise at desired points on PCB board.

PI analysis flow in Huawei has three steps:

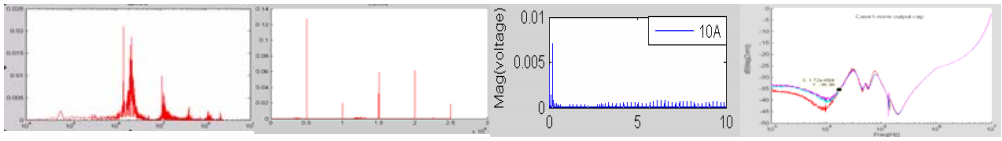
- Getting PI component models including capacitor, inductor, VRM, IC noise current and P/G plane;
- Getting impedance of PDS with PI component models;
- Predicting voltage noise magnitude of PDS in time domain.

Power Noise Analysis Example

➢3.3V power example:

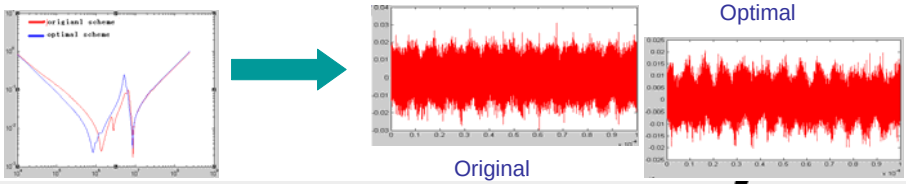


➢Models in frequency domain:



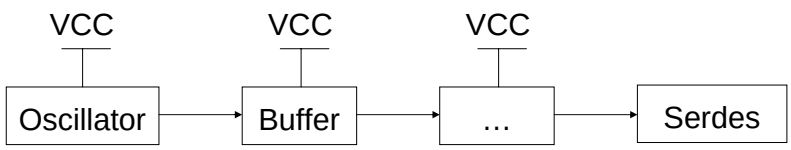
The noise current model of u55 | The noise current model of u54 | The noise current model of VRM | The impedance model of VRM

➢ Impedance simulation of PDS



3. Simulating Reference Clock Jitter

- Supposing that jitter transfer function and power noise sensitivity function of each component on clock chain are known;
- Jitter transfer function and jitter sensitivity of power supply of clock chain component could be derived by measurement;
- Power noise of VCC can be obtained from PI analysis;
- Similar analysis method with PLL jitter analysis, jitter could be calculated node by node;



4. Calculating Jitter Introduced from PLL

- Convolution Equation could be transformed into frequency domain;
- When jitter transfer function is known, jitter introduced from input clock could be calculated;
  Jitter(f) = transfer_function(f)*jitter_clock_in(f)
- When jitter sensitivity profile is known, jitter introduced from power noise could be calculated;
  Jitter(f) = jitter_sensitivity(f)* power_noise(f)
- Jitter transfer and jitter sensitivity may not contain phase information. The jitter result could be handled as PDF.

1) PCIE has used similar method to simulate and analyze the clock jitter transfer on serial link.
2) Rambus Ralf Schmitt gave the analysis of supply noise induced jitter in his designcon 2007 papper.

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Next Step

- Try the whole analysis method step by step and find some flaws inside it.
- Improving current measurement method to measure jitter transfer function and jitter sensitivity at RX side;
- Correlating the simulated results and measured results;

Summary of PLL model

An initial idea about how to analyze PLL effects presented here, including power noise and clock jitter transfer;

- PLL model should at least include jitter sensitivity of power noise and jitter transfer function;
- Jitter relationship in PLL may be expressed as function of LTI system or subsection linear system;
- PI analysis method is used to estimate power noise;
- Jitter analysis method is used to predict jitter on clock chain;

It is never too early for us to consider the PLL model problem in AMI model

Ian Dodd, Signal Integrity Market Segment Specialist
Richard Ward, Texas Instruments.
Sanjeev Gupta, SI Product Marketing Manager, Agilent Technologies

A Review of existing Multi-Gbps Serial Channel Analysis Methods and the Evolution of the Proposed IBIS ATM Algorithmic Modeling Standard

IBIS Open Forum,
Beijing, China
11th September 2007

contact: ian_dodd@exch.agilent.com

Texas Instruments

Agilent Technologies

Introduction

The IBIS Advanced Technology Modeling (ATM) committee has a proposal for a flexible approach to system level modeling of multi-Gbps channels

The principal target for this modeling technology is the PCB system designer

Other standards bodies such as the IEEE and INCITS have undertaken major efforts to define standards for multi-Gbps channels

This includes standardized modeling for these channels, principally targeted at the IC designer

This paper contrasts the modeling approaches and shows how the IBIS ATM proposal promises to solve problems not addressed by previous solutions

It also suggests how some of the features of previous approaches could be incorporated into the IBIS ATM proposal at future date.

Overall goal – Design and implement reliable 1-10Gbps self clocked serial channels

The Silicon Vendor

Design Transmitter and Receiver meeting specified channel standard and BER

- **Must be interoperable with other vendors designs for that channel standard e.g. 802.3ap and CEI11**

Simulate Transmitter, Receiver and representative interconnect

Create Prototype silicon and PCB, measure actual performance

- **Silicon design must tolerate a range of real PCB channel layouts with connectors, vias and cables**

Correlate simulation results to measurements to fine tune the modeling process

The PCB System Implementer

Choose IC vendors and technology

Plan channel implementation: set constraints on layers, lengths, via types

Simulate Transmitter, Receiver with representative interconnect

Layout channel, re-simulate with accurate modeling of channel

Fabricate PCB, measure actual performance

Correlate simulation results to measurements to fine tune the modeling process

Distribution of multi-Gbps models from the IC vendor to the PCB systems implementer

In creating models, the IC vendor wishes to satisfy customers while:

Protect their intellectual property

Delivery accurate, easy to use models that require a minimum of support

Minimize the incremental cost in providing externally distributed models

The PCB System Implementer has additional preferences:

Compatibility of models between IC vendors and support from multiple SI analysis tools

Simulation speeds that allow full coverage of a design including corner case analysis

This presents new model creation challenges for the IC vendor

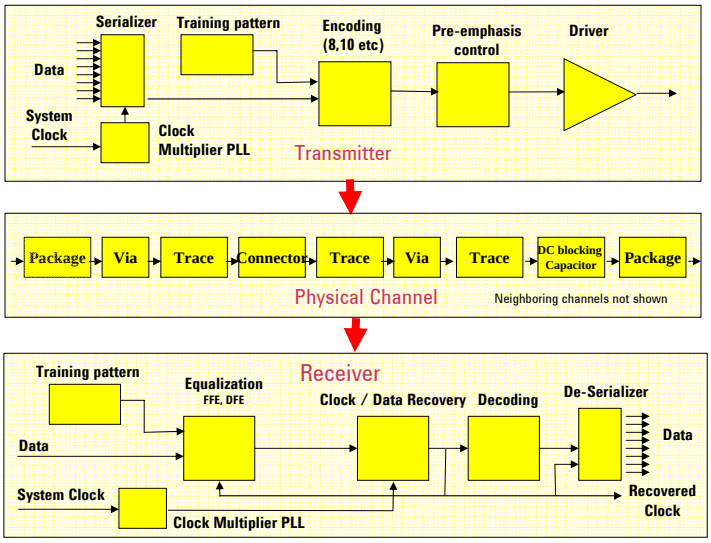
Historically many IC vendors internally utilized SPICE to design their general purpose buffers

IBIS was the preferred format for model distribution, frequently created from the IC vendors internal SPICE models using SPICE to IBIS utilities

Some IC vendors preferred to delivered encrypted versions of their internal SPICE models.

Today IC vendors are internally using a mixture of SPICE, RTL and system level tools to design multi-Gbps buffers and the channel control logic

The topology of a typical 6 Gbps serial channel



Approaches to multi-Gbps simulation

Transistor and circuit level

Drivers and receivers are modeled using SPICE, IBIS and SPICE macro-models

Packages and interconnect are modeled using transmission line and 'S' parameter models

Minimize the incremental cost in providing externally distributed models

Good accuracy but poor simulation speed

Circuit and system level co-simulation

Drivers and receivers are modeled using IBIS and SPICE macro-models co-simulating with RTL, Verilog AMS, VHDL-AMS, System-C, Proprietary 'C' or 'C++" and system level simulation tools.

Packages and interconnect are modeled using impulse response, transmission line and S-parameter models

Good accuracy and moderate simulation speed

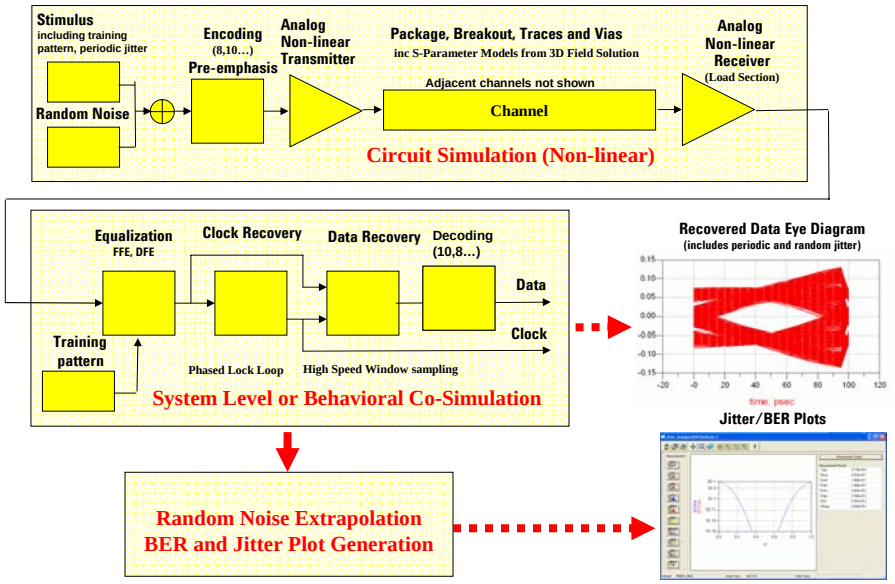
System level simulation

Drivers and receivers are modeled using RTL, Verilog AMS, VHDL-AMS, System-C, Proprietary 'C' or 'C++" and system level simulation tools.

Channels are characterized using impulse response or S-parameter models

Moderate Accuracy with good simulation speed

Circuit and system level co-simulation of a multi-Gbps channel



Circuit and system level co-simulation

Introduction

Presently favored by IC vendors for internal use

Explicitly implemented as co-simulation between a circuit level and system level simulator

Implicitly implemented as structural and behavioral modules in a AMS/SPICE simulation

The number of nodes in the circuit simulation generally governs simulation performance

- For best results use IBIS or behavioral models for the analog portion of buffers

It is critical to choose a tool with fast and accurate S-parameter simulation

Major Benefits

Can use the primary models used to design the silicon

Can include channel protocol logic e.g. training patterns in original design language e.g. RTL

Supports non-linear drivers and loads with complex random jitter sources

Disadvantages

No standard interface between the models and the simulator

- Can an extension to the IBIS ATM proposal be used to solve this issue?

Waiting for IEEE standardized HDL encryption

Example of circuit and system co-simulation

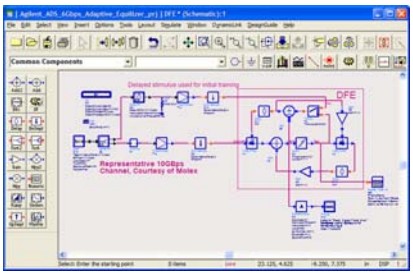
Simulation of a representative 10 Gbps channel with initial training and dynamic equalization

3000 bit training sequence

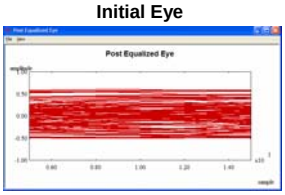
The initial eye is completely closed

The FFE and DFE coefficients can be seen to change as a function of the stimulus

Environmental variables such as supply voltage, temperature and humidity will also affect coefficients

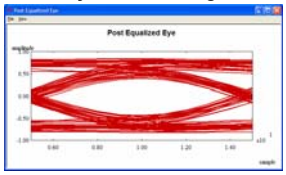


Initial Eye



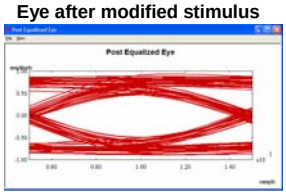
FFE and DFE coefficients

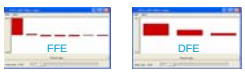
Eye after training



FFE and DFE coefficients

Eye after modified stimulus





FFE and DFE coefficients

Obtaining meaningful data from a limited dataset

Random jitter will include low probability events that have a major influence of the overall bit error rates for a channel

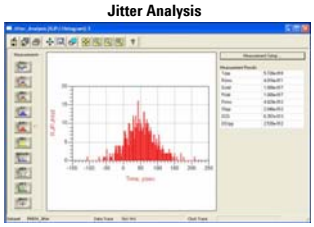
Statistical methods allow the full random jitter distribution to be predicted from the results of simulating a channel for a comparatively short number of bits

The figures on the right show the statistical separation of random jitter from the combination of deterministic jitter and random jitter and the subsequent extrapolation of a worst case BER plot

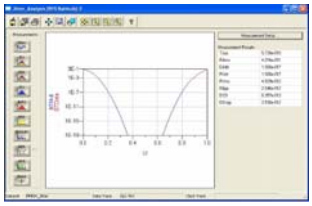
Other statistical methods such as improved importance sampling can achieve a similar result.

Instruments used to do hardware validation of multi-Gbps channels use similar statistical analysis to predict BER from a finite data sample

Jitter Analysis



Worst Case BER Plot



Observations on circuit and system co-simulation

Circuit and system co-simulation allows the behavior of multi-Gbps channels to be modeled to a very high level of accuracy

This includes the accurate modeling of random jitter and the prediction of its effect on the overall BER

It is important to note that there are many sources of random jitter

As an example, just a few sources of random jitter present in the transmitter include:

- **Thermal noise**
- **Jitter in the system clock,**
- **Jitter inherent in the clock multiplier PLL design and noise introduced into it from the reference planes**

Although this analysis of circuit and system co-simulation concentrates on driver and receiver modeling, it is also essential to also accurately model the interconnect over the full range of frequencies used for signaling.

In particular, vias and breakouts if not designed appropriately, will severely compromise channel reliability.

- **3D EM modeling is generally required**
- **Decomposition techniques that ignore the significant fringing fields generally produce inadequate results**

Established system level multi-Gbps solutions: StatEye

The StatEye tool was developed during the creation of the Optical Internetworking Forum CEI standard

Original authors: Anthony Sanders and Edoardo Prete of Infineon

Available as open source

Included as an integral part of compliance testing for multiple high speed channel standards

Provides a fast standardized analysis including:

Transmitter FFE and receiver FFE and DFE equalization with automatic optimization

Channel ISI and crosstalk noise from adjacent channels

Random jitter

Computes output pulse spectrum, bathtub curve and eye diagrams for different BER's

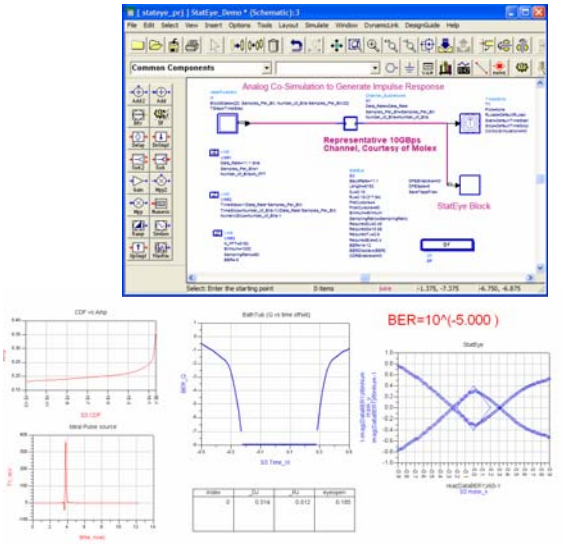
StatEye Example

Simulation of a representative 10 Gbps channel

Circuit simulation provides the impulse response of the channel, optionally including crosstalk from adjacent channels

The StatEye module calculates the optimal FFE and DFE coefficients

The BER and statistical eye is then generated



New system level multi-Gbps solutions: IBIS ATM

There is a critical need for standardized system level analysis for multi-Gbps channels

Moving forward, we need the ability to model much more complex drivers and receivers than those presently built into StatEye.

Need transmitter and receiver models that are interchangeable between IC vendors as EDA tools

Require a standard interface so models can be automatically incorporated into simulations

The IBIS Advanced Technology Modeling working group has proposed a system level simulation framework

Well defined programmatic interfaces to algorithmic transmitter and receiver models

Standardized parameter passing

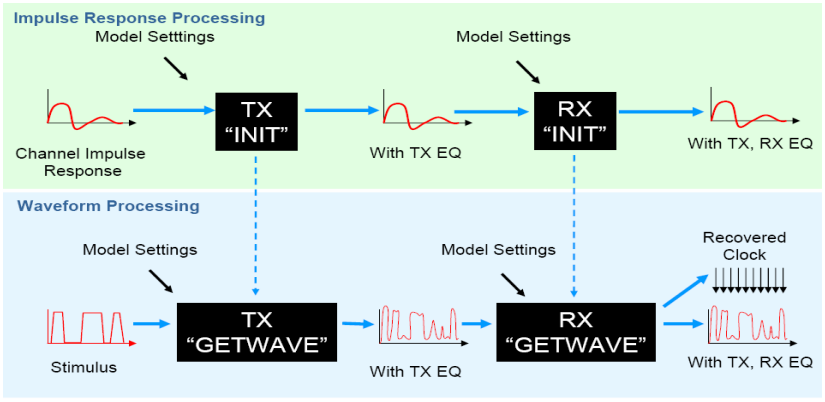
Initial effort has been to develop fast system level solutions suitable for PCB interactive and batch analysis

This framework and standardized model interface promises to solve many of the current system level simulation issues

At this time, reference models are available and their use in simulations demonstrated

Further details of the progress of the working group will be presented in an separate paper

The Standardized Interfaces of the IBIS ATM Algorithmic Transmitter and Receiver Models



Graphic courtesy of Todd Westerhoff, SiSoft

Observations on the IBIS ATM multi-Gbps proposal

The IBIS ATM working group proposal offers a flexible solution to system level multi-Gbps modeling

The working group has exhaustively considered alternate approaches and found this to be the most practical

At this time the proposal includes a well defined interface between the simulation framework and the models including parameter passing from the IBIS source file

It took a lot of hard work on behalf of the working group to achieve this result!

A general review of multi-Gbps analysis methods suggests that once the existing proposal is passed it could be further refined:

Standardized information as to which sources of jitter are included in the model

- **Allows appropriate statistical post-processing to obtain worst case BER**

A standardized approach for including RTL and other system level descriptions into the receiver and transmitter modules

- **Many IC vendors use RTL to synthesize their silicon designs**
- **The conversion of RTL into 'C' or other conventional programming languages would add costs and be a major source of modeling errors**
- **There appear to be few technical obstacles to this extension**

Conclusion

There are a multitude of approaches to multi-Gbps channel analysis

This paper has presented just a few examples

IC vendors have historically favored a combination of circuit and system level simulation

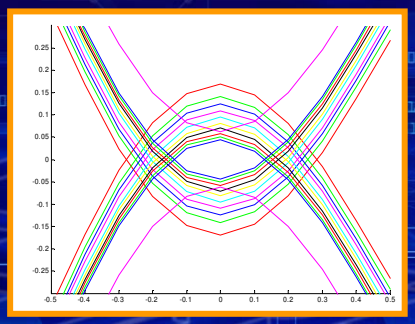
PCB system designers have a need to do system level channel analysis

The lack of a standard way of deriving system level models that protect IP from the IC vendors internal models is a major issue.

The IBIS ATM working group has made considerable progress in solving this crucial issue

An Overview of High-Speed Serial Bus Simulation Technologies

Asian IBIS Summit, Beijing, China
September 11, 2007



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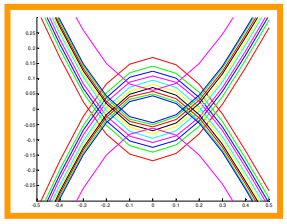
Mentor Graphics®

An Overview of High-Speed Serial Bus Simulation Technologies



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1. Overview: Traditional vs. Emerging Approaches
2. Worst-Case Bit Sequence
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Traditional TD Simulations and SerDes

- It is possible to generate eye diagrams and BER contours with normal Time Domain simulations
- Benefit:
  - all non-linear and time variant effects can be accounted for (with appropriate Tx/Rx models)
- Problem:
  - it usually takes a long time to simulate, especially with transistor level Tx/Rx models

Advanced Analysis Techniques

- Chip and CAD tool vendors developed numerous "fast" algorithms in recent years
- Benefit:
  - one can predict the eye and BER of huge number of bit transitions (millions) in a few seconds or minutes
- Problem:
  - most algorithms rely on some assumptions which are not always true or cannot always be satisfied
    - for example: using Linear, and Time Invariant (LTI) models
- Note:
  - there are specialized linear time domain simulators (using LTI assumptions) which are orders of magnitudes faster than general purpose time domain simulators

How do These "Fast" Algorithms Work?

- Most "fast" algorithms use superpositioning and statistical techniques to get quick results
- Example:
  - a worst case eye opening can be obtained from a pulse response by superimposing UI-wide slices of the waveform and summing them appropriately
  - BER curves are obtained similarly but the probability of each cursor combination is also calculated using statistical techniques

Statistical Contours

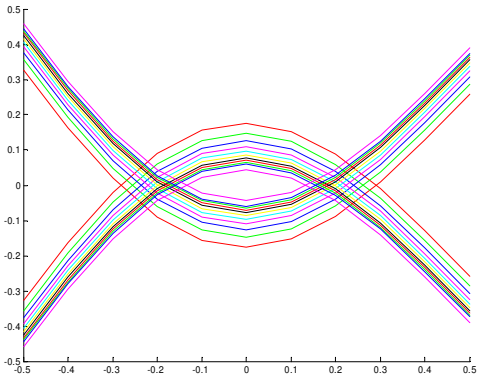


Illustration:

The innermost contour corresponds to the worst case eye opening

The worst case contour alone doesn't tell us of the probability a trace may reach a particular region

The nested contours confine the areas a trace may enter with a certain probability:
0, 1e-30, 1e-27…1e-3, etc...

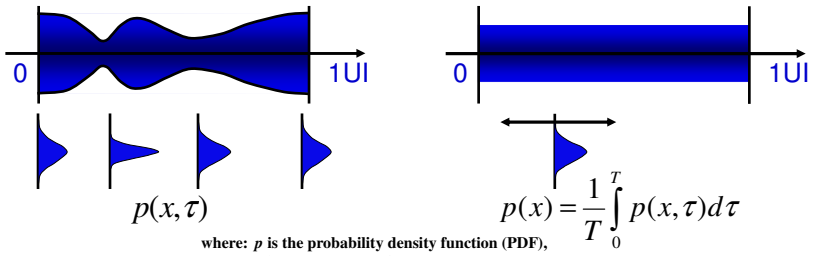
Statistical contours are what we'd get if we built the set of eye contours for increasingly longer sequences

Additional Effects

- Cross talk and jitter increases the complexity of the algorithms
  - is the aggressor signal synchronized with the victim?
  - deterministic and random jitter must be handled differently
  - etc…
- Multi-tap, equalization, clock recovery features require additional algorithms
- Encoded data needs special attention
  - 8b10b and similar encoding schemes eliminate certain data patterns and result in a more open eye naturally

Crosstalk Illustration

- Since crosstalk responses add to the self-response, the PDFs of the crosstalk responses and the self-response must be convolved
- However, the crosstalk PDFs must be defined differently depending on whether the signals of the victim and aggressor(s) are synchronized



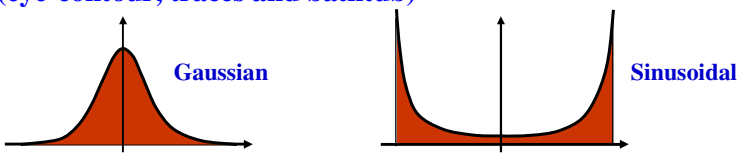
where: p is the probability density function (PDF),
x is the argument of the PDF,
τ is the synchronization variable (phase or delay)
T is the bit period

For synchronous crosstalk (left), we need to define a PDF for each slice along unit interval. For asynchronous crosstalk (right), we define uniform PDF by averaging all the crosstalk PDFs

Jitter Illustration

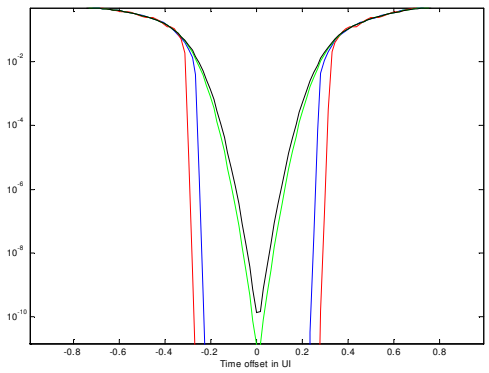
- Random jitter has unlimited Gaussian distribution. It may close the eye (at low levels of probability)
  - we characterize random jitter by defining both statistical (sigma/bit interval ratio) and frequency properties (median frequency/bit rate ratio)
- Deterministic sinusoidal jitter has 1/sqrt(1-x^2) type PDF. (Some use a double dirac delta function as a simplification).

  It may close the eye only if the magnitude is large enough
  - it is characterized by magnitude and frequency measure
- We account for jitter in statistical and time-domain simulation (eye-contour, traces and bathtub)



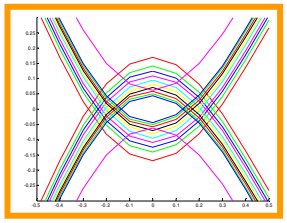
Further reading on jitter: http://www.tek.com/Measurement/scopes/jitter/55W_16146_1.pdf

Jitter Effects on Bathtub Curves



Red - no jitter
Blue - sinusoidal jitter, magnitude to bit interval ratio is 0.02
Green - gaussian random jitter, sigma to bit interval ratio 0.05
Black - both random and sinusoidal jitter

An Overview of High-Speed Serial Bus Simulation Technologies



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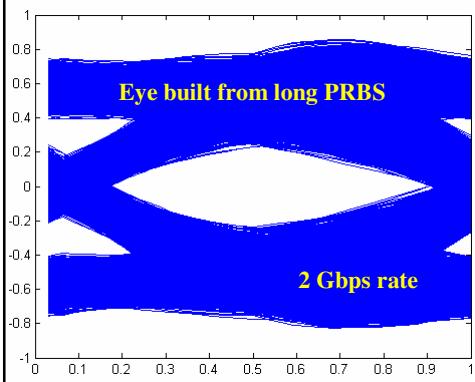
Verification at Worst Case

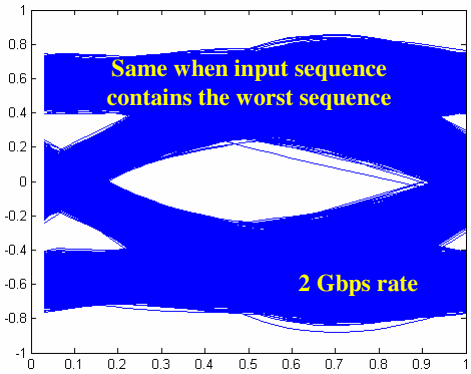
How do we Know we Have the Correct Answers?

- We can find what data sequence generates the worst eye contour and then using the same sequence we can run time domain simulations to check whether we get the same eye contour
- Problem:
  - how do we find the "true" worst case?
  - LTI models used in "fast" algorithms may give a different worst case sequence from the actual worst case sequence we would get using non-LTI models

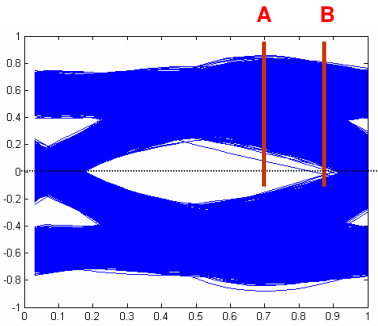
Worst Sequence (WS)

- The WS is ***unique*** for any combination of channel and pulse width
- For a given channel and pulse width, we can find a WS directly that generates the worst eye in a fraction of a second
- If WS contains 50 pulses, the probability to find WS & worst eye by applying a long random sequence would be 1 in 2^{50}, or less than 1 in $1e^{15}$
- We can also find the WS directly for encoded data sequences, such as 8b10b

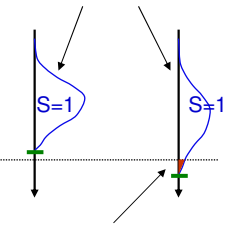




Why are the tails of the PDF so important?



PDF of eye slice at line A or B



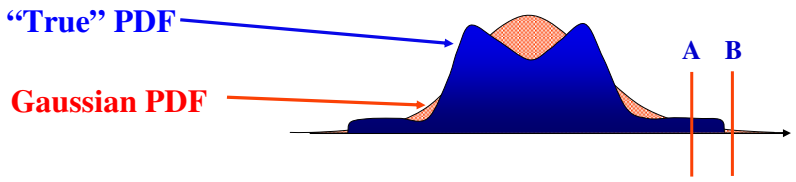
This small red area contains all of the bit errors (BE), and the lower bound on the PDF (green line) is the worst case

From here we can see how important it is to generate an accurate tail for the PDF.

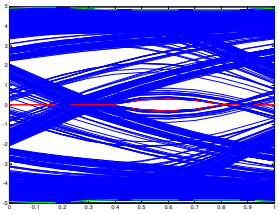
The lower bound of the PDF is determined by the worst case sequence. Without knowing this bound, an accurate BER estimation is not possible.

What does a true PDF look like?

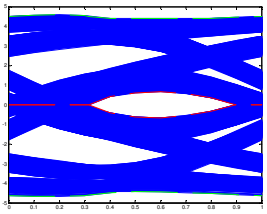
- **Two PDFs with the same expected value and similar mean deviations may produce both under- (A) and over-estimation (B) of the BER.**
  - *** The central limit Theorem states that the sum of many independent and identically distributed random variables tends to have Gaussian distribution. However, the cursors typically have very different magnitudes therefore the associated values are not identically distributed.**



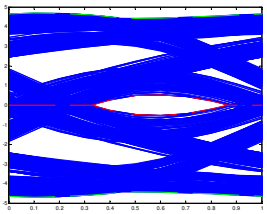
Data Encoding and WS Prediction



Unconstrained worst case sequence results in a closed eye (*pessimistic*)

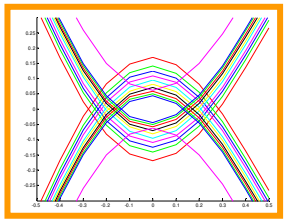


A 100k-bit long *random* 8b10b input sequence results in an eye that is better than reality (*optimistic*)



A 400-bit long *worst* 8b10b input sequence yields a *realistic* worst case eye while complying with the protocol

An Overview of High-Speed Serial Bus Simulation Technologies



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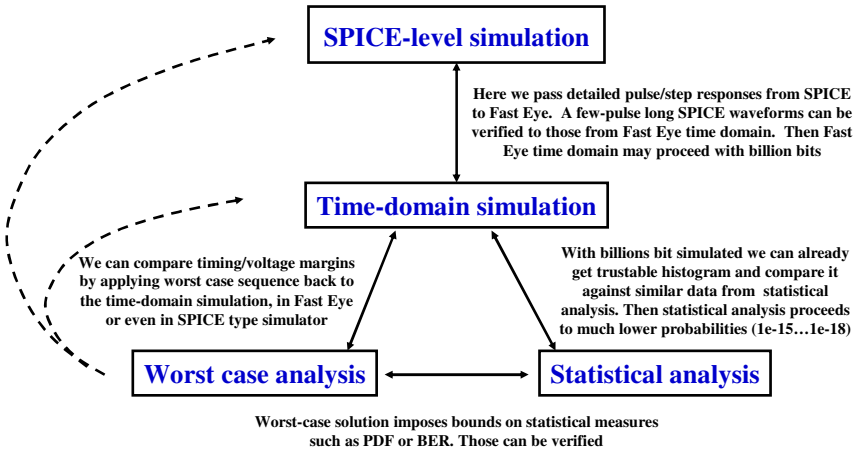
Additional Checks and Tests

- We can check the effects of non linearity by
  - overlaying the waveforms of full transistor level models with the waveforms of behavioral models used in the "fast" tools
- Comparing the results of the various "responses" can help to find the amount of non-linearity
  - rising/falling step, pulse, impulse
- We can run a huge number of bit transitions with *fast time domain* simulations and correlate its results with the results of statistical algorithms
  - remember, there are fast time domain simulation techniques (using LTI assumptions) that make trillions of bits simulations possible (in the time domain)

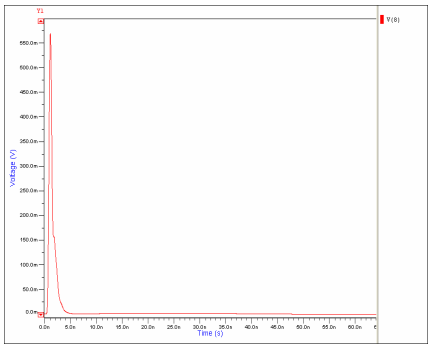
Cross-Verification Flow

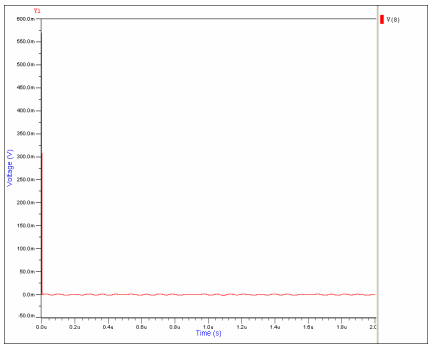


Fitted vs. Convolution-Based Algorithms

- **Problem:**
  - convolution based algorithms use impulse/pulse/step response waveforms as input
  - the length of the input waveform determines the length of the convolution and ultimately the accuracy and speed of the algorithm
- **Solution:**
  - use fitted functions
  - accuracy is independent of input waveform's length
  - no need to limit the waveform's sampling rate or length
  - unlimited dynamic range (accurate accounting for low frequency effects)
  - about 100 times faster than competing approaches

Channel with Long Impulse Response





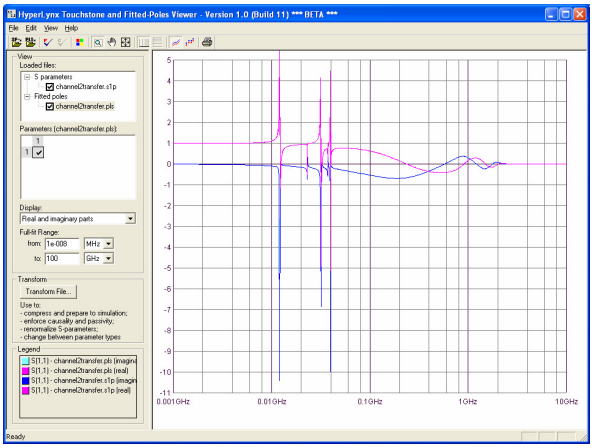
A 60 ns impulse response seems to settle after 5 ns

However, when zooming out, oscillations become visible

Convolution-based methods become inefficient with long responses

AC Analysis

Reveals Low-frequency resonances

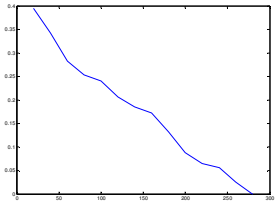


Sampled transfer function (from AC analysis with adaptive step) and fitted transfer function are in excellent agreement (error < 0.03%)

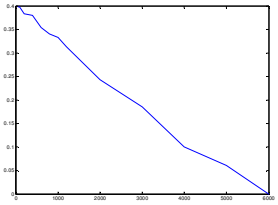
ISI May Propagate for Thousands of Bits

- Fitted data consists of 20 poles only vs. the thousands of points in the pulse response waveform that is used by the convolution based algorithm
- It is impossible to determine the required minimum length for the pulse response other than by trial and error

Eye opening vs. # of bits in the worst case sequence

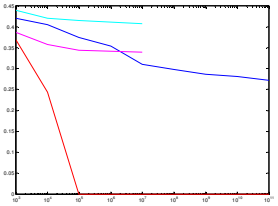


Unconstrained WS: need a length in the hundreds



8b10b WS: need a length in the thousands

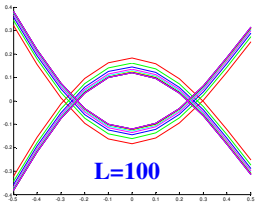
Eye opening vs. length of random sequence

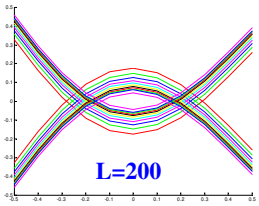


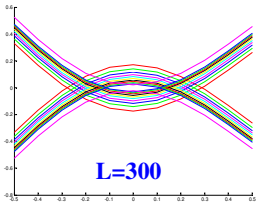
Convolution with a 100-bit WS does not show eye closing (magenta, cyan)

BER Contours for Long ISI Propagation

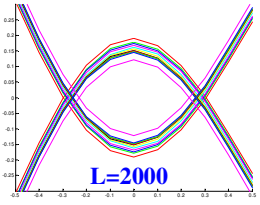
Unconstrained sequence

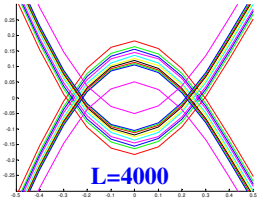


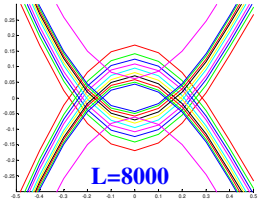




8b10b protocol







Benchmarks (Normalized to 1e6 Bits)

- Fit-based approach
  - No input jitter..... 2 sec
  - With input jitter.....12 sec
- Cursor-based approach (4000 bit long response)
  - No input jitter..... 300 sec
  - With input jitter.....4800 sec
- Summary:
  - The Ratio was 150 without and 400 with input jitter
  - However, as we saw it before from the 8b10b worst sequence, the 4000 bit pulse response is still too short to cover all of the ISI effects in this particular channel

Simulation Technique Comparison Chart

Modeling level	What do we miss?	How many bits can be simulated reasonably?
Device physical + EM models	N/A	1-10
Transistor + RLC (classic SPICE)	A few details as we covert into lumped	10^2-10^3
IBIS/VHDL-AMS + S-parameters	Some device details	10^3-10^6
Fast eye-diagram algorithms	Nonlinearity of devices	10^7-10^{11}
Direct worst sequence & BER	Jitter-ISI correlation, DFE error propagat.	infinity

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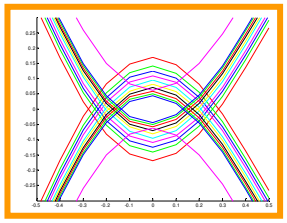

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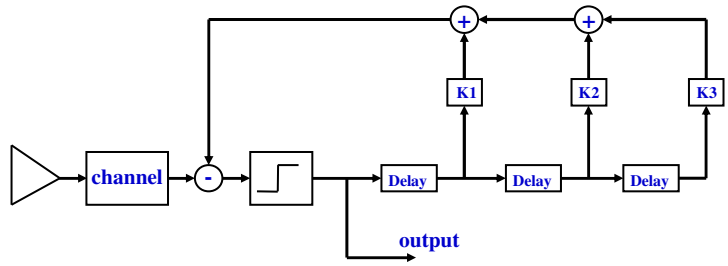
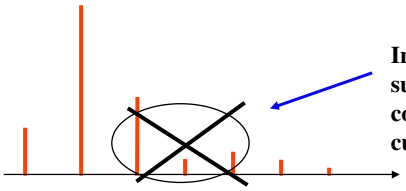
Tx and Rx Equalization

- There are two main types of equalization
  - Finite Impulse Response (FIR), also known as Feed-Forward Equalizer (FFE)
    - http://en.wikipedia.org/wiki/Finite_impulse_response
  - Infinite Impulse Response (IIR), also known as Feed-Back Equalizer (FBE)
    - http://en.wikipedia.org/wiki/Infinite_impulse_response
- Both of these can be implemented in Tx and Rx
- Decision Feedback Equalization (DFE)
  - similar to IIR (or FBE) but it has a decision block (comparator) in the loop
  - implemented in Rx only

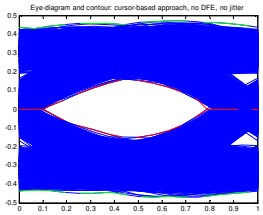
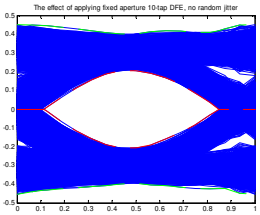
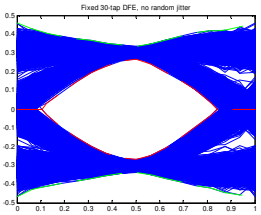
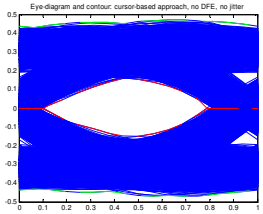
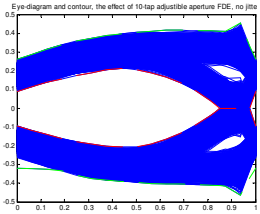
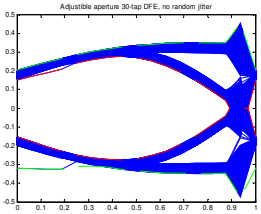
A Typical DFE Block



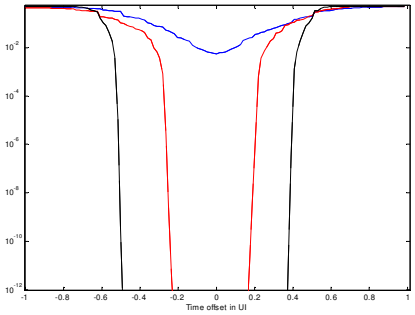


In contrast to linear equalization, DFE cannot suppress pre-cursors. However, it is capable of completely removing a number of the post cursors

Opening the Eye with DFE

	# taps = 0	# taps = 10	# taps = 30
Fixed coeff.			
Adjustable coeff.			

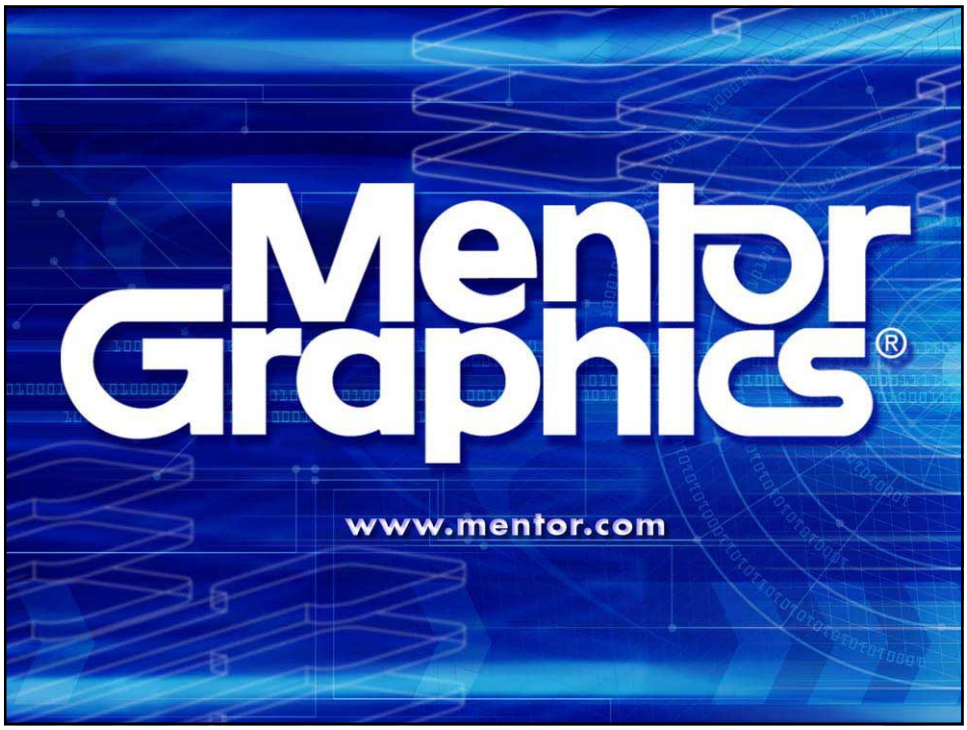
Bathtub Curves with FFE and DFE



FFE and DFE if applied together allow the best combined effect.

If necessary, we may add random jitter and build the combined eye/bathtub or investigate bit error propagation

Blue - no DFE
Red - 2 tap DFE
Black - 5 tap DFE and 3 tap FFE



Asian IBIS Summit

Modeling and Simulation for Multi-Gigabit Interconnect System

Zhu Shunlin (朱顺临) Hu Weidong Chen Songrui

High-Speed System Lab，ZTE Corporation
Zhu.shunlin@zte.com.cn

Beijing China
September 11,2007

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Agenda

- Modeling Methodologies
- Behavioral-level Interconnect Modeling
- Lab Correlation for Macromodels and S-parameters
- Eye diagram analysis and design margin budget
- Conclusions

Modeling Methodologies

- There are behavioral IBIS and structural Spice modeling for active devices. Spice model is appropriate for demanding situations, while IBIS model is often used in system and board level simulation.
- Choose an appropriate modeling method is critical for simulation. Otherwise simulation may not be accurate enough or too complex and time consuming.
- For multi-gigabit interconnect system design, behavioral-level model enables much faster simulation time than transistor-Level spice model.
- Modeling covers active devices as well as passive devices, such as package, transmission line, connector, via, and plane etc..
- Modeling methods have tradeoffs and are suitable for different applications. Multi-Gigabit Interconnect System design requires that the interconnect modeling must be valid over a wide bandwidth.
- For behavior-level modeling,correlation is necessary.

3

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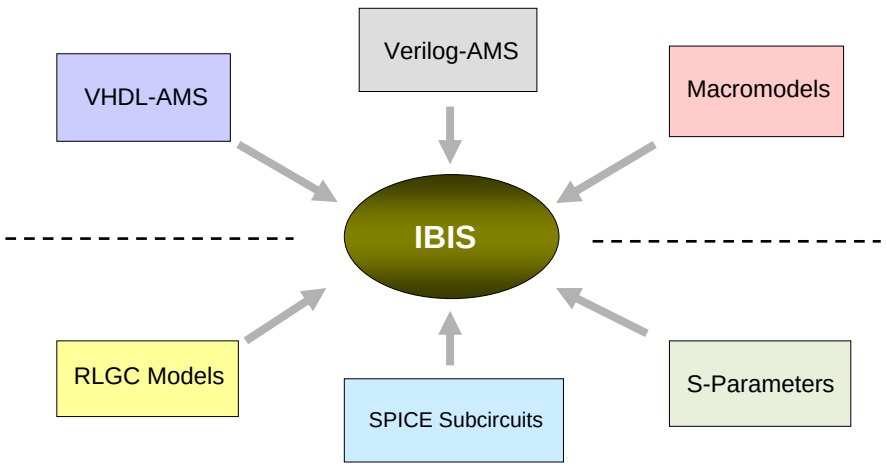
IBIS Multi-lingual Modeling



Passive interconnects modeling

4

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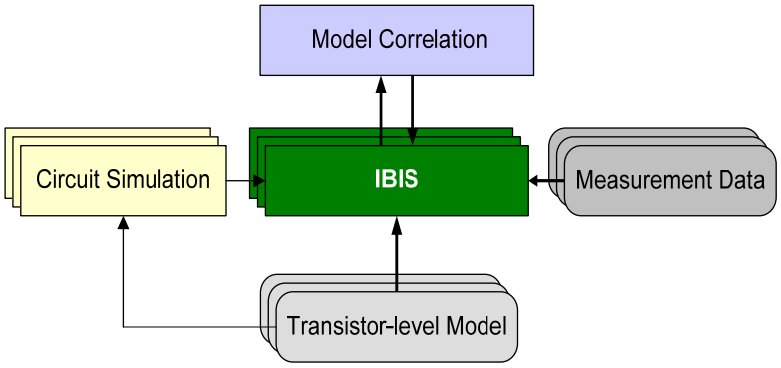
Modeling and its Correlation Flow



5

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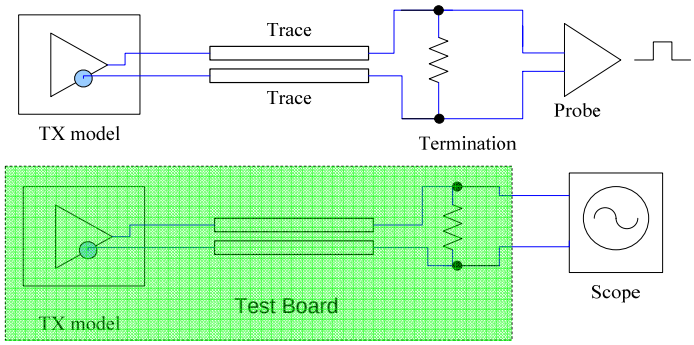
Model Validation Setup



Correlations with lab measurements and HSPICE simulations

6

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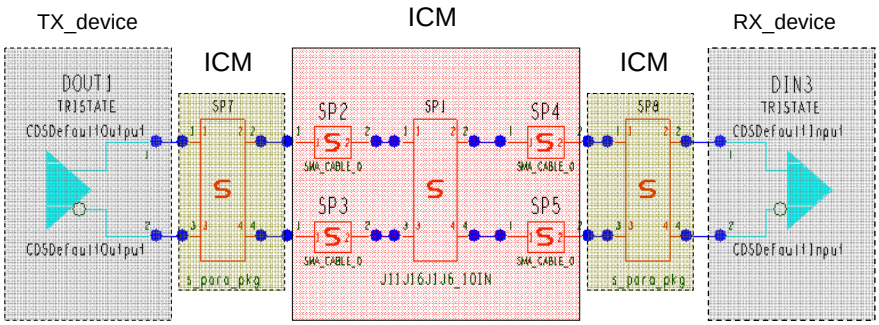
Behavioral-level Interconnect Modeling

- Transceiver Buffer Modeling
- Transceiver Package Modeling
- Interconnect (Traces, Vias, Connectors) Modeling
- Lab Correlation



Multi-Gigabit Interconnect System

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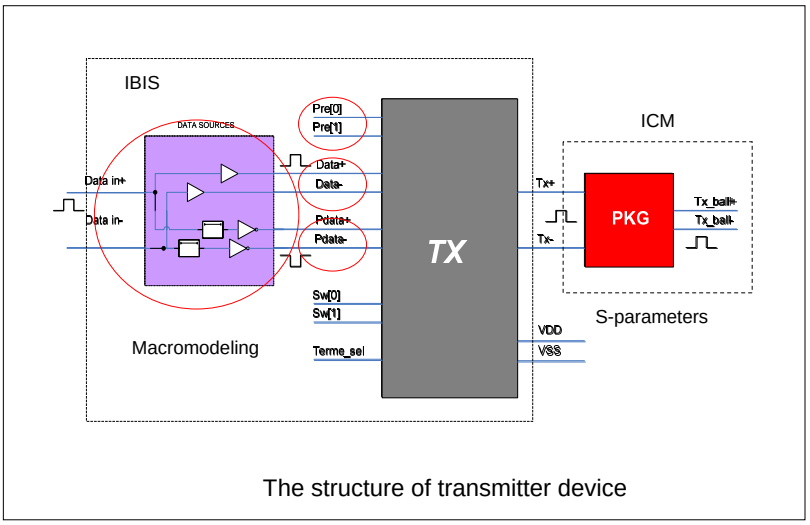
Behavioral-level Modeling of SERDES



The structure of transmitter device

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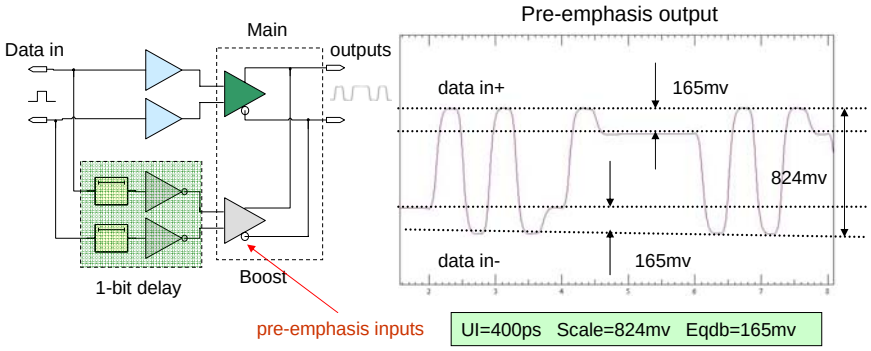
Pre-emphasis



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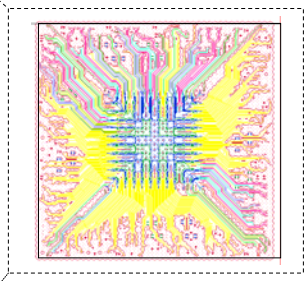
Package Modeling using S-parameters

```
("../../../Pkg_models/s_para_pkg.dml"
 (PackagedDevice
  (s_para_pkg
   (ESpice ".subckt s_para_pkg 1 2 3 4
Xs_para_pkg_4Port 1 3 2 4

.subckt s_para_pkg_4Port_Data 1 2 3 4
S1 1 2 3 4 algorithm=default
DATAPOINTS SPARAM
R=50.000000
DATAUNIT=HZ
FREQUENCY=0.000000e+000
.
. END SPARAM
.ends s_para_pkg_4Port_Data
.ends s_para_pkg_4Port" )
   (PinConnections
.
      (NumberOfPorts 4 )
   (SubType SPARAM ) ) )
 (LibraryVersion 136.2 ) )
```



S-parameters can be added to Cadence DML file.

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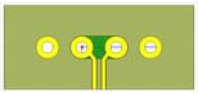
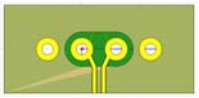
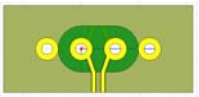
Vias Modeling and Optimization



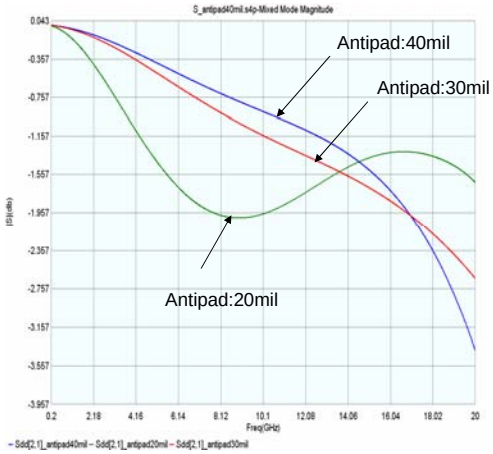
Antipad:20mil



Antipad:30mil



Antipad:40mil



11

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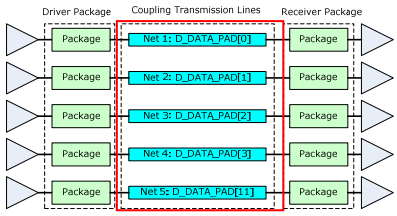
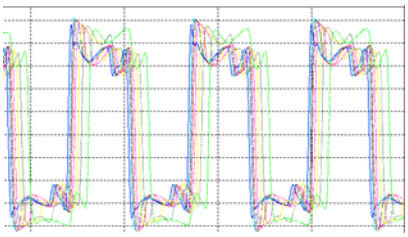
Traces Modeling and Optimization

- Extracting S-parameters using 2D/3D EM field solver





.alter change transmission line length = 38.1mm
.param len=38.1mm
.alter change transmission line length = 50.8mm
.param len=50.8mm
.alter change transmission line length = 62.5mm
.param len=62.5mm
.alter change transmission line length = 76.2mm
.param len=76.2mm
.alter change transmission line length = 88.9mm
.param len=88.9mm
.alter change transmission line length = 101.6mm
.param len=101.6mm
.alter change transmission line length = 127mm
.param len=127mm

.param lo=0v
.param hi=1.32v
.param dl=1ns
.param tr=30ps
.param ui=25.72ns
VA a 0 pulse 0 hi dl tr tr 'ui/2-tr' ui

Time domain simulation and optimization using S-parameters.

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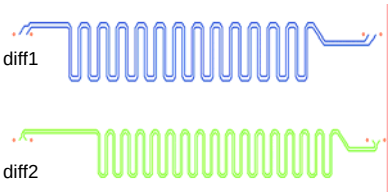
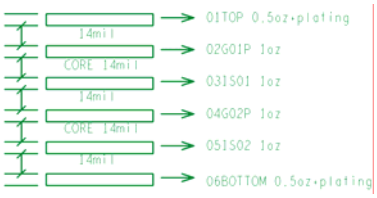
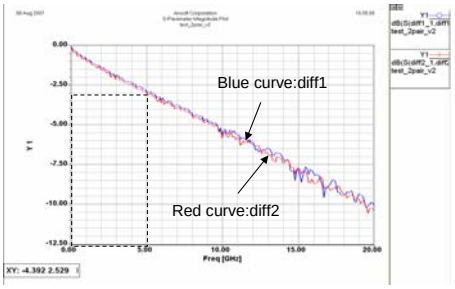
Traces Modeling and Optimization



Trace width ： 10mil

Trace width ： 8mil





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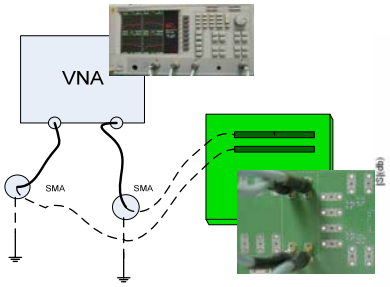
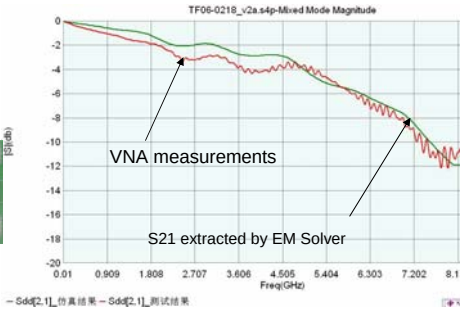
Lab Correlation for S-parameters

- Correlation based on VNA measurements





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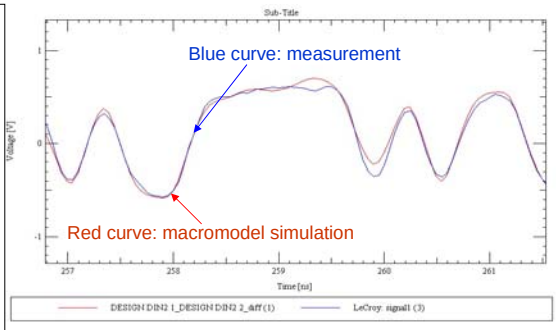
Lab Correlation for Macromodels

```
*  This is the top-level subcircuit for this
MacroModel.
*  It MUST have the same name as the
IOCell, or it will not work.
.subckt Tx nvdd outp ngnd in en  pcl  gcl
outn  BUFF=BUFF ibis_file=ibis_models.inc
+ bitp=400p
+ inv0=0
+ inv1=1
+ scale=1
+ eqdb=-0.5
+ cf0=1
+ rt=50

*  Some parameters are derived for use in
the MacroModel.
.param adj='eqdb*0.58'
.param eqf='1.0 - (10.0 ^ (adj/20.0))'
.param cf1='cf0 * eqf'
```



10% Pre-emphasis

For behavior-level modeling, correlation is necessary.

Lab Correlation Steps:
1.Simulation using HSPICE models
2.Simulation using macromodels
3.Correlate with laboratory measurement

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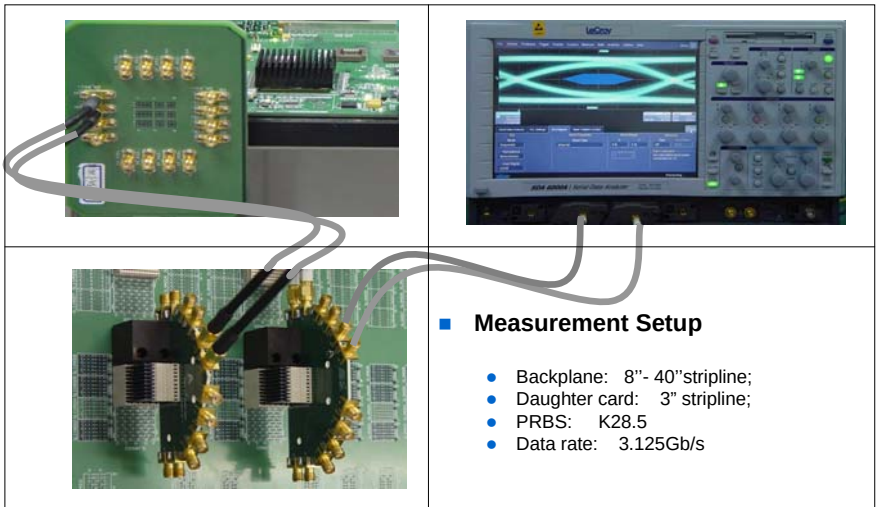
Lab Correlation and Multi-gigabit System Measurement



- **Measurement Setup**
  - Backplane: 8”- 40”stripline;
  - Daughter card: 3” stripline;
  - PRBS: K28.5
  - Data rate: 3.125Gb/s

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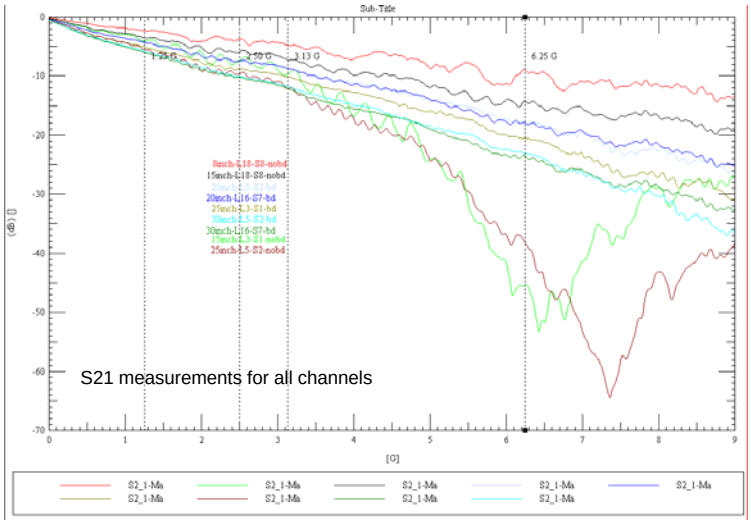
S-parameters Measurement for Channels



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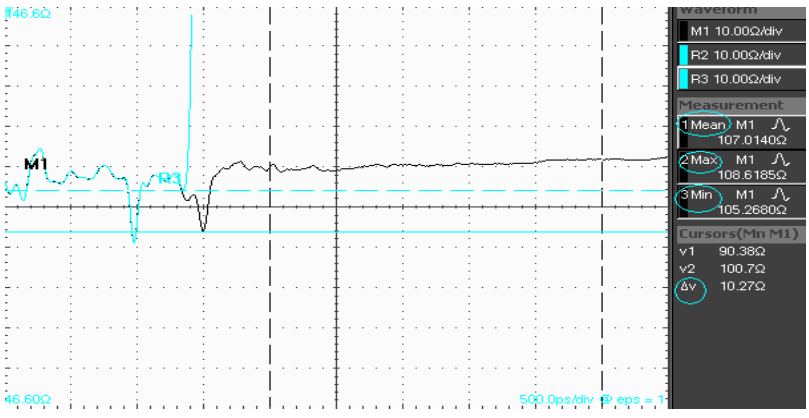
TDR Measurement



Stub Length	Mean(ohm)	Max(ohm)	Min(ohm)	ΔV(ohm)
35.3mil	107.01	108.6	105.27	10.27

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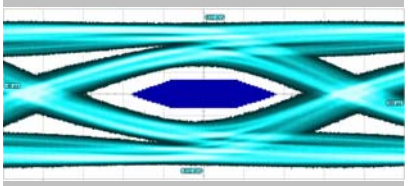
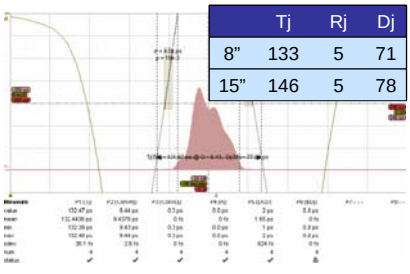
Eye Diagram Analysis and Design Margin Budget

8” stripline Stub=34mil

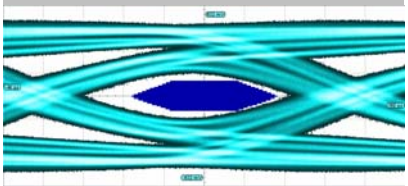


No pre-emphasis

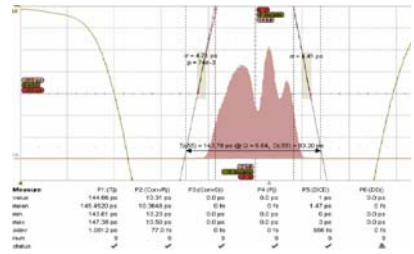
	Tj	Rj	Dj
8”	133	5	71
15”	146	5	78



15” stripline Stub=34mil



No pre-emphasis



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Conclusions

- For Multi-gigabit channel optimization, it is a good practice to use marcomodels for active devices and EM solver derived S parameter models for passive elements, provided the behavioral models have been correlated by lab measurement.
- Measurement correlated MacroModel enables much shorter simulation time than transistor-level spice model for pre-emphasis simulation and fine tuning.
- S-parameter is an accurate and efficient way for interconnect modeling. They can be used with confidence after being generated from EM solver and correlated with VNA measurement.

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Thanks
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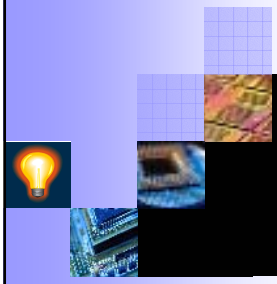


Power Delivery System Design Automation

Tao Xu
taoxu@sigrity.com

A Proposal for Specification of
System-Level Design Requirements

Asian IBIS Summit, Beijing China, September 11, 2007

SIGRITY

Agenda

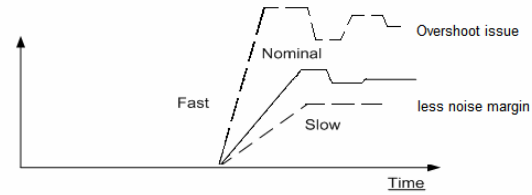
- ***PDS affects I/O performance***
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- PDS Design Flow

Why is good PDS design important?

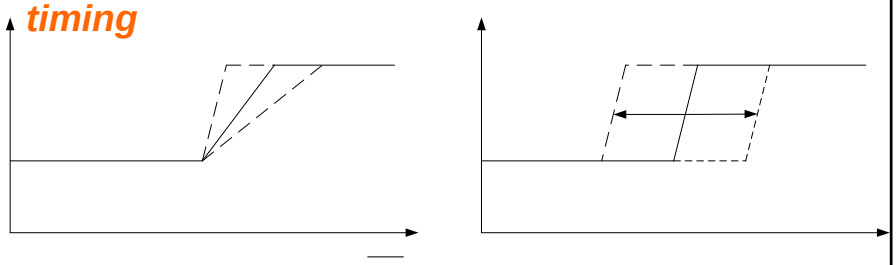
SIGRITY

PDS Affects I/O Performance

- Noise from bad PDS affects ***signal quality***



- Noise from bad PDS affects ***timing***



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Agenda

- PDS affects I/O performance
- ***Technology trends***
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- PDS Design Flow

Why is PDS design more important today?

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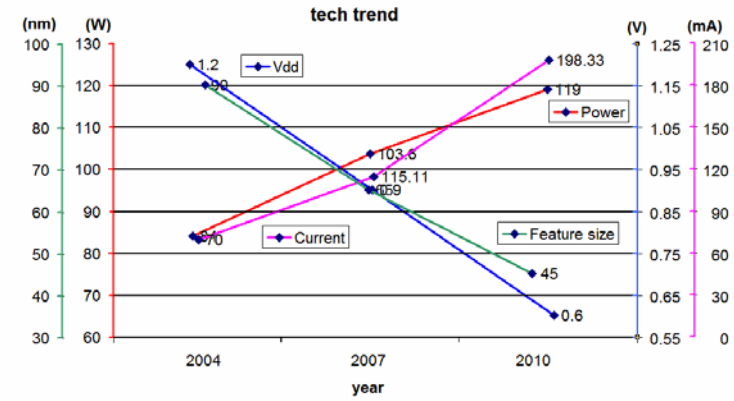
Technology Trends



- **with process size shrinking, system voltages dropping, load currents rising, and clock rates increasing,** good PDS design is now crucial to system performance.

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Agenda

- PDS affects I/O performance
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- ***Time domain analysis***
  - ***SSN simulation with IBIS***
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- PDS Design Flow

IBIS enables time domain PDS performance verification.

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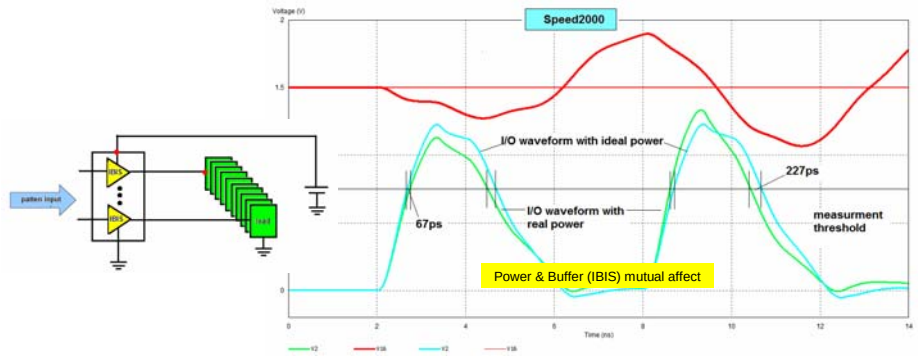
Time Domain Analysis

SSN analysis with IBIS



- IBIS provides effective ways to study how PDS interacts with signals in time domain
  - direct indication on Peak-to-Peak noise; easily know final signal waveform with real power supply models
  - rely on pattern assumptions, one simulation for one input vector
- Good way to validate the final performance of system

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Agenda

- PDS affects I/O performance
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- Time domain analysis
  - SSN simulation with IBIS
- ***Frequency domain analysis***
  - ***PDS impedance approach***
- Recent PDS design automation
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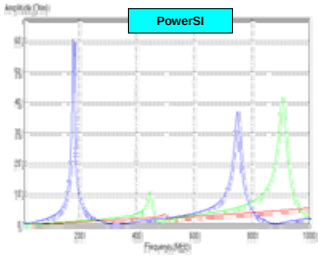
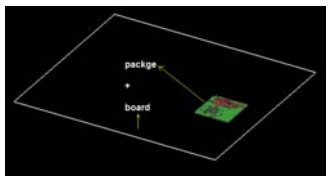
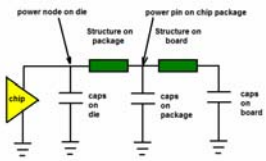
- PDS Design Flow

Frequency domain is efficient, but what impedance to specify?

Frequency Domain Analysis
PDS impedance approach







- Higher PDS performance corresponds to lower input impedance seen from the component (chip) into the system.
- PDS impedance at the chip, looking into the package or board, can be simulated accurately with EDA tools, including the effects of: VRM, board, package, and decaps
- PDS design success can be judged by comparison of impedance to a "target" or "reference" impedance (*Z_target*).

Agenda

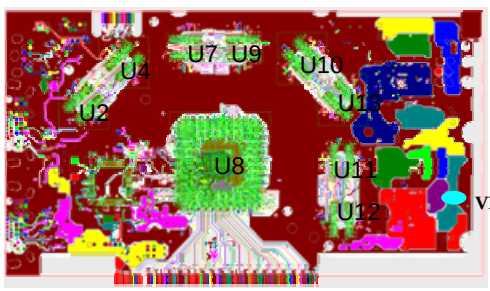
- PDS affects I/O performance
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- ***Recent PDS design automation***
- Target Impedance in IBIS
- PDS Design Flow

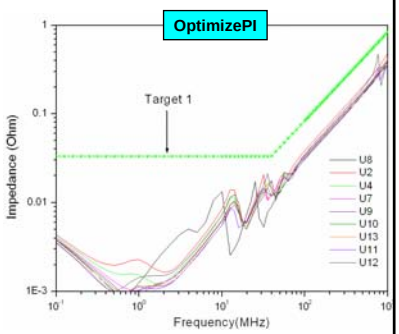
New PDS analysis and optimization

Automated PDS Design Flow
- Performance and Cost Optimization

- Input for PDS design
  - Physical: stack-up, layout, decap library
  - Electrical: initial decap placement or Z_target
- Analysis and Optimization tasks for PDS
  - Frequency domain, full-wave PDS analysis
  - Optimization of decap placement/selection
- Results of automated EDA design flow
  - Lowest manufacturing cost for specified system-level performance
  - Highest performance for a range of cost
  - Reduced design area
  - Interactive cost-performance tradeoffs

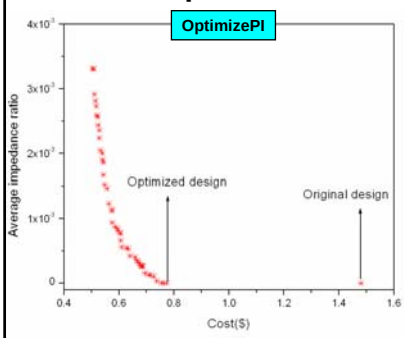
Case 1

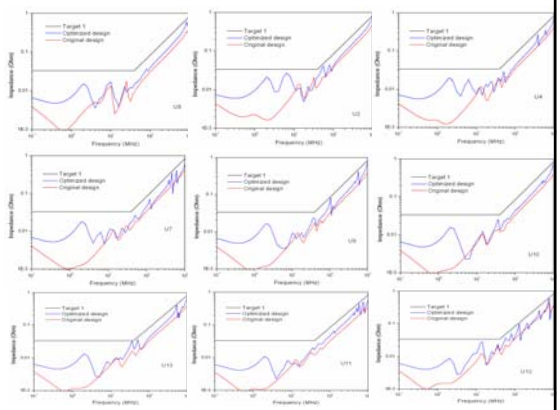




- Nine component impedances control the optimization process.
- Green curve is user-specified Z_target.
  - original design used as a reference.

Optimum Performance vs. Cost



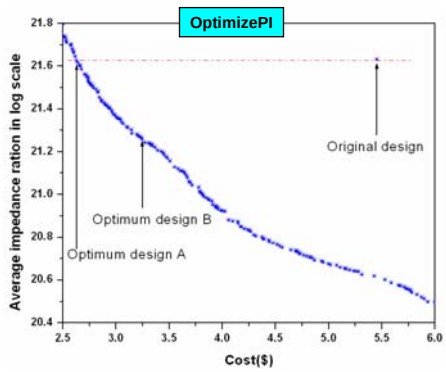


Design	Cost
Original	1.48
Optimized	**0.77**

- Cost reduced by half, while maintaining the required system-level performance.
- Component-level performance details are shown.

Case 2

- Eleven component impedances control the optimization process
- No Z_target was provided by component manufacturer
- Original design impedance used as a reference
- Interactive cost-performance tradeoffs are examined



Capacitor Configurations

	Average Impedance Ratio	Cost($)
Original Design	**21.633**	**5.49**
Optimum Design A	**21.628**	**2.67**
Optimum Design B	**21.270**	**3.32**

Optimum Design A

Cap ID	Qty
1	1
2	3
3	5
4	13
5	5
6	45
20	4
23	4

Cost: **$2.67**

Optimum Design B

Cap ID	Qty
1	1
2	2
3	2
4	3
5	6
6	47
10	3
20	8
23	4

Cost: **$3.32**

Original Design

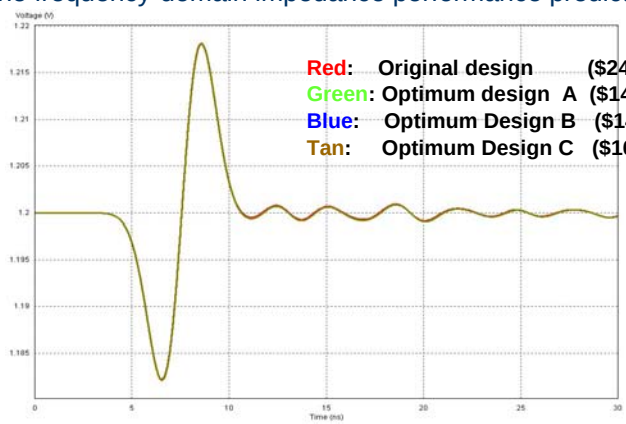
Cap ID	Qty
1	32
3	2
7	30
9	2
11	1
23	3
20	14
27	1
28	8

Cost: **$5.49**

- Interactive cost-performance tradeoffs quickly determine designs with both better performance and lower cost.

Case 3 - Time Domain Verification

- Frequency-domain optimization was performed first.
- All devices driven simultaneously with Gaussian current pulses.
- Time domain voltage noise performance provides an alternative mean of verifying the frequency-domain impedance performance prediction

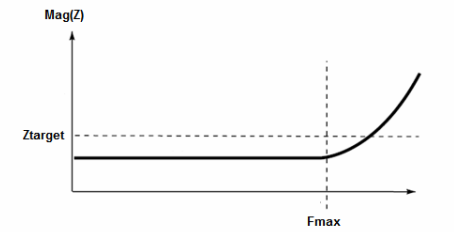


Agenda

- PDS affects I/O performance
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- ***Target Impedance in IBIS***
- PDS Design Flow

Where to get Z_target to define PDS design goals?

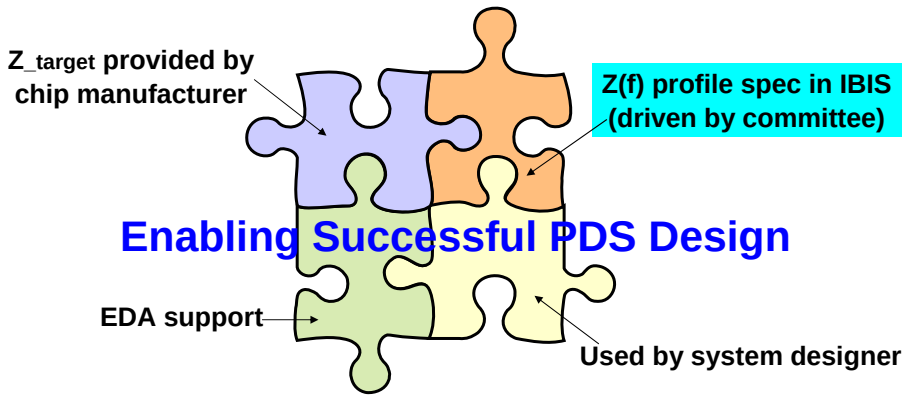
Target Impedance



$$Z_{target} = \frac{V_{dd} \times 0.05}{I \times 50\%}$$

- Z_target from simple calculation
  - more detailed and accurate simulations are usually available
- Z_target from reference design (*chip manufacturer*)
  - I/O design has applied and can generate Z_target requirements
  - Available EDA tools are able to extract Z_target of reference and demo designs
- Z_target from previous successful design (*system manufacturer*)
  - Meet or beat actual PDS impedance of previous generation system

Proposal for Z_target Specification in IBIS



A win-win-win scenario:

- System designers require Z_target to define PDS design goals.
- Chip manufacturer's existing component-specific PI knowledge can be leveraged in a standard manner.
- EDA vendors can provide support of Z_target specification in IBIS to enable automated and successful PDS design.

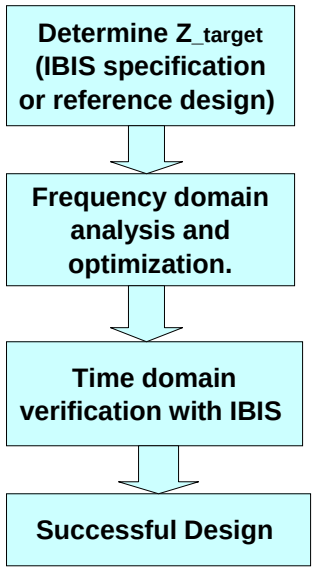
Agenda

- PDS affects I/O performance
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- ***PDS Design Flow***

Automated PDS Design Flows.

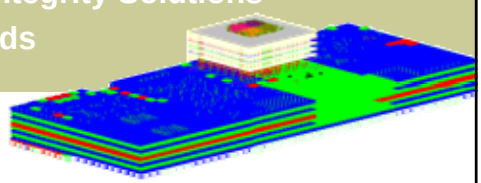
PDS Design Flow

- Z_target profile definition should be added to IBIS.
  - leverages existing knowledge of chip vendors.
  - enables system design goals to be defined.
- EDA vendors will quickly apply this information with PDS analysis and optimization tools.
- Verification with IBIS in time domain is suggested, applying actual current profiles.



Thank You!

Advanced Power and Signal Integrity Solutions for Chips, Packages and Boards



02. August 2007

IBIS4.2 FOR DDR2 TIMING ANALYSIS

September 11, 2007
Asian IBIS Summit, Beijing China

Guan Tao
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HUAWEI TECHNOLOGIES Co., Ltd.

HUAWEI

Outline

- **New technologies have brought challenges to IBIS model**
- **DDR2 timing analysis**
  - The read cycle timing analysis
  - The write cycle timing analysis
- **IBIS4.2 model meets the challenges**

Challenges

- **More SI and timing problems emerge as the rate of bus increases , these problems can be eliminated by new techniques :**
  - ODT (On Die Termination);
  - OCD (Off-chip Driver).
- **Challenges of DDR2 modeling:**
  - How to model the ODT circuit;
  - How to use the slew rate table.

  The setup and holdup time are varying with the slope of the signal in DDR2.

DDR2 Timing Analysis Method

A proper method of a DDR2 timing analysis should contain the following essentials:

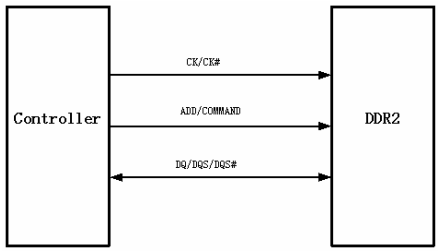
- **Seeking for a balance between simulation efficiency and waveform quality.**
- **The parallel simulation and crosstalk can be processed by EDA platforms.**
- **The EDA platform can process the PRBS (pseudo-random bit sequence) code;**
- **Topology 、matching and transmitter/receiver buffer can be automatically analyzed**
- **The settle and switch delay between standard load and practical load can be considered;**
- **Influence of voltage and temperature can be included in the simulation;**
- **The ODT circuit and slew rate table can be considered.**

Current simulation method is not good enough to support the features listed here!

Timing Relationships of DDR2

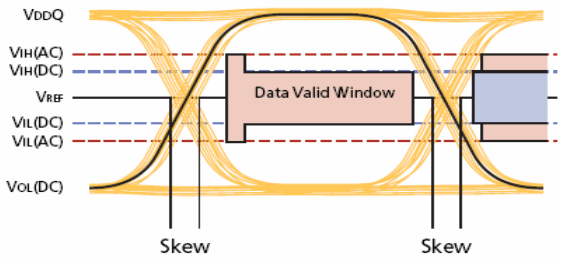
Three timing relationships in DDR2 timing analysis:

- **ADDRESS、COMMAND and CK/CK#;**
- **DQ and DQS/DQS#;**
- **DQS and CK/CK#.**



Data Valid Window

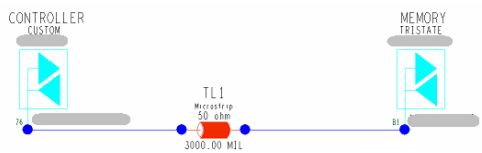
The SSTL_18 is intended for DDR2 interface application.



DDR2 Timing Analysis with IBIS 3.2

Following is an example of timing analysis of DQ and DQS. The ADDRESS/COMMAND timing analysis is similar.

- **The topology of DQ/DQS is point to point feature.**
- **The models of CONTROLLER and MEMORY are IBIS3.2 model.**

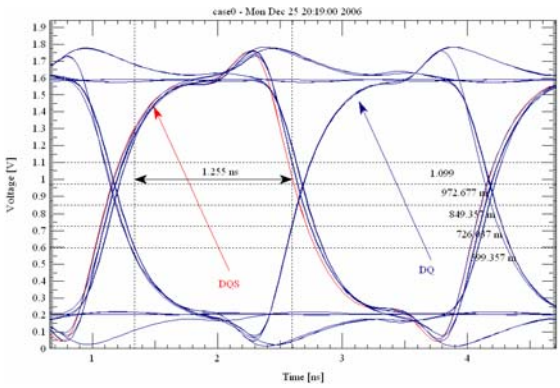


Read Cycle Timing Analysis (fast)

In fast mode, the simulated eye diagram of read cycle is as follow.

data valid window :1.255ns

waveform distortion: 0.245ns

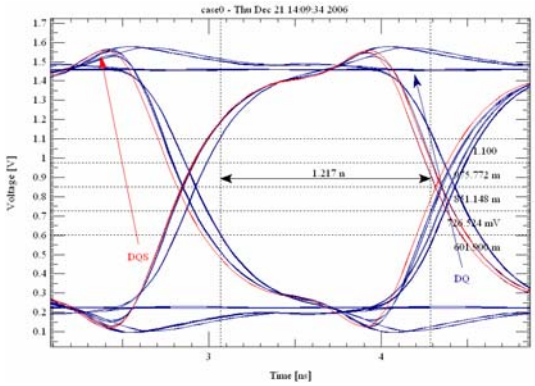


Read Cycle Timing Analysis (slow)

In slow mode, the simulated eye diagram of read cycle is as follow.

data valid window: 1.217ns

waveform distortion :0.283ns



Read Cycle Timing Calculation

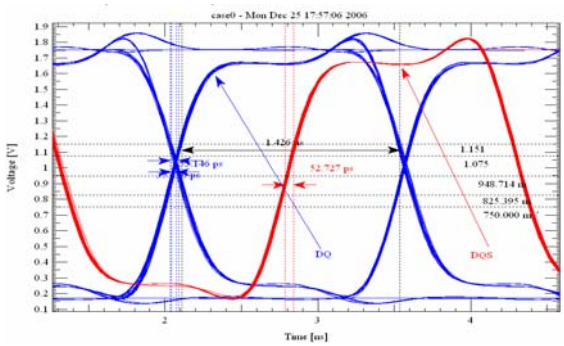
	TimingParameter	Time (ps)	Description
Memory Parameter	tHP	1500	Ideal clock
	tDCD	150	Output clock (includingmemory clock duty cycle distortion)
	tDQSQ	240	Skew between DQS and DQ from memory
	tDHS	340	Data hold skew
Waveform distortion	tSD	283	Waveform distortion
Controller Distortion	TSAMP_BUFIO	350	The minimal data width required in the IOB of FPGA
	DELAY Tap Jitter	336	The jitter induced by delay tap
Timing Margin	Timing margin		

Write Cycle Timing Analysis (fast)

In fast mode, the simulated eye diagram of write cycle is as follow.

data valid window :1.426ns

waveform distortion :0.074ns

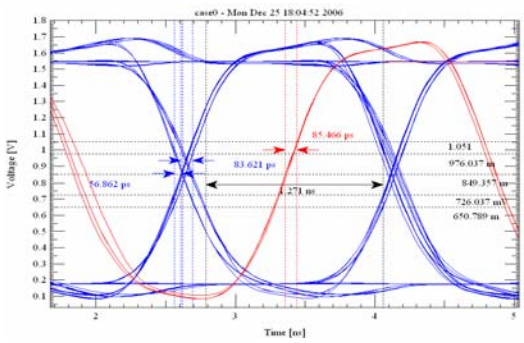


Write Cycle Timing Analysis (slow)

In slow mode, the simulated eye diagram of write cycle is as follow.

data valid window:1.271ns

waveform distortion: 0.229ns



Write Cycle Timing Calculation

	Timing Parameter	Time (ps)	Time (ps)	Time(ps)
Controller Timing Parameters	T_{CK}	3000		
	T_{DCD}	150		
	T_{DATA_OUT}	1350		
	$T_{Package\_skew}$	30	30	30
	Tjitter	50	50	50
	Tclock _skew_ max	50	50	50
	Tclock _out _phase	140	140	140
DDR2 Memory Parameters	*Tsetup*	200	200	
	Tholdup	238		238
Waveform Distortion	*Tsd*	229		229
Timing Margin	Total uncertainties		470	737
	Timing margin	143		

Drawbacks

- **Inefficient**

The method of DDR2 timing analysis above is a time-consuming and manual procedure. Simulations are run on each net to generate eye diagrams, through which signal integrity and timing characteristics of an individual net can be evaluated.

- **Sometimes meaningless**

The simulation is meaningless, when the margin is negative.

The DDR2 timing analysis is made under absolute worst-case conditions. Owing to the worst-case prediction of all parameters applied to a single net, the margin analysis method described above may predict a failure when in fact the actual design is sound.

Deficiencies of IBIS3.2

IBIS3.2 model has the following several deficiencies for timing analysis of DDR2:

1. The IBIS3.2 model is not programmable, so that it is difficult to implement a flexible simulation and process slew rate table automatically.

2. The IBIS3.2 model is not flexible enough to accommodate new techniques.

3. The IBIS3.2 model is a parameterized model, not able to process the simulated waveforms.

IBIS4.2 Model Meets the Challenges

Randy Wolff 、Gary L. Pratt. P.E and their collaborators solve these problems in IBIS4.2 model. IBIS4.2 is an extension of IBIS3.2.

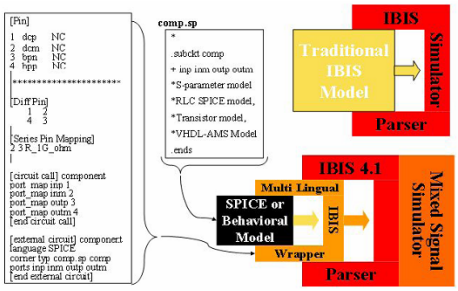
- **IBIS4.2/AMS multiplexer permits the simulator to select between an IBIS model with ODT and one without ODT;**
- **Supports seamless switch of read cycle and write cycle simulation;**
- **Through running a section of VHDL code, the simulator is able to measure the slope of relevant signals;**
- **Automatically determines the corresponding value in the slew rate table;**

It's a good solution to problems we are facing now.

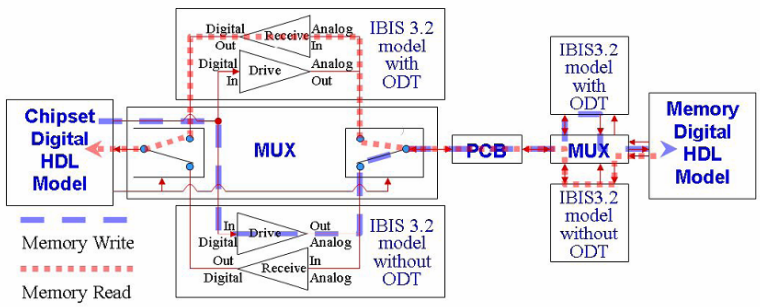
IBIS 4.2 for Timing Analysis

Using the IBIS4.2 model ,we can make the following measurements automatically:

- **Automatic overshoot area measurements**
- **Automatic setup and holdup timing measurements**
- **Slew-dependent timing calculation**



One Solution of ODT Circuit

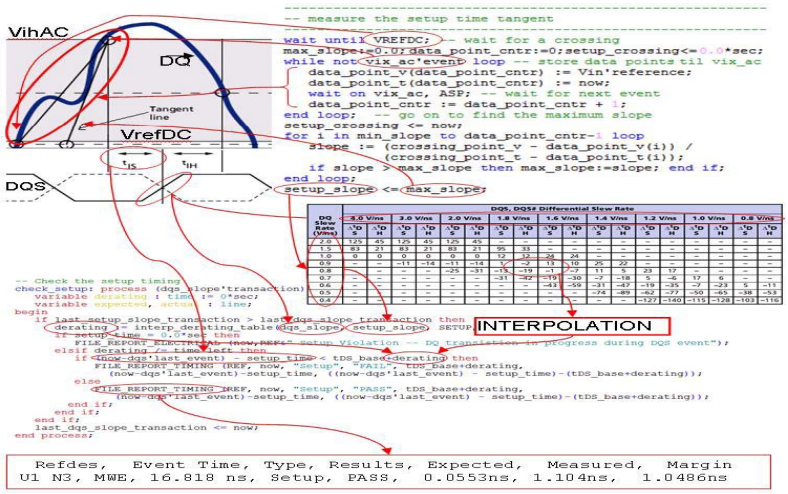


VHDL-AMS Code for Multiplexer

```
if ODTmux = '1' use  -- Connect the ODT driver
   v_a_signal == v_ODT_a_signal;
   i_a_signal == -i_ODT_a_signal;
   -- Keep the non-ODT driver C_comp charged
   v_noODT_a_signal == a_signal'reference;
else  -- Connect the non-ODT driver
   v_a_signal == v_noODT_a_signal;
   i_a_signal == -i_noODT_a_signal;
   -- Keep the ODT driver C_comp charged
   v_ODT_a_signal == a_signal'reference;
end use;
break on ODTmux;

-- ODTmux bit chooses between ODT and non-ODT digital receiver
d_receive <= ODT_d_receive when ODTmux='1' else noODT_d_receive;
-- ODTmux bit chooses between ODT and non-ODT digital driver
-- Set non-used driver output to Z to keep it charged
ODT_d_control <= d_control when ODTmux='1' else 'Z';
noODT_d_control <= d_control when ODTmux='0' else 'Z';
```


Slew Rate Table Calculation



Output Results

Electrical results

Time	Receiver Pin(s)	Net(s)	Violations/Errors
0.003 ns	U1 J7 H8	MDQS0 and MDQS0#	Violation - DQS Failed to Meet TDQSx Minimum Pulse Width Limit
0.003 ns	U1 J7 H8	MDQS0 and MDQS0#	Violation - DQS exceeded VIXACMIN at Differential Crossing
40.92 ns	U1 E7 D8	MDQS1 and MDQS1#	Violation - DQS Non-Monotonic
41.04 ns	U1 J7 H8	MDQS0 and MDQS0#	Violation - DQS Non-Monotonic
58.407 ns	U1 G1	MDQ11	Setup Violation -- DQ transistion in progress during DQS event
58.407 ns	U1 E3	MDQ1	Setup Violation -- DQ transistion in progress during DQS event

timing results

Refdes/net	Event Time	Type	Results	Expected	Measured	Margin
U1 T3 MA5	30.579 ns	Setup	PASS	0.146751 ns	1.071 ns	0.924249 ns
U1 N3 MWE	78.579 ns	Setup	PASS	0.160759 ns	1.113 ns	0.952241 ns
U1 T8 MA4	72.579 ns	Setup	PASS	0.145127 ns	0.402 ns	0.256873 ns
U1 R2 MA10	15.579 ns	Setup	PASS	0.156969 ns	0.423 ns	0.266031 ns
U1 P7 MCAS	95.43 ns	Hold	PASS	0.266398 ns	0.276 ns	0.009602 ns
U1 P7 MCAS	21.996 ns	Hold	PASS	0.249038 ns	0.282 ns	0.032962 ns
U1 P1 MBA2	15.579 ns	Setup	PASS	0.139647 ns	0.417 ns	0.277353 ns
U1 U2 MA7	15.579 ns	Setup	PASS	0.119884 ns	0.399 ns	0.279116 ns

Warnings/Errors results

RefDes/Net	Warning/Error
U1 T3 MA5	Warning - Runt Pulse at time: 71688
U1 R2 MA10	Warning - Runt Pulse at time: 71730
U1 G3 MDQ15	Warning - Excessive Hold Slope at time: 72480
U1 E1 MDQ14	Warning - Excessive Hold Slope at time: 72495
U1 E9 MDQ8	Warning - Runt Pulse at time: 112983
U1 F2 MDQ10	Warning - Runt Pulse at time: 113013
U1 J9 MDQ1	Warning - Excessive Setup Slope at time: 125673
U1 K2 MDQ7	Warning - Excessive Setup Slope at time: 126852

Advantages

- **Flexible**

  The IBIS4.2 model is programmable, so that the model is flexible and appropriate to new technology.

- **Real-time**

  The margin is properly measured on every edge in the method of timing analysis, which takes the influence of slew rate table into consideration.

- **Automatic**

  The procedure of timing analysis is automatic and prompt. The output results are reasonable and simple.

Requirements from System Vendors

The IBIS4.2 model is a good solution to the high rate bus of memory timing analysis,

1. There is still few EDA vendors to fully support the IBIS4.2 model;

2. Due to no spice2AMS tool in place, the majority of IC vendors do not have a schedule to provide the IBIS4.2 model;

3. The results are consistent , when we use the same IBIS model on different platforms;

4. The IBIS model should be accurate enough to depict electrical characteristics of chip properly;

5. Building the package model should be paid more attention to as the bus rate increases;

The development of IBIS needs our efforts!

Validation for IBIS Models

Asian IBIS Summit
Beijing China
September 11, 2007

Lance Wang lwang@iometh.com
Xinjun Zhang xjzhang@iometh.com
Benny Yan zyan@iometh.com
IO Methodology Inc.

Agenda

- IBIS Quality Issue
- One test result
- How to improve current IBIS model qualities?

Agenda

- **IBIS Quality Issue**
- One test result
- How to improve current IBIS model qualities?

IBIS (I/O Buffer Information Specification)

- Public Standard
  - ANSI
  - EIA-656-A
- Well known behavioral buffer model specification
- There are about 300+ companies provide IBIS models, thousands of companies use IBIS for their designs

IBIS faces quality issues

- IBIS model quality is poor in general
  - "70% of IBIS models on the web are JUNK" quoted a few years ago
  - "More than 50% of IBIS models are not accurate" quoted recently
  - "the IBIS simulation results are different using different simulators" quoted a long time ago. But it is still TRUE ……
- How to solve these issues?

The things we are doing

- IBIS Committee efforts
  - Quality Sub-committee
  - Model Review Sub-committee
  - Educational seminars done by companies and individuals
- But, the MOST Important thing for your design and analysis is:

  Validate the IBIS models before your design and analysis

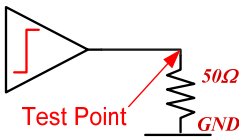
Agenda

- IBIS Quality Issue
- **One test result**
- How to improve current IBIS model qualities?

Test Implementation

For validating C_comp and Ramp data with VT curves

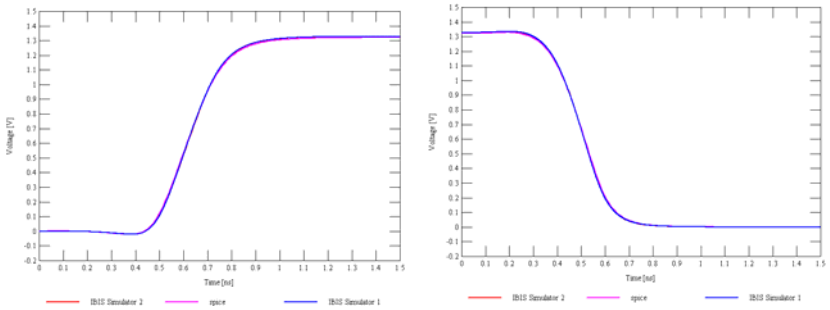
- Output buffer with 50 Ohm resistor to GND
- 0.1ps rising and falling edge for stimulus
- Probe the output pad of driver
- Keep C_comp constant, sweep Ramp data
- Keep Ramp data constant, sweep C_comp
- Simulate in two different IBIS Simulators



Correlation spice and IBIS model with 4 VT

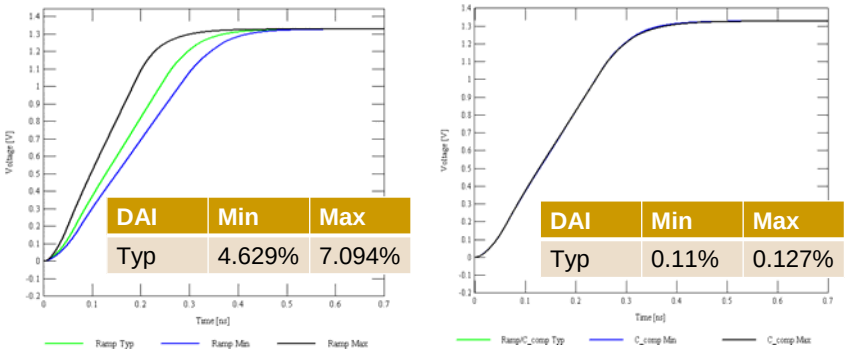
The Max DAI between two simulators is 0.525%

Showed perfect matching



IBIS Simulator1 /wo VT (Rising)

- Keep C_comp constant, sweep Ramp data, the maximal DAI is 7.094%
- Keep Ramp data constant, sweep C_comp, the maximal DAI is 0.127%
- At rising edge, Ramp data is the main factor in Simulator1

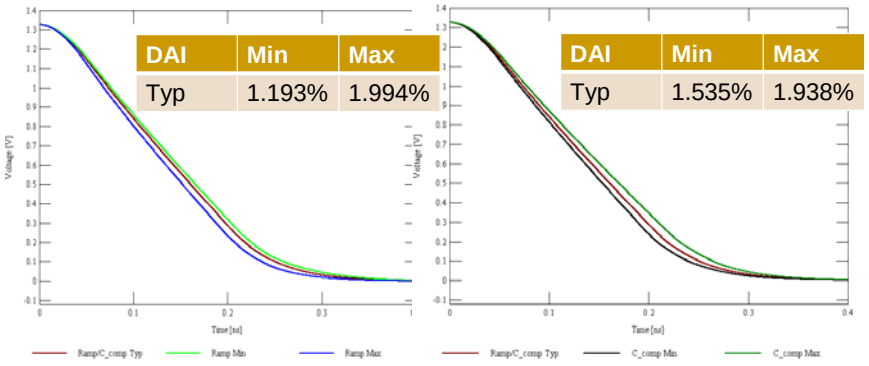


DAI	Min	Max
Typ	4.629%	7.094%

DAI	Min	Max
Typ	0.11%	0.127%

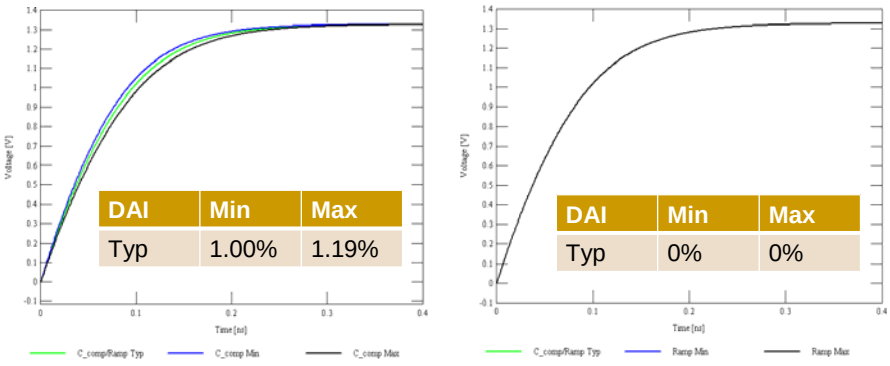
IBIS Simulator1 /wo VT (Falling)

- Keep C_comp constant, sweep Ramp data, the maximal DAI is 1.994%
- Keep Ramp data constant, sweep C_comp, the maximal DAI is 1.938%
- At falling edge, Ramp and C_comp play almost the same role in Simulator1



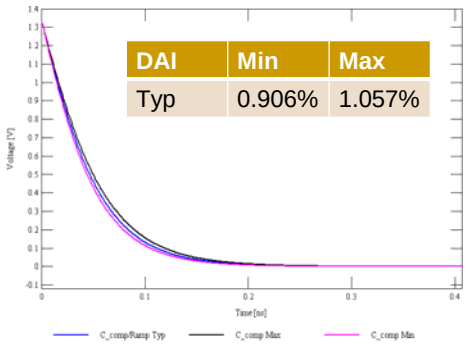
IBIS Simulator2 /wo VT (Rising)

- Keep Ramp constant, sweep C_comp, the maximal DAI is 1.19%
- Keep C_comp constant, sweep Ramp, there is NO difference
- At rising edge, C_comp is the main factor in Simulator2

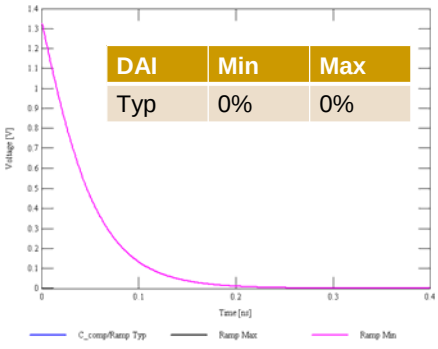


IBIS Simulator2 /wo VT (Falling)

- Keep Ramp constant, sweep C_comp, the maximal DAI is 1.057%
- Keep C_comp constant, sweep Ramp, there is NO difference
- At falling edge, C_comp is the main factor in Simulator2

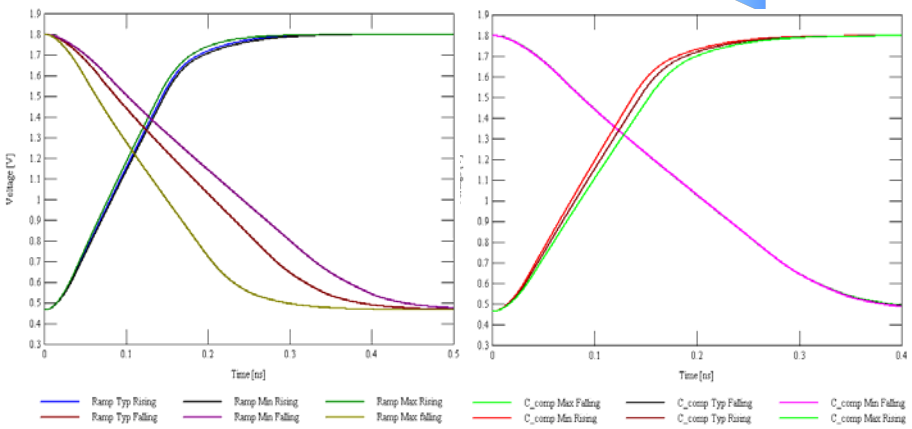


DAI	Min	Max
Typ	0.906%	1.057%



DAI	Min	Max
Typ	0%	0%

How about 50 Ohm resistor to VCC in the same simulations?



The effect is reversed for the previous simulations in Simulator1 while Simulator2 has the same effect as the previous simulations.

Test Conclusions

- Simulators are giving the different results due to different implementations for IBIS simulations
- Another words, even the same IBIS model, you may get different results when you used the different simulators

Agenda

- IBIS Quality Issue
- One test result
- How to improve current IBIS model qualities?

IBIS Validation Process

- Steps
  - Develop a proper validation method
  - Contact vendor(s) to get the Golden source (results)
  - Run the tests using IBIS simulators
  - Compare the results
  - You are lucky if the results are aligned with each others
  - Or, contact vendor(s) if the results are not correlated – both simulator and model vendors are needed
  - *You might have to repeat many steps to get it done*
- Concerns? Problems?

Concerns and Problems in IBIS Validation Process

- Too long
  - Average is more than 8 business days
- Not accurate enough
  - Lack of the knowledge for the device technologies, IBIS and EDA tools
- This is a Model Librarian job
  - Not all SI engineers have enough model and tool knowledge for this process
  - Not every company has the model librarian

IBIS Certification Program (IBISCP)

A Vendor Neutral Program

- Motivations
  - Provide a solution for IBIS users to have GOOD models for their high-speed designs
  - Provide a solution for IBIS vendors to have GOOD models for their customers
- Target
  - To have IBIS as a primary industry standard on behavioral IO modeling for High-Speed Signal Integrity analysis
  - To allow designers make faster, cheaper and more reliable electronic products

IBISCP: Purposes and Goals

- Provide a professional IBIS model validation results to IBIS users and vendors
- Provide a multi-simulator validation results to IBIS users, IBIS vendors and EDA vendors
- Provide a on-going validation process based on requests from IBIS users and IBIS vendors
- Provide statistical reports about IBIS feature usages, feedbacks and enhancement requests to IBIS Open Forum
- Provide IBIS quality reports to IBIS Open Forum, IBIS Quality Sub-committee and IBIS Model Review Sub-committee
- Provide IBIS feature support reports to EDA vendors


IBISCP
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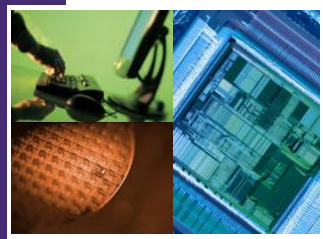
IBIS Algorithm Including Reactive Loads



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September 11, 2007

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Outline

- Accuracy Issue of Reactive Loads
  - Concept of Reactive Loads
  - Related Presentation Before
  - Example of the Issue
- IBIS Algorithm with R/L/C/V_fixture
  - Algorithm Steps and Equations Involved
  - Recall the Example with Above Algorithm
- Conclusions

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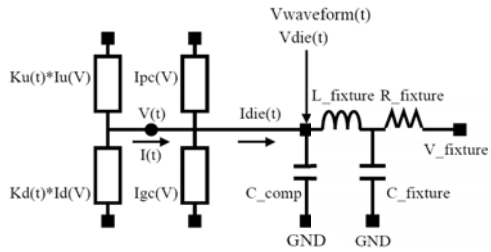
Reactive Loads



The general Reactive load in this presentation is the **R/C/L/V_fixture** load shown in the diagram

The presentation does not consider additional components **L/R/C_dut** defined in the IBIS standard (not shown) to mimic the package model of a specific pin

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Related Presentation in Past Meetings

- Arpad Muranyi: http://www.vhdl.org/pub/ibis/summits/feb06/muranyi2.pdf
  Deals with a series capacitor (C_load) in series with R_load.
  Found difficulties applying the 2EQ/2UK process.

- Manfred Maurer: http://www.vhdl.org/pub/ibis/summits/apr07/maurer.pdf
  Considered using R_fixture, L_fixture, C_fixture by superposition.
  Not yet resolved for series C_load with R_load problem.

- Bob Ross: http://www.vhdl.org/pub/ibis/summits/feb06/ross1.pdf
  Suggested using C_fixture (if handled by IBIS processing algorithm) for buffer peaking to compensate for connected buffers and C_comp loading interactions.

- Michael Mirmak: http://www.vhdl.org/pub/ibis/summits/apr04/mirmak2.pdf
  Considered C_comp extraction issues when buffers are connected and interact.

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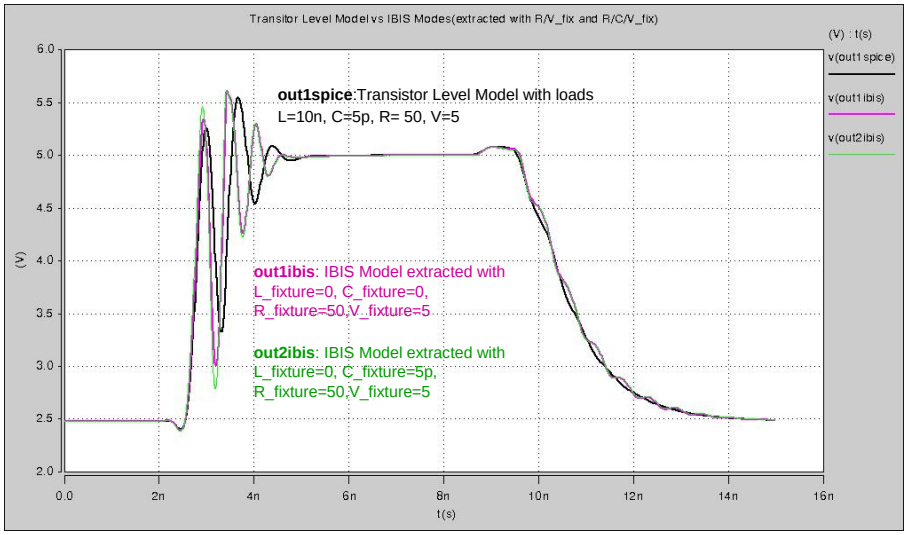
Example:

Accuracy Issue with L, C, R, V Loads



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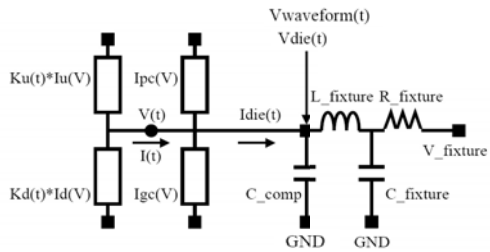
IBIS Algorithm with R/L/C/V_fixture



Two steps to get scaling coefficients of PU, PD (Ku,Kd)

1. Get $I_{die}(t)$ by VT waveforms, C_comp and *_fixture
2. Use the well known 2EQ/2UK algorithm

$$0 = Ku(t) * Iu(V_{wfm1}(t)) + Ipc(V_{wfm1}(t)) - Kd(t) * Id(V_{wfm1}(t)) - Igc(V_{wfm1}(t)) - Idie(V_{wfm1}(t))$$
$$0 = Ku(t) * Iu(V_{wfm2}(t)) + Ipc(V_{wfm2}(t)) - Kd(t) * Id(V_{wfm2}(t)) - Igc(V_{wfm2}(t)) - Idie(V_{wfm2}(t))$$

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IBIS Algorithm with R/L/C/V_fixture (Cont.)

- Compute $I_{die}(t)$ of preceded step 1

$$I_{die}(t) = I_{Ccomp}(t) + I_{Lfix}(t)$$

$C_{comp} * dV_{wfm} / dt$

Differential equations:

$$dI_{Lfix}(t)/dt = (V_{Cfix}(t) - V_{wvf}(t)) / Lfix$$

$$dV_{Cfix}(t)/dt = ((Vfix - V_{Cfix}(t)) / Rfix - I_{Lfix}(t)) / Cfix$$

With initial values:

$$V_{Cfix}(0) = V_{wvf}(0)$$

$$I_{Lfix}(0) = (Vfix - V_{wvf}(0)) / Rfix$$

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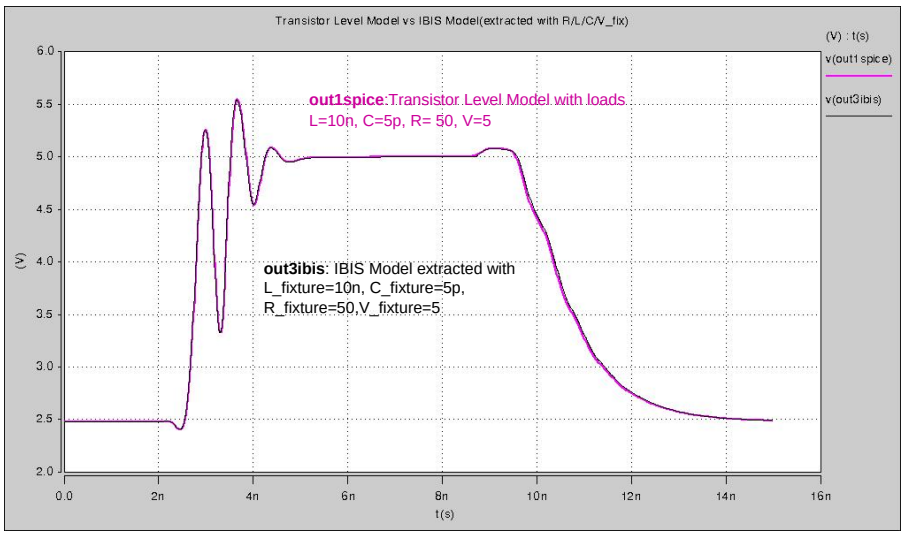
Example:

Fitting Result if Model is Extracted with all L,C,R,V fixtures



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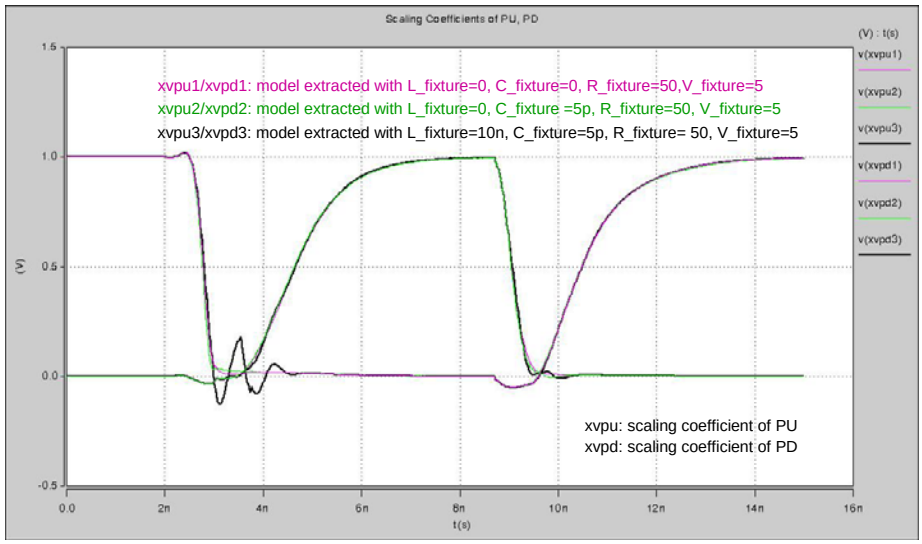
Substantial Accuracy Improved



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Conclusions

- For reactive loads, IBIS model result can be perfectly fitting with Transistor level model if proper R_fixture , V_fixture, C_fixture , L_fixture are used in model extraction
- The proper values of them are based on practical loads

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Special Thanks to Bob Ross

For the help of providing research background, review and good suggestions for this presentation

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INVENTIVE

Understanding and Using ICM Models

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Asian IBIS Summit,
Beijing China,
September 11, 2007

Topics

- IBIS ICM Model Introduction
  - What's IBIS ICM Model
  - What can we do with ICM model
  - ICM model structure
- ICM model usage scenario
  - Black box model
  - Package model
  - S-parameter support
  - ICM swath model support
- Summary

IBIS ICM

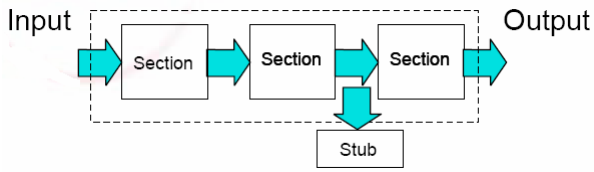
- **IBIS Interconnect Modeling Specification**
  - ICM stands for InterConnect Modeling
- **The goal of the ICM**
  - Provide a better, *more accurate*, non-proprietary interconnect data exchange format
    - Faster & ***accurate*** simulations
    - Smaller file size
- ICM history
  - Final Draft 1.0 released publicly May 16, 2003
    - See IBIS web site under “Connector Info”
  - Version 1.1 “ICM” specification approved in July 2005

What can we do with ICM model

- ICM supports models for Connectors, PCB traces and IC-Packages
- ICM can include
  - RLGC Matrices
  - Swaths
  - S-parameters

Section of ICM

- Each section is made up of a Single Line Model (SLM) or Multiple Line Model (MLM)
- A matrix section is a set of tables of numerical values that represent the electrical relationships between all conductors of a given geometry



- S-parameter can be used in place of RLGC matrix

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Section: ICM core unit structure

```
/--[Begin ICM Section]
|   |--[Derivation Method]
|   --[Resistance Matrix]
|       /-- [Bandwidth]
|       |-- [Frequency]
|       \-- [Row]
|   --[Inductance Matrix]
|       /-- [Bandwidth]
|       |-- [Frequency]
|       \-- [Row]
|   --[Conductance Matrix]
|       /-- [Bandwidth]
|       |-- [Frequency]
|       \-- [Row]
|   --[Capacitance Matrix]
|       /-- [Bandwidth]
|       |-- [Frequency]
|       \-- [Row]
|
|   --[ICM S-parameter]
|        File_name
|        Port_assignment
|
\--[End ICM Section]
```

- Sections are basic units and core structure of one ICM model

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ICM model usage scenario

- ICM models can be used during pre-layout and post-layout analysis
- Two cases are presented
  - Case1: In pre-layout simulation, ICM model is used as a Black box model in a topology
  - Case2: In post-layout simulation, ICM package model is assigned to a component IBIS model on the PCB

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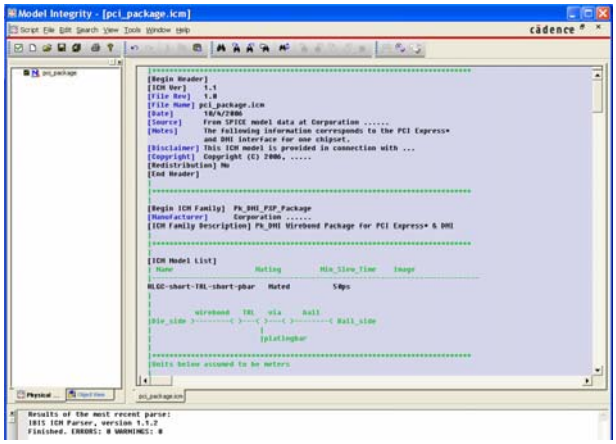
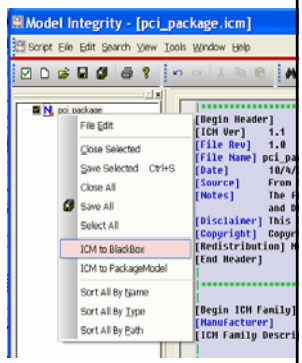
Example: ICM model of PCI express package





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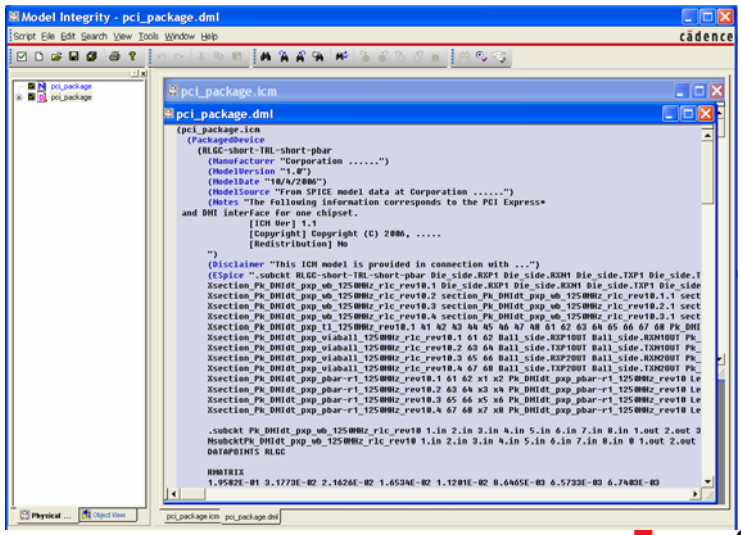
Device model case (Black box model)



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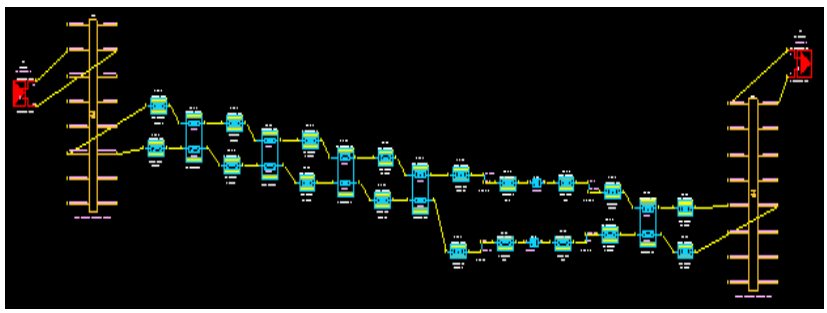
Case 1: ICM acts as device model (Black box model)

- The package ICM model has been wrapped into one black box model, just like one connector



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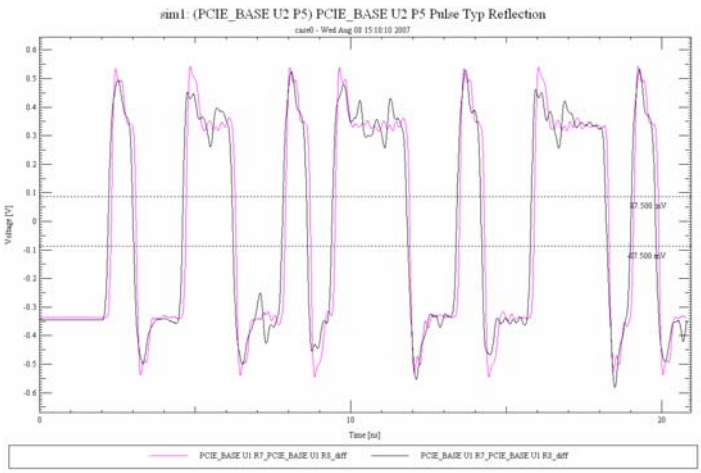
Case 1: Simulation Results comparing (with/o ICM model)



The pink line represents the simulation with ICM model

The black line represents the simulation without ICM model

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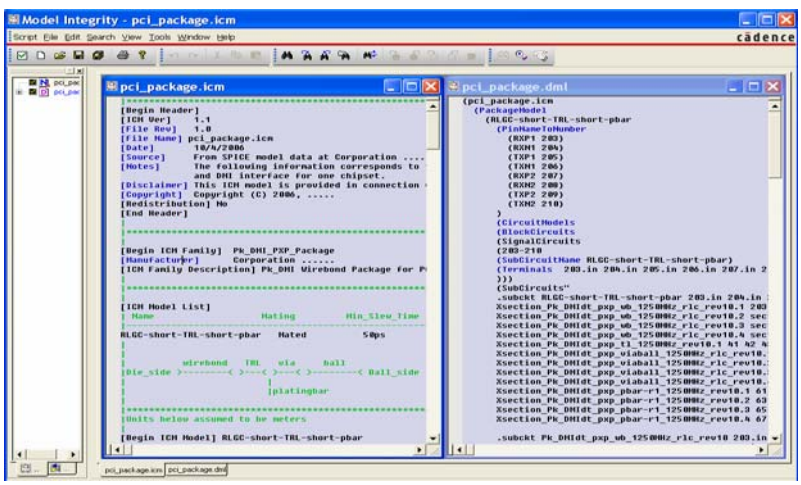
Package model case (associating with its corresponding IBIS model)



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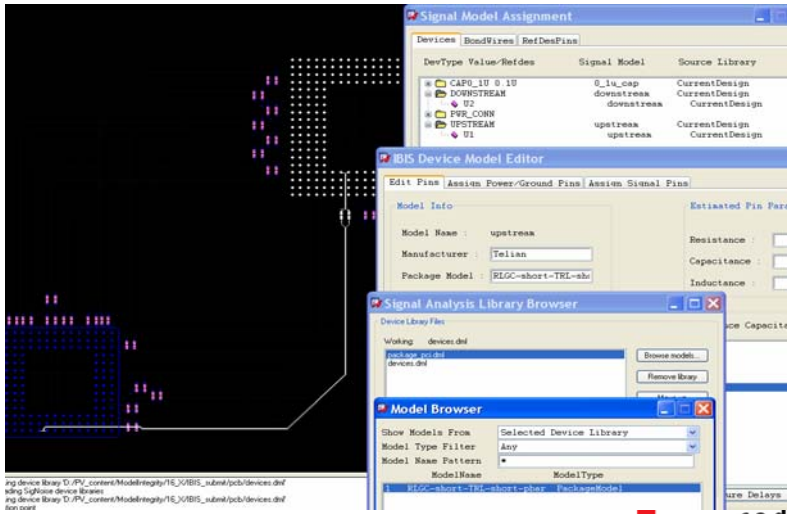
Case 2: ICM acts as package model



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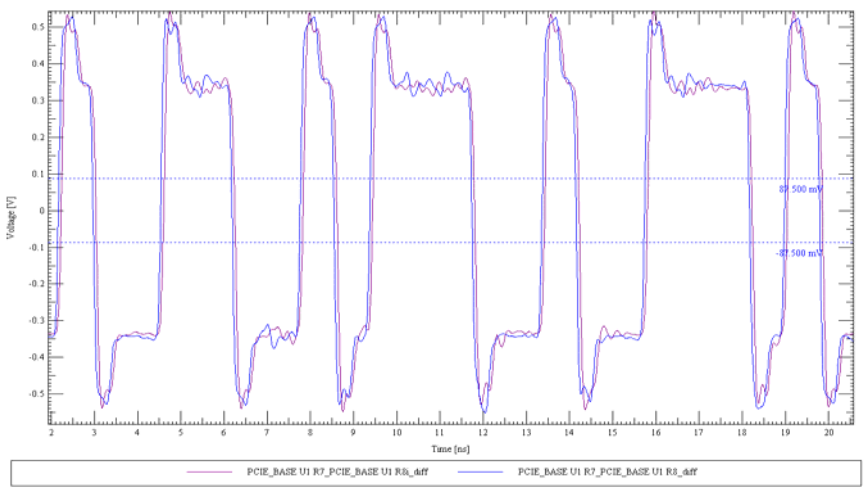
Case 2: Simulation Results comparing (with/o ICM model)



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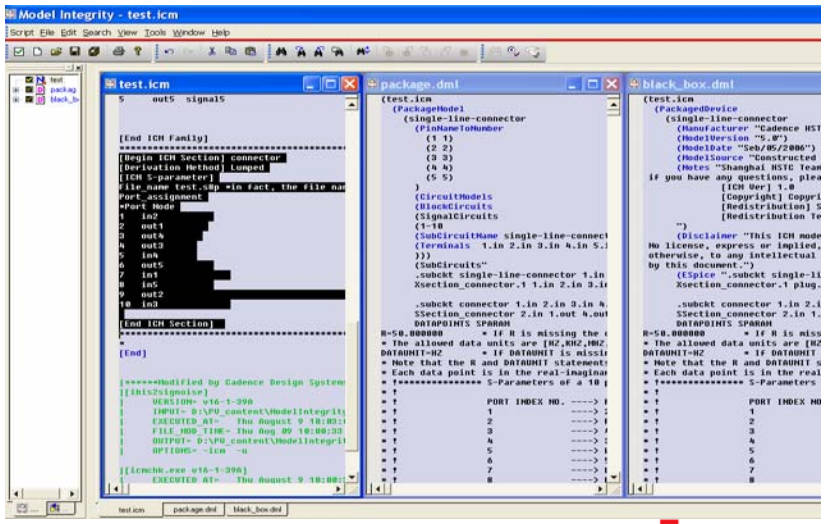
S-parameter support



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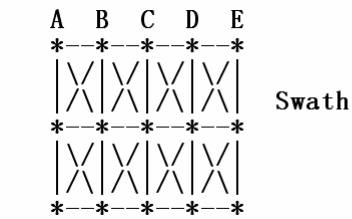
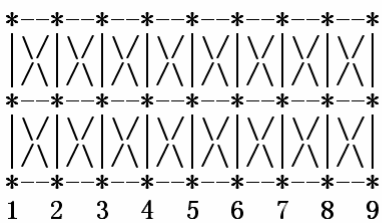
ICM Swath model support





- Swath model
  - Is a method of using a small matrix section to define a much larger and variable size section of a connector
  - This facilitates faster simulation, smaller file size, and makes the creation of a family of connectors much easier

Full Interconnect

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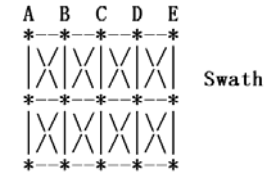
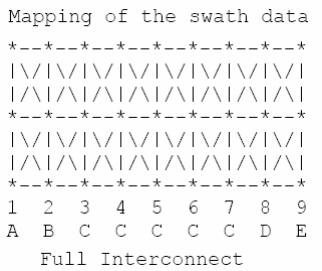
Expanding the swath matrix





- **Three methods can be used to expand a swath matrix into a full-sized interconnect**
  1. Centering the Swath around the pins of interest
  2. Expansion and Centering: Expanding the Swath matrix into a larger sized Swath matrix and centering it about the paths of interest
  3. Expansion to Full Sized Interconnect: Expanding the swath matrix to the full sized interconnect matrix

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Summary

- **ICM models offer open, non-proprietary way for vendors to provide interconnect models to their customers**
- **ICM models can be accurate for simulation at higher frequencies *they can include coupling***

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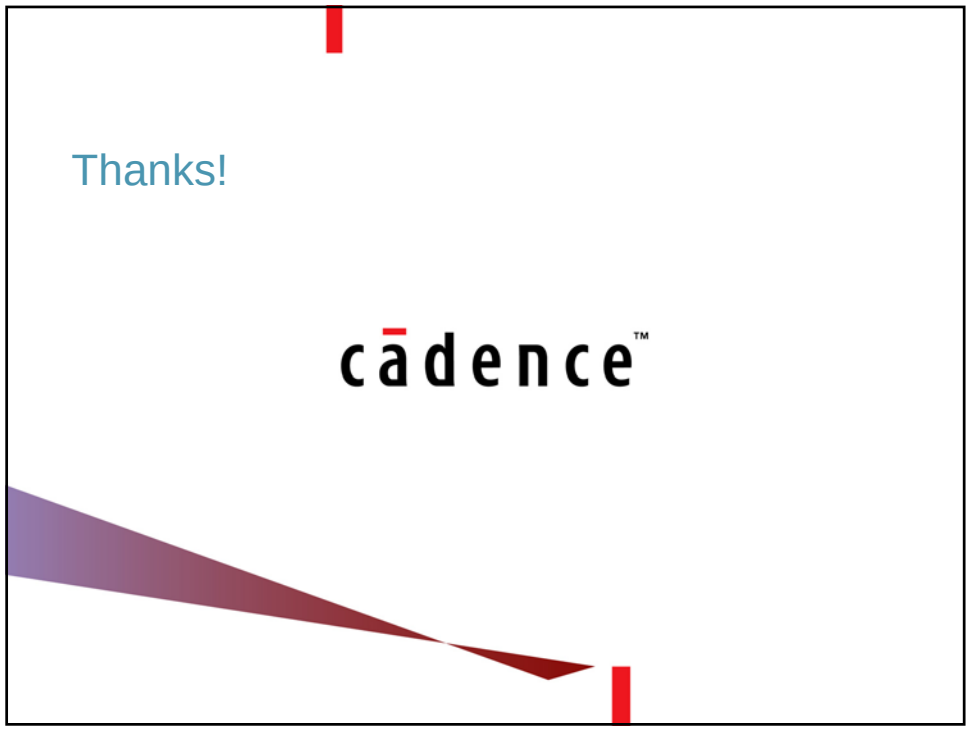
Thanks!
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Using S-Parameters for High Performance Simulation

Asian IBIS Summit
Beijing China
September 11, 2007

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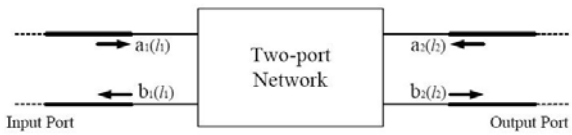
Ansoft Beijing Office

ANSOFT

What's S-Parameter

- S-parameter-- Scattering parameter

S Parameters



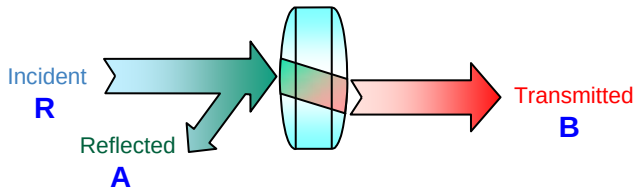
Return Loss $S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}$ $S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}$

Insertion Loss $S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$ $S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$

HIGH-PERFORMANCE EDA

ANSOFT

Insertion Loss & Return Loss



REFLECTION

$$\frac{\text{Reflected}}{\text{Incident}} = \frac{A}{R}$$

Return Loss

TRANSMISSION

$$\frac{\text{Transmitted}}{\text{Incident}} = \frac{B}{R}$$

Insertion Loss

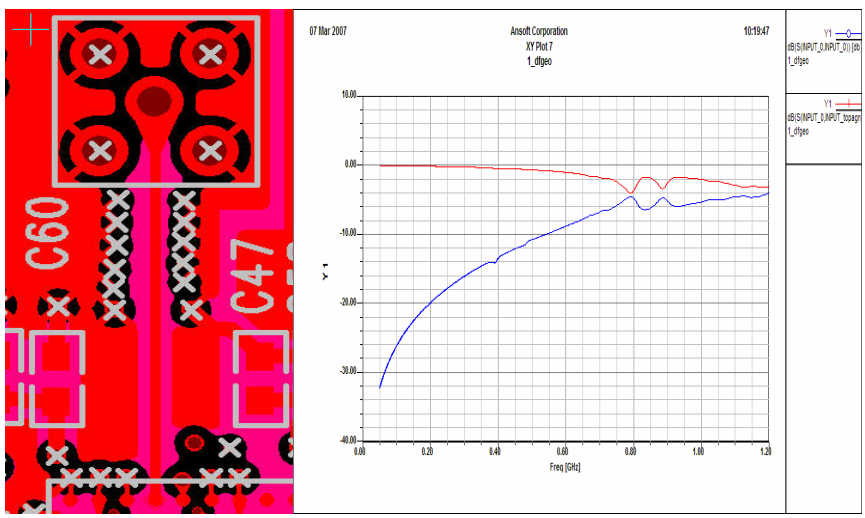
How to get S-Parameter

- Simulation: Full Wave EM Simulation
  - Including complex 3D construction and non-idea return path
- Measurement
  - Vector Network Analyzer
  - Test fixture de-embedding

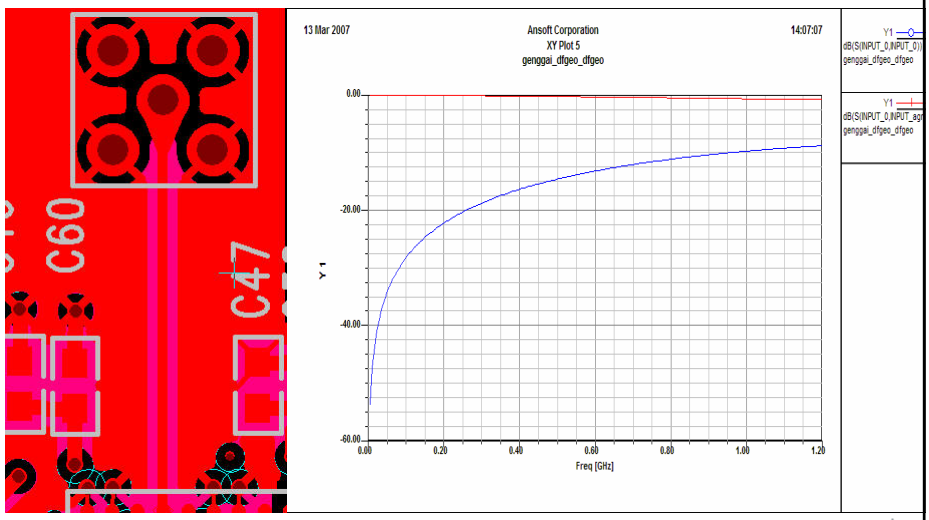
What's S-Parameter tell you

- Accurately describe the electrical characteristics of passive structures over a very wide bandwidth
  - Insertion loss and return loss of non-idea T-Line
  - Isolation of separate plane
  - Multi-coupling of signals and power nets

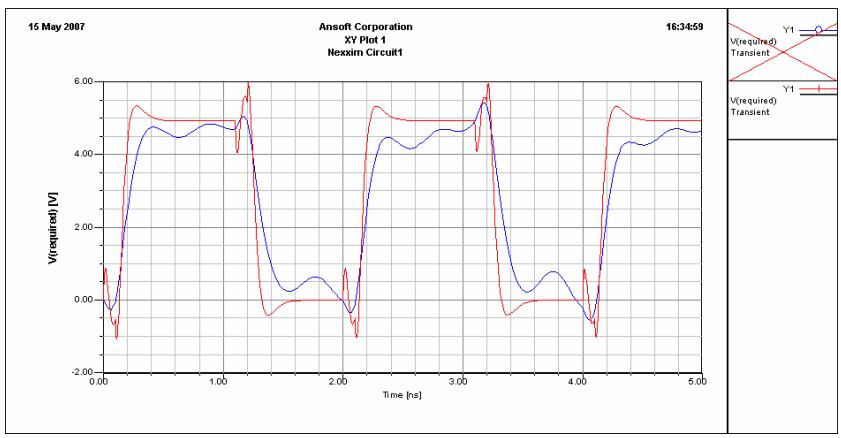
S-Parameter of Non-idea plane



S-Parameter of idea plane



Transient analysis results

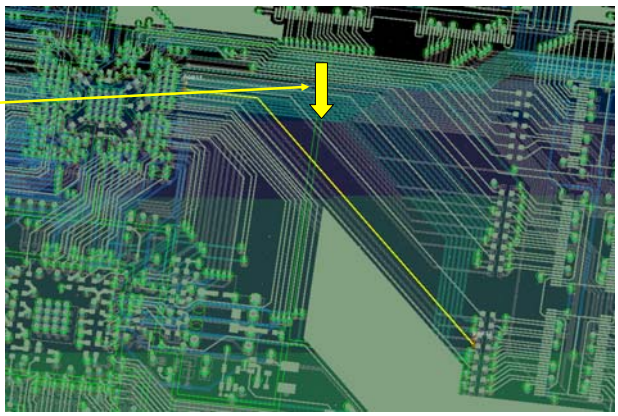


- 100ps Tr/Tf，1GHz pulse

Cross gap analysis

SI Investigation ---Signal Net IOA8 Cross Split Power Plane: Reference Changed

Power Plane Split Here

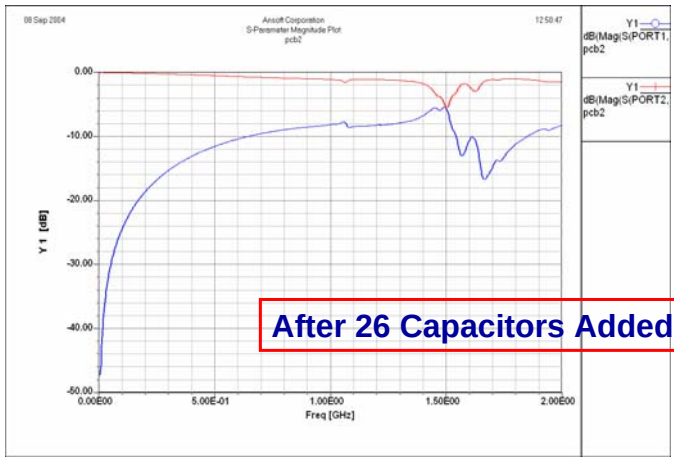


Cross gap analysis

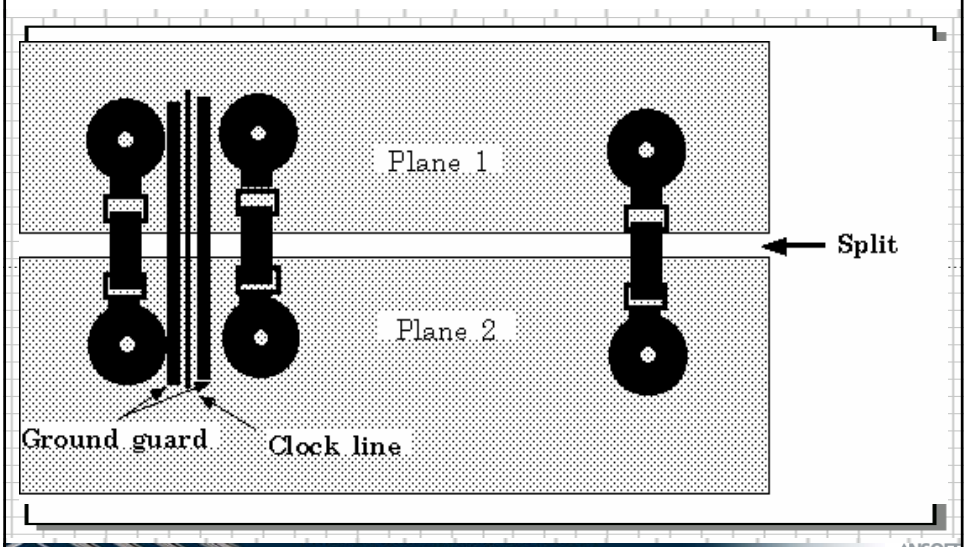
Signal Trace Transmission / Reflection(S21 /S11)

Cross gap analysis

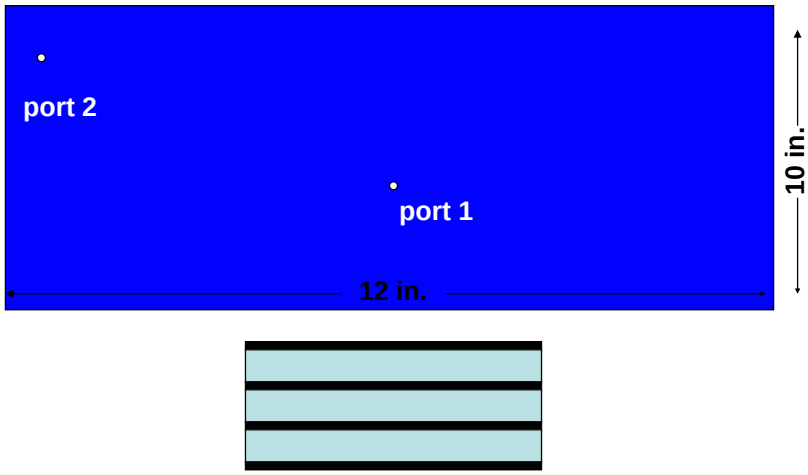
Signal Trace Transmission / Reflection(S21 /S11)



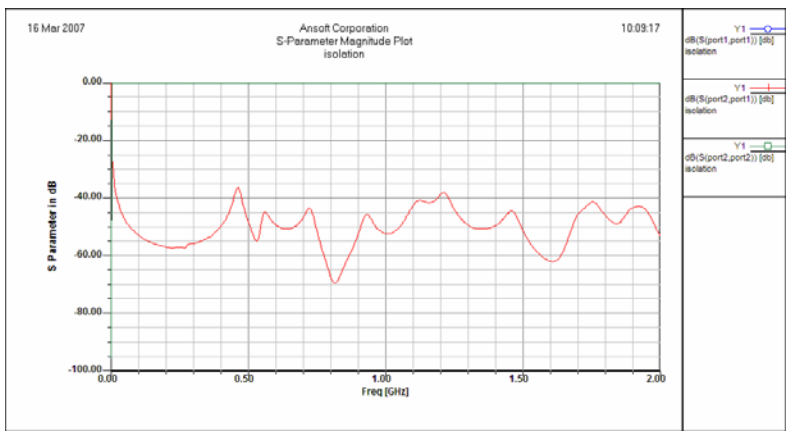
Isolation of split plane



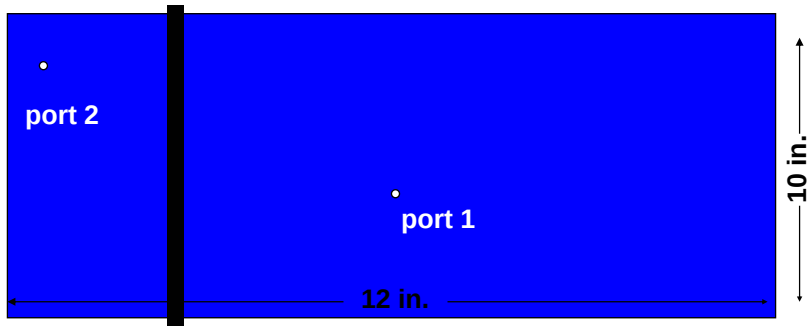
Isolation analysis



Result

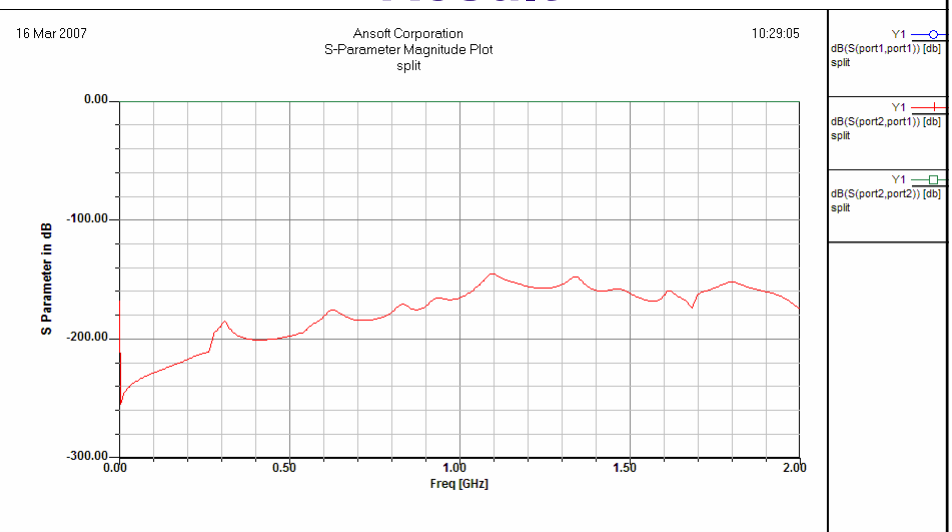


Isolation analysis

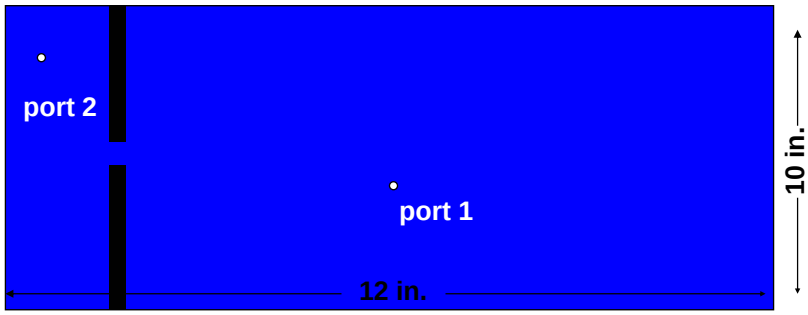


Separate

Result

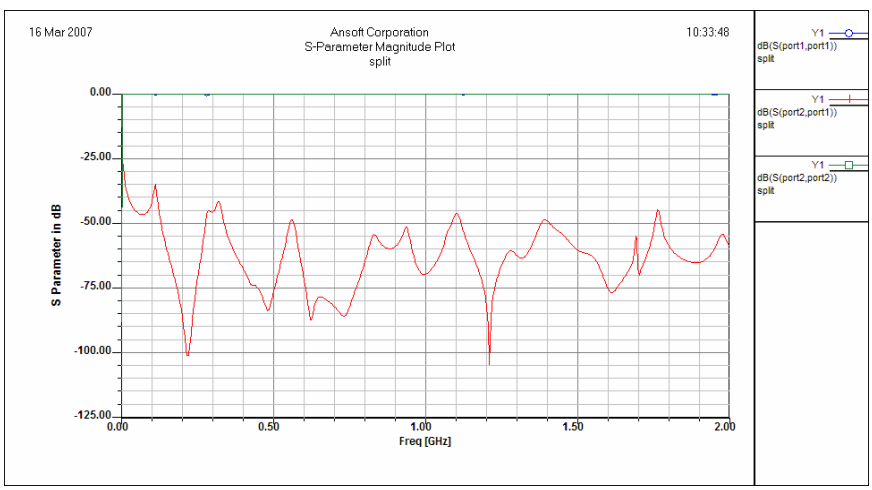


Isolation analysis

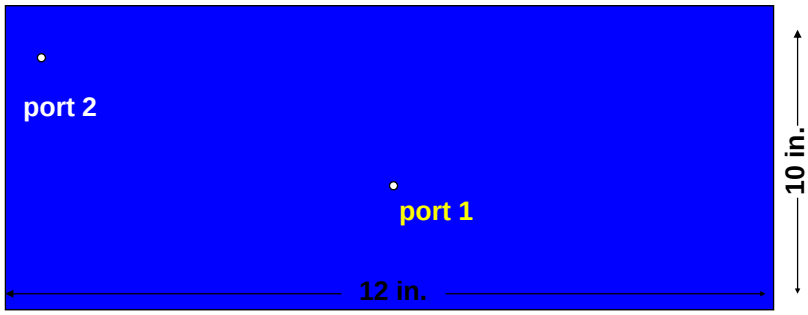


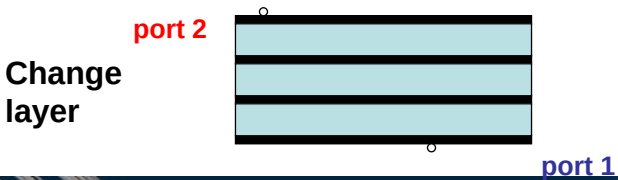
One point connect

Result



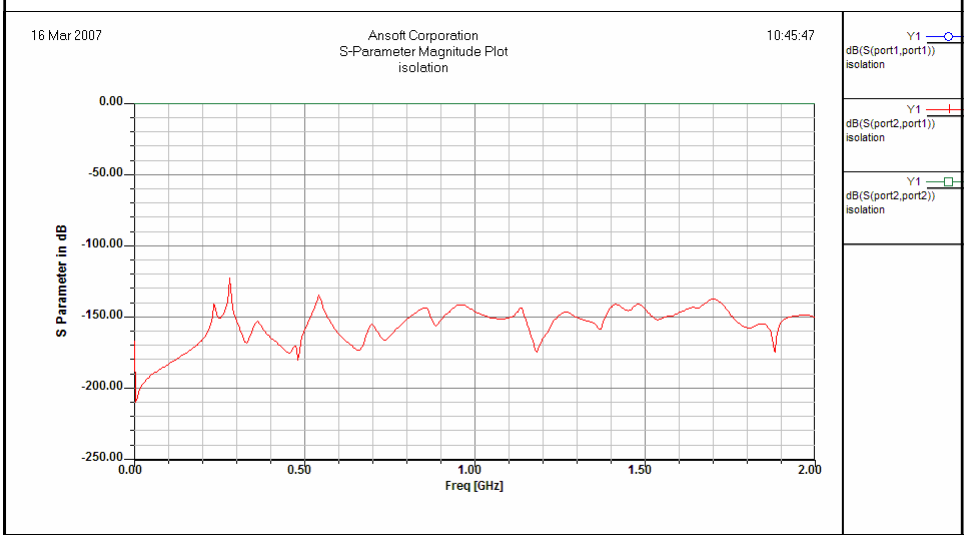
Isolation analysis





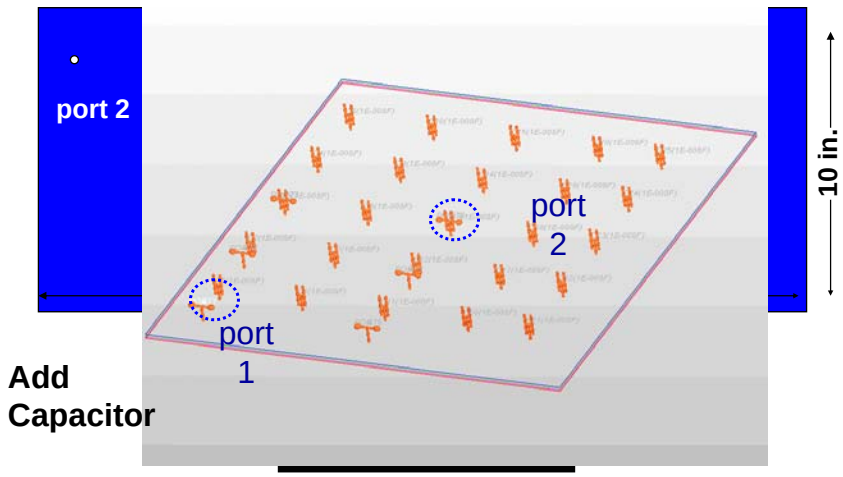
HIGH-PERFORMANCE EDA

Result



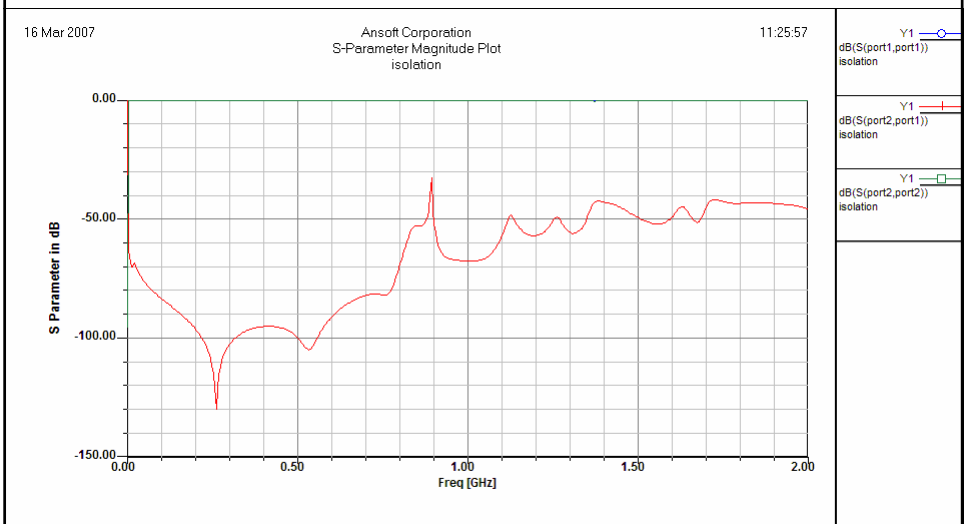
HIGH-PERFORMANCE EDA

Isolation analysis



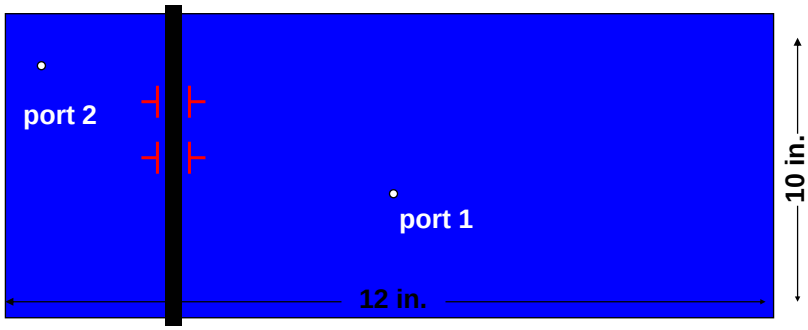
HIGH-PERFORMANCE EDA

Result



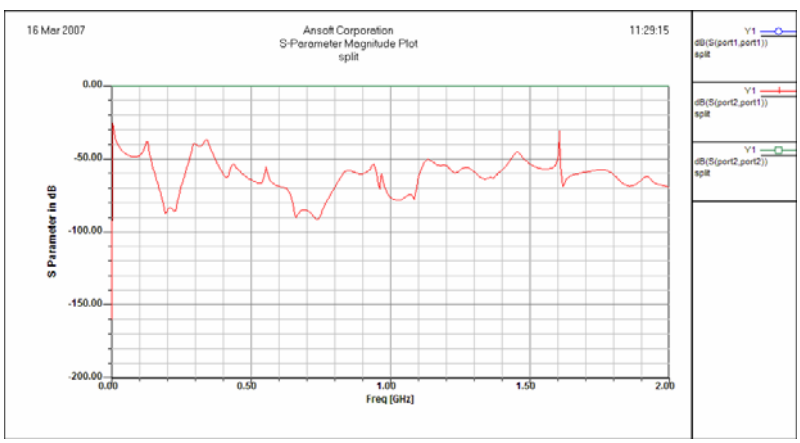
HIGH-PERFORMANCE EDA

Isolation analysis

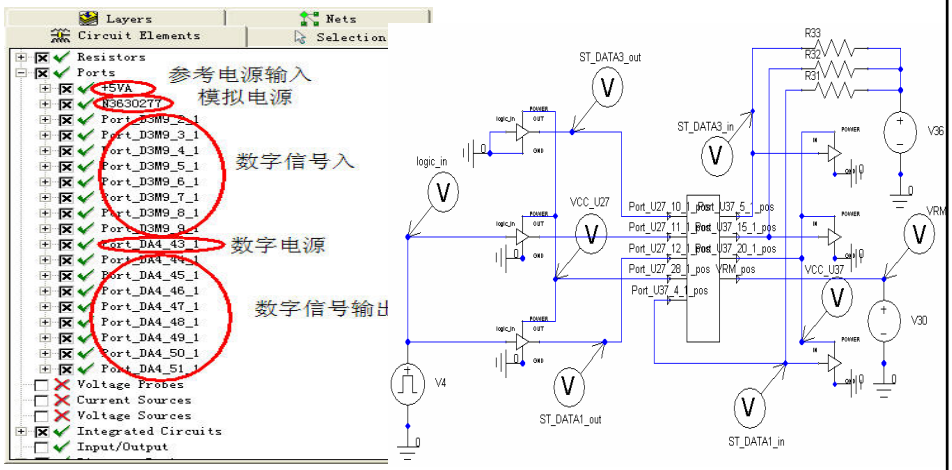


Add Xgap Capacitor

Result



SSO analysis using N-port S-Parameter



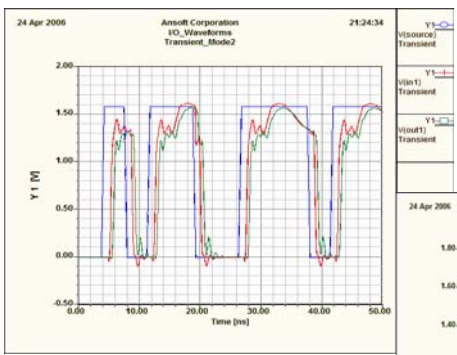
Problem in using S-Parameter for Transient analysis

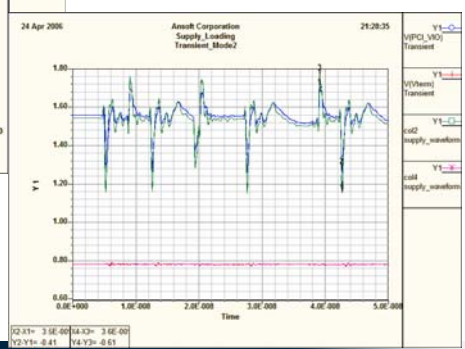
- Non-convergence
  - Most Timing domain simulator using IFFT to solve the S-parameter (because it's Frequency domain)
  - Mostly happen in multi-port S-parameter(>10) or long delay
  - S-parameter Convolution
    - Do not Consider causality/passivity problems
- Non-Causal or Non-Passive
  - State-space with rational functions or Enforce Passivity option

Ensuring accuracy across simulation domains

- State Space
  - Pole-residue fit to frequency-domain data
  - Only stable poles used: causal
  - Very efficient transient simulation
    - Simple first-order differential equation
  - Passivity not guaranteed
    - But can be enforced for moderate-sized problems

Transient analysis results using State Space

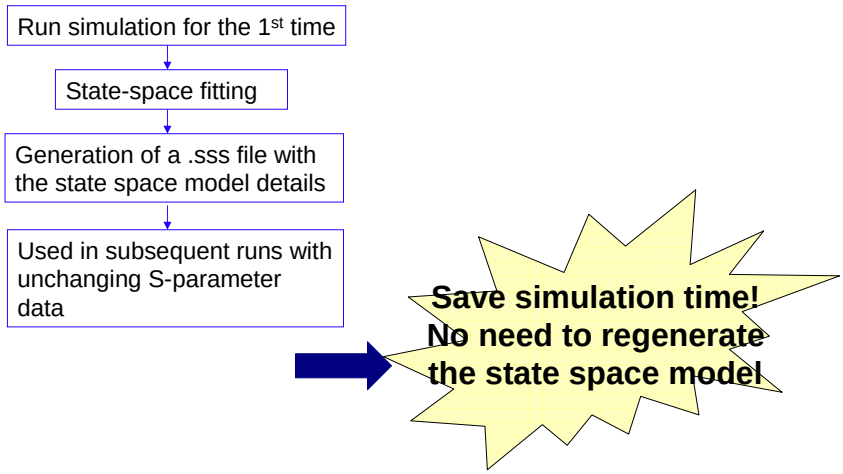




18 IBIS Drivers
57 Port S-parameter model

Transient simulation time: 366s

Reuse of state-space model



Conclusion

- S-Parameter Model for High Speed Interconnection
  - Wideband, Accuracy
  - Full Wave Simulation or Measurement
- Time Domain Simulation for S-Parameter Model
  - Convergence, Causal and Passive
  - State Space and Convolution

Issues Combining Buffer and Interconnect Model Formats

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马梦宽
英特尔公司
IBIS 委员会主席

IBIS Summit
Beijing, China
September 11, 2007

亚洲 IBIS 技术研讨会
中国北京
2007 年 9 月 11 日

1

Legal Disclaimer

An Additional Disclaimer

- The following information is presented as the opinion of one person at Intel. This presentation does not necessarily represent Intel policy, commitments or preferences.
- This is not presented on behalf of the IBIS Open Forum and does not represent the official IBIS Open Forum direction.

Agenda

- The System Viewpoint
- Buffer Model Formats
- Package and Interconnect Model Formats
- Combining Components into a System
  - Summary of Today's Industry Options
- Steps Toward a Unified Solution

The Number of Model Formats is Increasing!

- IC designers can model buffers in many ways
  - Proprietary SPICEs (transistor or behavioral)
  - Traditional IBIS (3.2/4.0): table-based
  - Verilog-A (for analog-only simulation)
  - Verilog-AMS/VHDL-AMS (for mixed-signal)
  - Multi-lingual IBIS 4.1/4.2 (IBIS+*-AMS, IBIS+Verilog-A, IBIS+SPICE)
- There are just as many ways to model packages & interconnects
  - Proprietary SPICEs (lumped-element, RLGC)
  - Traditional IBIS (3.2/4.0) for packages
  - S-parameters (Touchstone*, CITI*)
  - ICM (RLGC or Touchstone*)
- … and many ways to combine these models in a system
  - Both system and IC vendors simulate system designs
  - System sims involve all of the above plus other components

How well do all these options work together?

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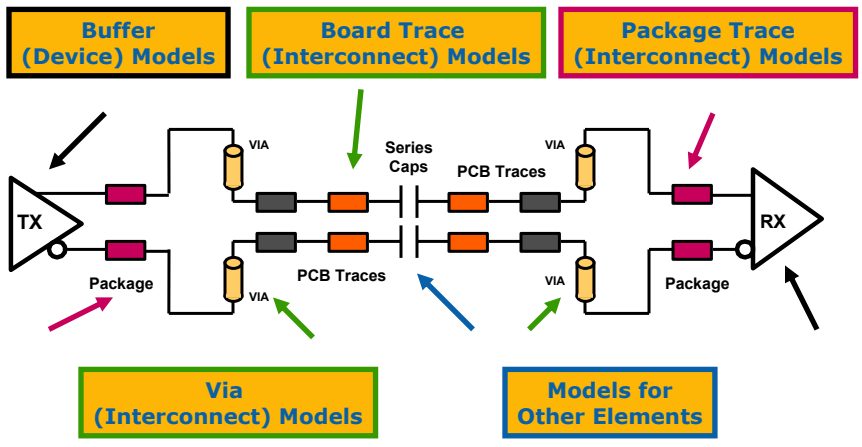
SI Models - The System View

SerDes Example



… plus the language or format that connects them all

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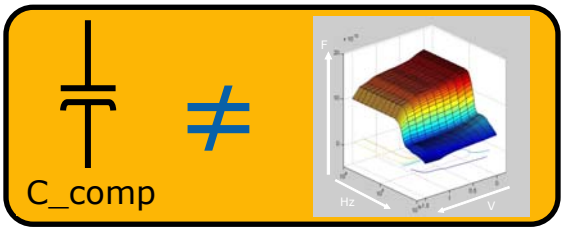
Buffer Models

- "Traditional" table-based IBIS 3.2/4.0 has some advantages
  - Standard and enjoys widespread support
  - Fast (behavioral) and protects IP
  - Supports integration with layout (pin and signal information)
  - Free syntax checking (IBIS Golden Parser)
  - Reasonably simple to learn
- Format has increasing issues



  - Best for single-ended, time-domain design
  - Frequency-domain support is weak (e.g., C_comp as buffer capacitance)
  - Also weak for SerDes: equalization, frequency-dependence, jitter

"SPICE" vs. "AMS" vs. Algorithmic Models

- Several options exist to improve buffer model support

SPICE

- Can be used behaviorally
- Familiar to most engineers
- Versions implemented in most EDA tools
- Not standard
- A format, not a language
- Analog-only
- Not suited to algorithmic modeling
- Still data-driven

"AMS"

- VHDL-AMS, Verilog-AMS
- Mixed-signal (digital + analog)
- Also Verilog-A (analog-only)
- Industry standard
- Languages, not just formats
- More familiar to IC designers than SI/system designers
- Expensive to implement for lower-cost EDA tools
- Languages are not easily cross-ported
- HDLs, not general purpose mathematical languages

IBIS 4.2 supports Verilog-AMS, VHDL-AMS, Verilog-A and (Berkeley) SPICE;
IBIS-ATM working on SerDes algorithmic models

Package modeling through IBIS 4.2

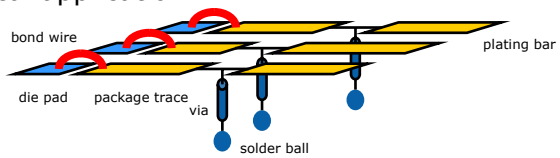
- [Package] keyword
  - Required for each component
  - Contains corner values for R_pkg, L_pkg and C_pkg
- [Pin] keyword
  - Each pin can have a distinct R_pin, L_pin or C_pin value
  - Only a single value can be used (no corners)
- [Package Model] keyword (also Electrical Board Description)
  - Can reference an external file or data within the same .IBS file
  - Two methods available currently in IBIS
    - *Coupled, single-matrix RLC description (full, banded, and sparse matrix formats available)*
    - *Uncoupled multi-section description using RLC, length*

No coupling for multi-section packages, no AC loss
Not suitable for today's fastest designs!

BGA Package Structure

Drawing courtesy A. Muranyi

- A typical application

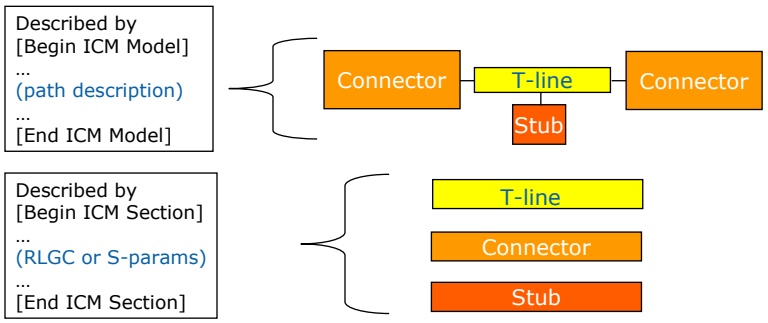


- BGA (Ball Grid Array) Package structure
  - **Bond wire (usually gold): connects die pad to traces**
  - **Package trace: lossy routing path in package FR4**
  - **Via: connects trace to solder ball**
  - **Solder ball: attach point for device to PCB**
  - **Plating par: lossy stub left from separation of packages**

Can we describe this today using EBD, IBIS or PKG?
Not with adequate loss and coupling.

SPICE and ICM

- Many vendors use SPICE to address IBIS package shortcomings
  - Most SPICEs support lumped or distributed RLGC
  - Proprietary! One model set may not work across multiple tools
- ICM (IBIS Interconnect Modeling specification) available but new
  - Standard, with industry support picking up
  - A separate specification – no direct connection to IBIS yet
  - Not intended to support series components (e.g., series capacitance)



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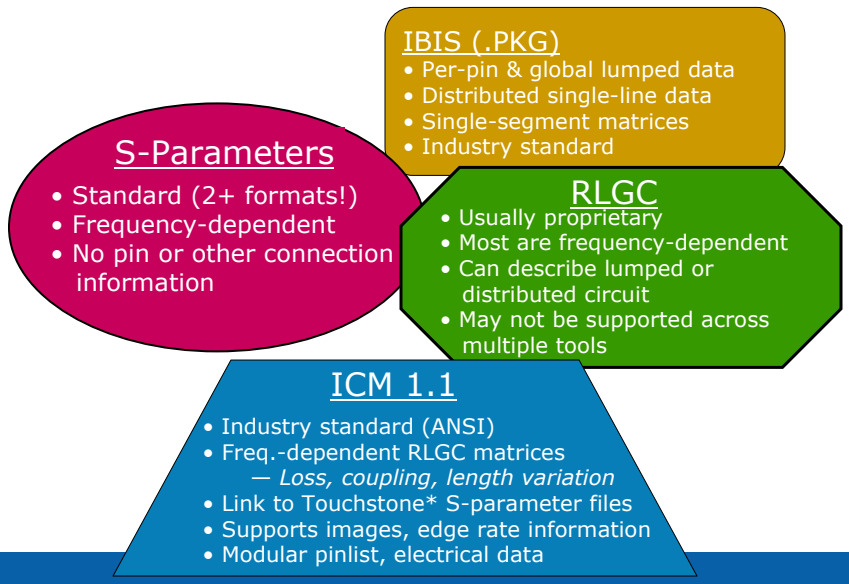
Package & Interconnect Formats



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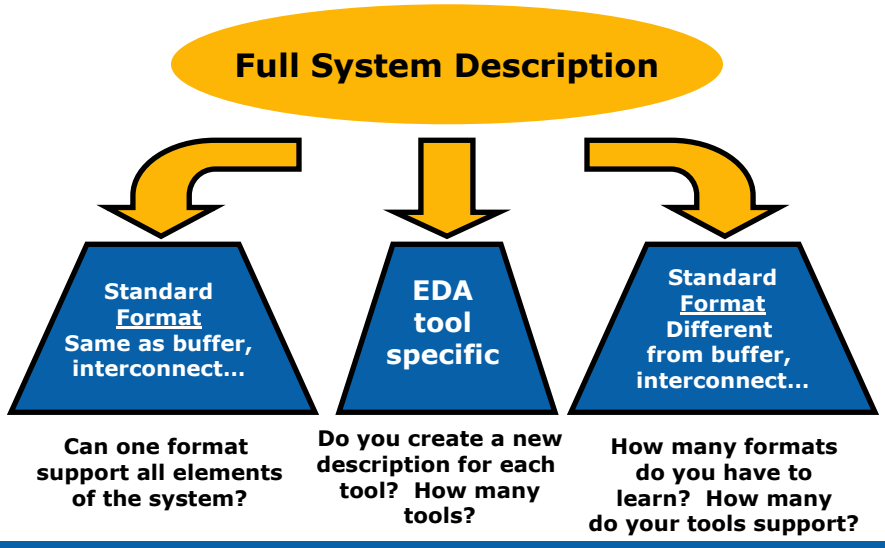
Combining Models – A Dilemma



SPICE as a Topology Format

- Some IC vendors want to provide complete system "decks"
- Using proprietary SPICEs is popular, but faces several issues
  - Inconsistency in format
    - *SPICE is not standard! Elements and features vary across SPICEs*
    - *Some analysis functions are proprietary (e.g., S-parameters)*
  - Lack of expandability
    - *Users cannot define new elements or analyses, only new subcircuits*
  - Inconsistency in results
    - *With different engines, the same model can give different results*
  - Integration with layout is not automatic

All are barriers to using SPICE to represent systems across tools

Models in Combination

Model Type	Buffer	Interconnect (Board, Package, etc.)	"System Assembly"
Behavioral SPICE	Which SPICE? Frequency-dependent interconnect? Features compatible across several tools?		
Traditional IBIS	Weak C_comp, no core-side information…	No distributed, frequency-dependent interconnect	not intended
IBIS 4.2 + Berkeley SPICE	➡	No distributed, frequency-dependent interconnect	not intended
IBIS 4.2 + *-AMS	➡	Need custom transmission line libraries	not intended
ICM 1.1	not intended	➡	No active models, limited series components
Verilog-A	➡	Need custom transmission line libraries	➡

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Steps Toward a Unified Solution

- Options exist for a unified buffer+interconnect+system format
  - e.g., Verilog-A can be treated as a SPICE-like standard analog language
  - Standard transmission line libraries would be required to support interconnects under Verilog-A
- The IBIS Open Forum is addressing several of these issues
  - IBIS-ATM is adding algorithmic model support for SerDes
  - IBIS-ICM links are being developed for a future version of IBIS
  - A standard SPICE superset syntax has been proposed
    - *"The 3S Proposal" – http://www.eda.org/ibis/summits/feb07/mirmak.pdf*
- Market forces will determine the most popular combination
  - e.g., IBIS 4.2 + ICM 1.1 + Verilog-A might be possible, but it might not be least expensive or easiest to learn

Make your preferences known!

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SerDes Modeling:
IBIS-AMI Evaluation Toolkit

Presented by: Todd Westerhoff, SiSoft
twesterh@sisoft.com

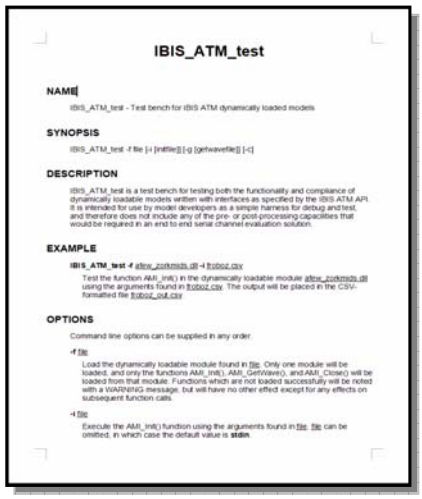
IBIS Summit
Beijing, China
September 11, 2007

Signal Integrity Software, Inc.

Challenges

- IBISCHK cannot check compiled models
  - Similar problem to AMS model calls
- Several possible sources of platform/model incompatibility
  - Incorrect EDA tool implementation
  - Incorrect model implementation
  - Incompatible run-time libraries
- A “reference standard” for IBIS-AMI is needed
  - Reference platform implementation
  - Reference model implementation

IBIS_AMI_Test



IBIS_ATM_test

NAME

IBIS_ATM_test - Test bench for IBIS ATM dynamically loaded models

SYNOPSIS

IBIS_ATM_test -f file [-i [initfile]] [-g [getwavefile]] [-c]

DESCRIPTION

IBIS_ATM_test is a test bench for testing both the functionality and compliance of dynamically loadable models written with interfaces as specified by the IBIS ATM API. It is intended for use by model developers as a simple harness for debug and test, and therefore does not include any of the pre- or post-processing capabilities that would be required in an end to end serial channel evaluation solution.

EXAMPLE

IBIS_ATM_test -f afrev_zorkmids.dll -i frobozz.csv

Test the function AMI_Init() in the dynamically loadable module afrev_zorkmids.dll using the arguments found in frobozz.csv. The output will be placed in the CSV-formatted file frobozz_out.csv

OPTIONS

Command line options can be supplied in any order.

-f file

Load the dynamically loadable module found in file. Only one module will be loaded, and only the functions AMI_Init(), AMI_GetWave(), and AMI_Close() will be loaded from that module. Functions which are not loaded successfully will be noted with a WARNING message, but will have no other effect except for any effects on subsequent function calls.

-i file

Execute the AMI_Init() function using the arguments found in file. file can be omitted, in which case the default value is stdin.

- Allows IBIS-AMI .dll models to be run as standalone “executables”
  - Facilitates model debug
  - Provides standard environment for testing model compliance
- Authored by SiSoft, source code to be turned over to IBIS Open Forum
  - Executable will be publicly available

IBIS_AMI_Tx Model

AMI File

```
(IBIS_AMI_Tx
 (Dll
  (linux ibis_ami_tx_lnx.so)
  (solaris ibis_ami_tx_sun4.so)
  (windows ibis_ami_tx.dll)
 )
 (Reserved_Parameters
  (Ignore_Bits (Type Integer) (Default 21))
  (Max_Init_Aggressors (Type Integer)(Default 25))
  (Init_Returns_Impulse (Type Bool)(Default True))
  (GetWave_Exists (Type Bool) (Default True))
 ) | End Reserved
 (Model_specific
  (txtaps
    (tapid (Range -1 3) (type int) )
    (txtapcoeff
        (-1 (Range -0.1 0.1 0.1) (Type float) (Default 0))
        (0 (Range 1 1 0) (Type float) (Default 1))
        (1 (Lis
        (2 (Ran
        (Defaul
        (3 (Ran
        (Defaul
    )  | tapcoe
    )  | txtaps
  (tx_freq_offs
 ) | End User_D
)  | End IBIS_A
```

```
tmp_dbl = (double*)malloc( row_size*(aggressors+1)*sizeof( double ) );
for( ondx = 0; ondx < aggressors+1; ondx++ ) {
    for( indx = 0; indx < row_size; indx++ ) {
        tmp_dbl[ indx+row_size*ondx ] =
                                self->taps[0]*impulse_matrix[ indx+row_size*ondx ];
        if( indx >= self->samples ) {
            tmp_dbl[ indx+row_size*ondx ] +=
                self->taps[1]*impulse_matrix[ indx+row_size*ondx-self->samples ];
        }
        if( indx >= 2*self->samples ) {
            tmp_dbl[ indx+row_size*ondx ] +=
              self->taps[2]*impulse_matrix[ indx+row_size*ondx-2*self->samples ];
        }
        if( indx >= 3*self->samples ) {
            tmp_dbl[ indx+row_size*ondx ] +=
              self->taps[3]*impulse_matrix[ indx+row_size*ondx-3*self->samples ];
        }
        tmp_dbl[ indx+row_size*ondx ] *= self->swing;
    }
}
memcpy( impulse_matrix, tmp_dbl, row_size*(aggressors+1)*sizeof( double ) );
free( tmp_dbl );

//Calculate the step response
self->step_response = (double*)malloc( row_size*sizeof( double ) );
self->step_response[0] = sample_interval * impulse_matrix[0];
for( indx = 1; indx < row_size; indx++ ) {
    self->step_response[indx] = self->step_response[indx-1] +
                                sample_interval * impulse_matrix[indx];
}
```

Algorithmic Model Code

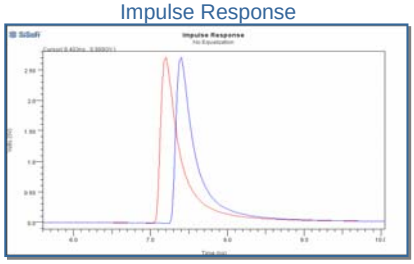
- Reference IBIS & AMI files
- Reference Algorithmic model
  - Impulse response and waveform processing
  - 4 tap equalizer
    - Pre-cursor tap
    - Cursor tap
    - 2 post-cursor taps
    - Model normalizes tap sum
  - Scalable transmit swing
  - Executable and source code publicly available

IBIS-AMI Evaluation Toolkit

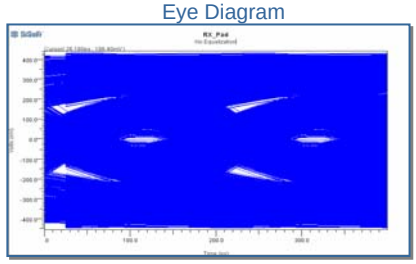
- Goal: allow interested parties to evaluate & develop IBIS-AMI models
- Available on-line from IBIS-ATM task group website and from www.sisoft.com
- Contents
  - IBIS_AMI_Test utility
  - Sample TX model and source code
  - Sample input data, scripts, documentation
- Email discussion group established: ibis-ami-toolkit@freelists.org

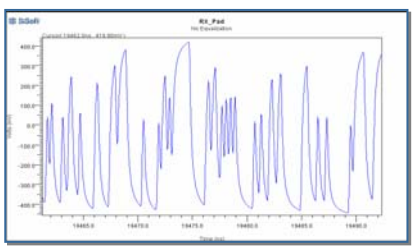
Sample Results: No TX EQ

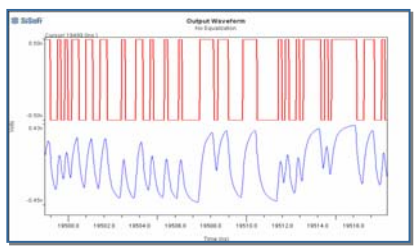
Impulse Response



Eye Diagram





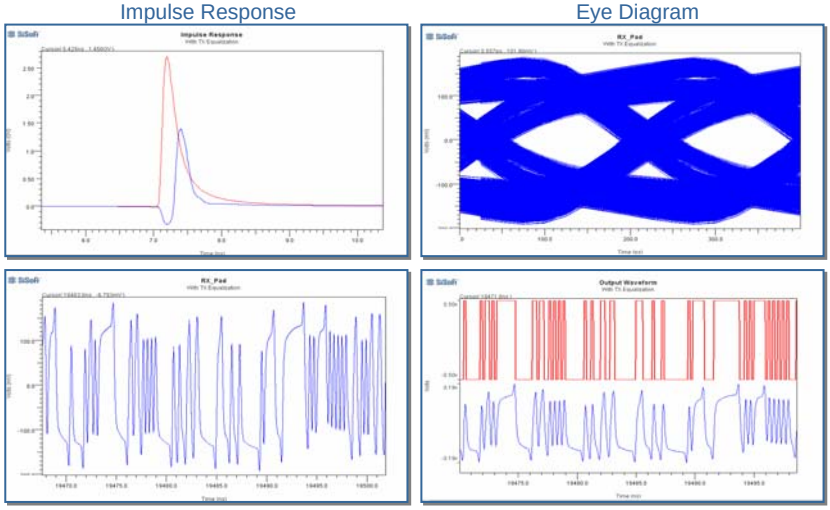


Signal @ Rx pad, Stimulus

Sample Results:
TX EQ: (-.15, .7,-.125,-.025)*0.8

Impulse Response

Eye Diagram



Signal @ Rx pad, Stimulus

IBIS-AMI Toolkit

- Provides a “reference implementation” for testing EDA platforms and IBIS-AMI models
- Allows users to assess IBIS-AMI model functionality and performance
- Users can run analyses based on their own designs and channel impulse responses

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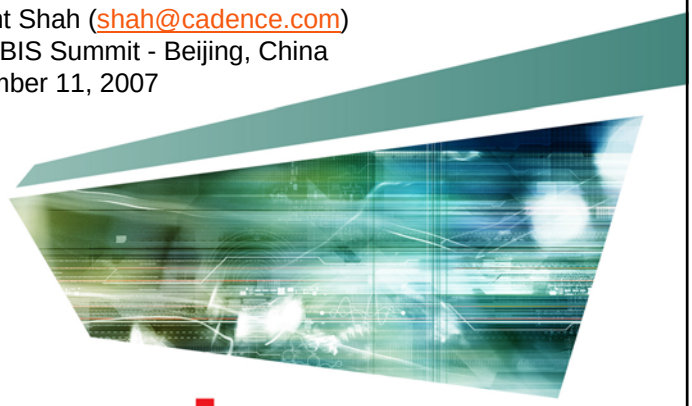
INVENTIVE

IBIS AMI Model Developers Toolbox

Hemant Shah (shah@cadence.com)
Asian IBIS Summit - Beijing, China
September 11, 2007



What's in it

- Sample Model Rx
  - Source code
  - Executable on Linux
  - Model params file
- Tester Program
  - Executable on Linux
  - Tester config file
- Starter model templates
- Documentation

- Use sample model and tester program to understand the details of the IBIS AMI API
- Create your own algorithmic models using starter model templates
- Use the tester program to test the model

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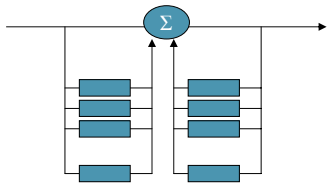
Sample Rx Model

- Continuous Time Filter (CTF) RX model
  - Combination of feed forward and feed backward filter
  - Modifies the waveform given a set of coefficients
  - Tested for 6.25Gbps data rate
  - User configurable forward and backward taps



- Parameters needed by the model
  - Number of forward taps, Number of backward taps, Coefficients
  - Can be provided in a file
- To Compile:
  a) gcc -c ibis_ctf_rx.c
  b) gcc -shared -o ibis_ctf_rx.dll ibis_ctf_rx.o

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CDNS AMI Tester Program

- Inputs
  - Bit Stream: “(0111100001111)”
    - Alternatively, users can specify the number of bits and let tester generate random bits
  - Data Rate
  - Impulse Response
  - DLL to interface to
  - Model specific parameters

- Outputs
  - Wave_out: *voltage-time pairs in txt file* wave form data modified by the Model
  - Wave_in: *voltage-time pairs in txt file* Represents waveform passed to the model
  - ImpulseResponse: IR data if it is modified by the model (init)

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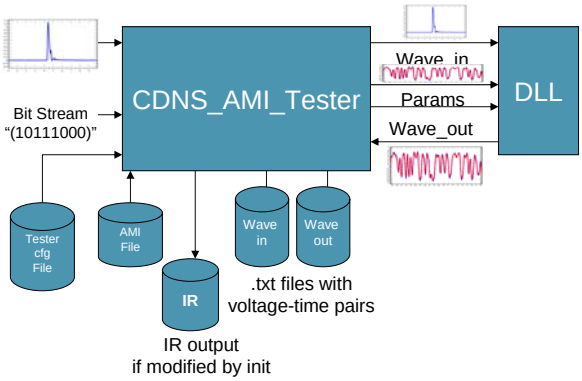
CDNS AMI Tester Program

- Usage:
  CDNS_TESTER [-h] ctf_rx_model



AMI File contains:
- Measurement Delay
  - Ignore data for spec delay
- Model specific parameters

Tester config file contains
- Information generally set by end users through the EDA platform
  - Data Rate
  - Number of bits
  - Input file names
  - Output files names

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How to get the kit

- Cadence AMI Developers toolbox will be available through IBIS web site soon
- In the mean time, you can send request for the toolbox to: shah@cadence.com

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Resources

- Many presentations on Algorithmic Modeling starting from June 2006 can be found at:
  http://www.vhdl.org/pub/ibis/macromodel_wip/archive-date.html
- Updates on the AMI work can also be found in ATM subcommittee updates provided at DAC 2007 and DesignCon 2007 IBIS Summits
  - Presentations can be accessed from this page:
    http://www.vhdl.org/pub/ibis/summits/
- To reach the IBIS-ATM group on this topic, you can send email to: ibis-ami-toolkit@freelists.org

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