

ASIAN IBIS SUMMIT (CHINA)

亚洲 IBIS 技术研讨会 (中国)

September 11, 2007
Park Plaza Hotel
Beijing, CHINA

2007 年 09 月 11 日
北京丽亭华苑酒店
中国 北京

EIA IBIS OPEN FORUM <http://www.eigroup.org/ibis/>



cādence™

Mentor
Graphics®

SYNOPSYS®



SiSoft®



Agilent Technologies

ZTE中兴

ASIAN IBIS SUMMIT (CHINA)

亚洲 IBIS 技术研讨会 (中国)

- 8:15 Refreshments & Sign In
- 9:00 Official Opening and Welcome
- Xiang Zhong JIANG (Huawei Technologies, People's Republic of China)
- Michael MIRMAK (Chair., EIA IBIS Open Forum, Intel Corporation, USA)
- 9:30 Wang Algebra and Interconnects
Bob ROSS (Teraspeed Consulting Group, USA)
- 9:50 IBIS-ATM Update: SerDes Modeling in IBIS
Todd WESTERHOFF (Signal Integrity Software (SiSoft), USA)
- 10:15 BREAK
- 10:30 Serial Link Analysis and PLL Model
Chun Xing HUANG (Huawei Technologies, China)
- 11:00 A Review of Existing Multi-Gbps Serial Channel Analysis
Methods and the Evolution of the Proposed ATM Algorithmic Modeling Standard
Ian DODD*, Richard WARD** and Sanjeev GUPTA*
(*Agilent Technologies, USA and **Texas Instruments, USA)

- 11:30 An Overview of High-Speed Serial Bus Validation Techniques
Arpad MURANYI and Vladimir DMITRIEV-ZDOROV
(Mentor Graphics Corporation, USA)
- 12:00 LUNCH - Hosted by Our Sponsors
- 13:30 Modeling and Simulation for Multi-Gigabit Interconnect System
Shun Lin ZHU, Wei Dong HU, and Song Rui CHEN
(ZTE Corporation, People's Republic of China)
- 14:00 Power Deliver System Design Automation
Tao XU (Sigrity, People's Republic of China)
- 14:30 IBIS 4.2/AMS for DDR2 Timing Analysis
Tao GUAN (Huawei Technologies, People's Republic of China)
- 15:00 Validation for IBIS Models
Lance WANG*, Xin Jun ZHANG**, and Benny YAN**
(IO Methodology, *USA, **People's Republic of China)
- 15:25 IBIS Algorithm Including Reactive Loads
Xue Feng CHEN (Synopsys, People's Republic of China)

- 15:40 BREAK (Refreshments)
- 15:55 Understanding and Using ICM Models
Yu Bao MENG (Cadence Design Systems, People's Republic of China)
- 16:25 Using S-Parameters for High Performance Simulation
Bao Long LI (Ansoft, People's Republic of China)
- 16:55 Issues Combining Buffer and Interconnect Models
Michael MIRMAK (Intel Corporation, USA)
- 17:15 SerDes Modeling: IBIS-AMI Evaluation Toolkit
Todd WESTERHOFF (Signal Integrity Software (SiSoft), USA)
- 17:20 IBIS AMI Model Developers' Toolbox
Hemant SHAH (Cadence Design Systems, USA)
- 17:25 Concluding Items
- 17:30 END OF IBIS SUMMIT MEETING