Extracting On-Die Terminators

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Process Motivation

- Issues with "Clip and Extend" recommendations
- "Black box" rules from experiences since 1992 (Zeelan with Quad format)
  - Decompose model consistent with the internal architecture
    - Example: Output and clamps isolated by curvature changes (Nasef, October 1999 IBIS Summit)
  - Extrapolate for continuous slope
    - Outputs above and on-die extractions here
    - Known SPICE MOSFET level slope discontinuity issues
- Extrapolation recommended in IBIS Cookbook

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Creating Clamp Tables

- Goal: Mimic physical device 3-terminal simulation
  - [Gnd Clamp Ref] Vg, [Power Clamp Ref] Vp anchors
    - ESD or substrate "diodes"
    - On-Die Terminator (ODT) "resistance" structure
  - Best currents thru Vp and Vg for rail analysis
  - I/O node correct with Vg and Vp changes
- Default algorithm covers most practical cases
  - Based on deviation from Thevenin resistor ODT
  - "pullup" and "pulldown" ODTs are subsets
  - $\boxed{\textbf{DEC: Deviate Extrapolate Calculate}}$

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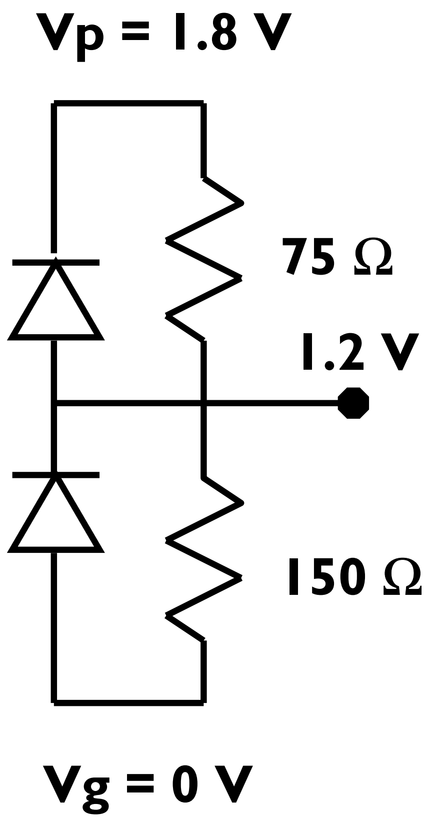
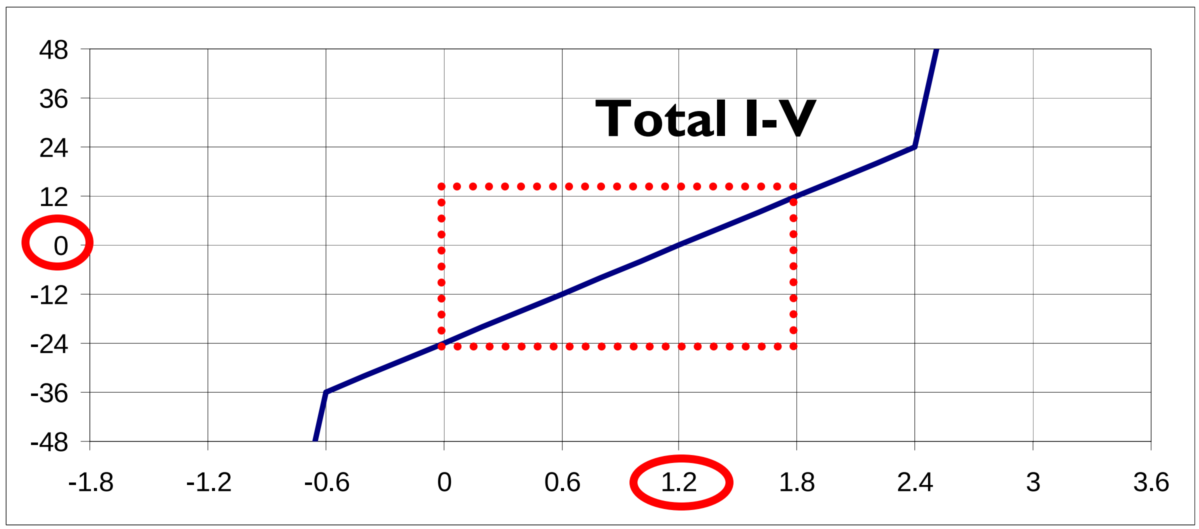
Example: 50 Ω, 1.2 V ODT





50 Ω Total I-V curve with 0.6 V "stick" diodes anchored to each rail

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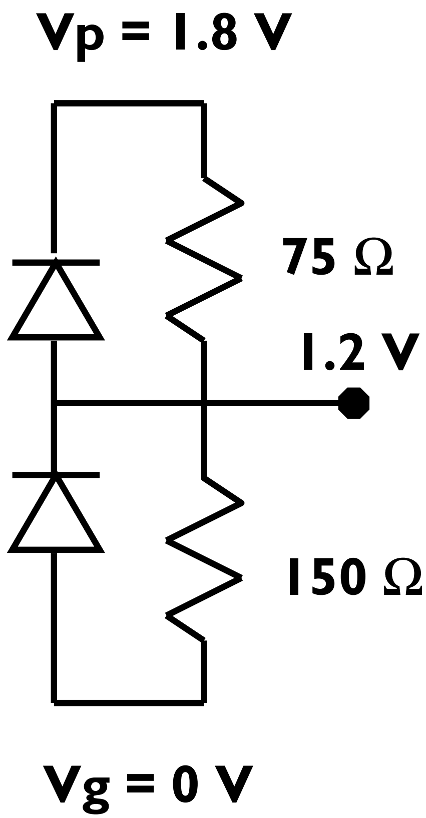
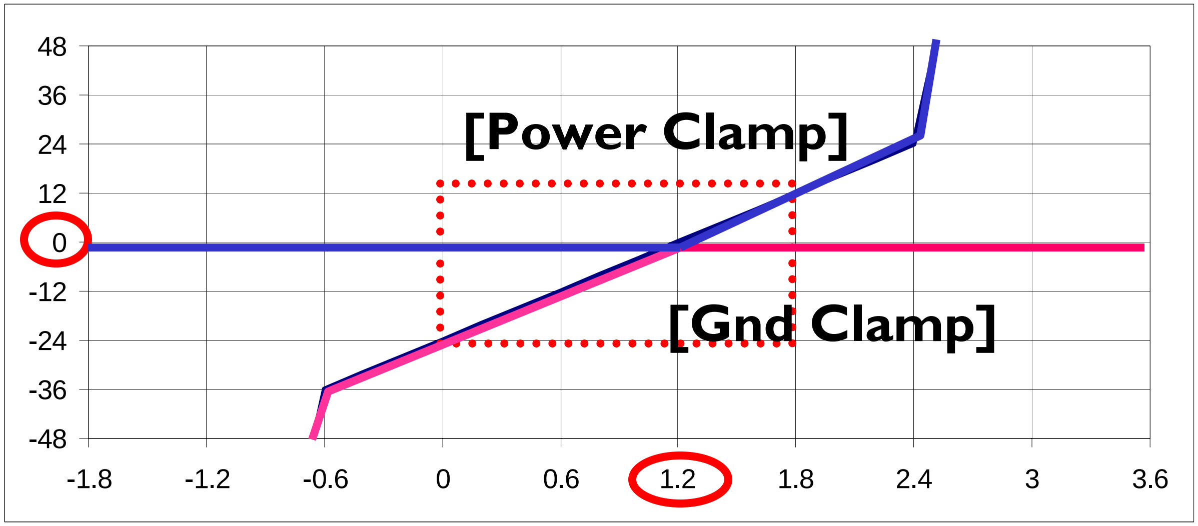
Clip and Extend





50 Ω Total I-V curve with 0.6 V "stick" diodes anchored to each rail

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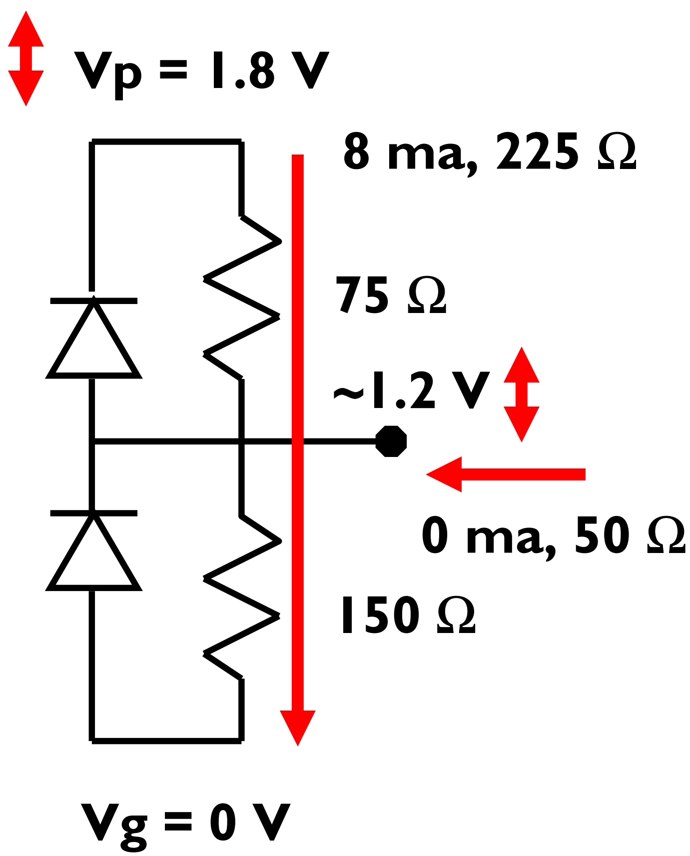
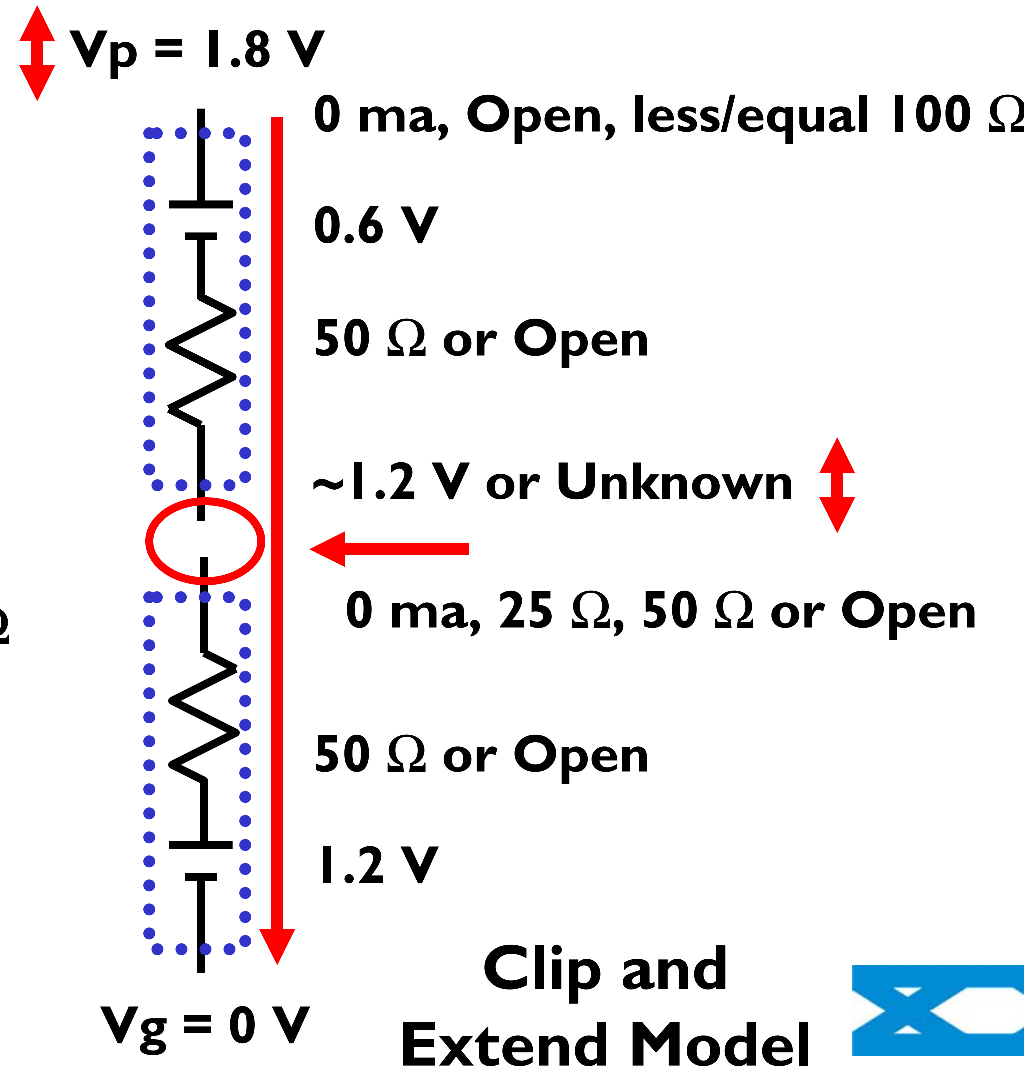
I(V) Blocks and Simulations



Resistor Network



Clip and Extend Model

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Problems with Clip and Extend

- Wrong circuit impacting IBIS 3.2 and beyond
  - DC currents different (with, without I/O node circuit)
  - AC Thevenin impedances different and open
  - Higher frequency effects from non-linear elements
  - Driver at I/O node sees different impedance
- Tool dependencies including
  - Slope discontinuities issues
  - Open 0 ma discontinuities with potential simulation ambiguities and failures (Errors)
  - Unpredictable performance even with validation
- Avoid "Clip and Extend", use DEC
- Be wary of any truncation recommendation

DEC (from Resistors) Algorithm

- Draw box bounded by (Vg, Ig) and (Vp, Ip) and draw the zero current axis
- Draw the three lower-left to upper right diagonals, where the upper region is for the [Gnd Clamp], and the lower region is for the [Power Clamp]
- ***Deviate***: Proportionally allocate "Total I-V" delta deviation to [Gnd Clamp] and [Power Clamp] diagonals
- ***Extrapolate*** [Gnd Clamp] data ABOVE Vp
- ***Extrapolate*** [Power Clamp] data BELOW Vg
- ***Calculate*** [Gnd Clamp] data BELOW Vg (Total - PC)
- ***Calculate*** [Power Clamp] data ABOVE Vp (Total - GC)
- (Backup slides for some computational details)

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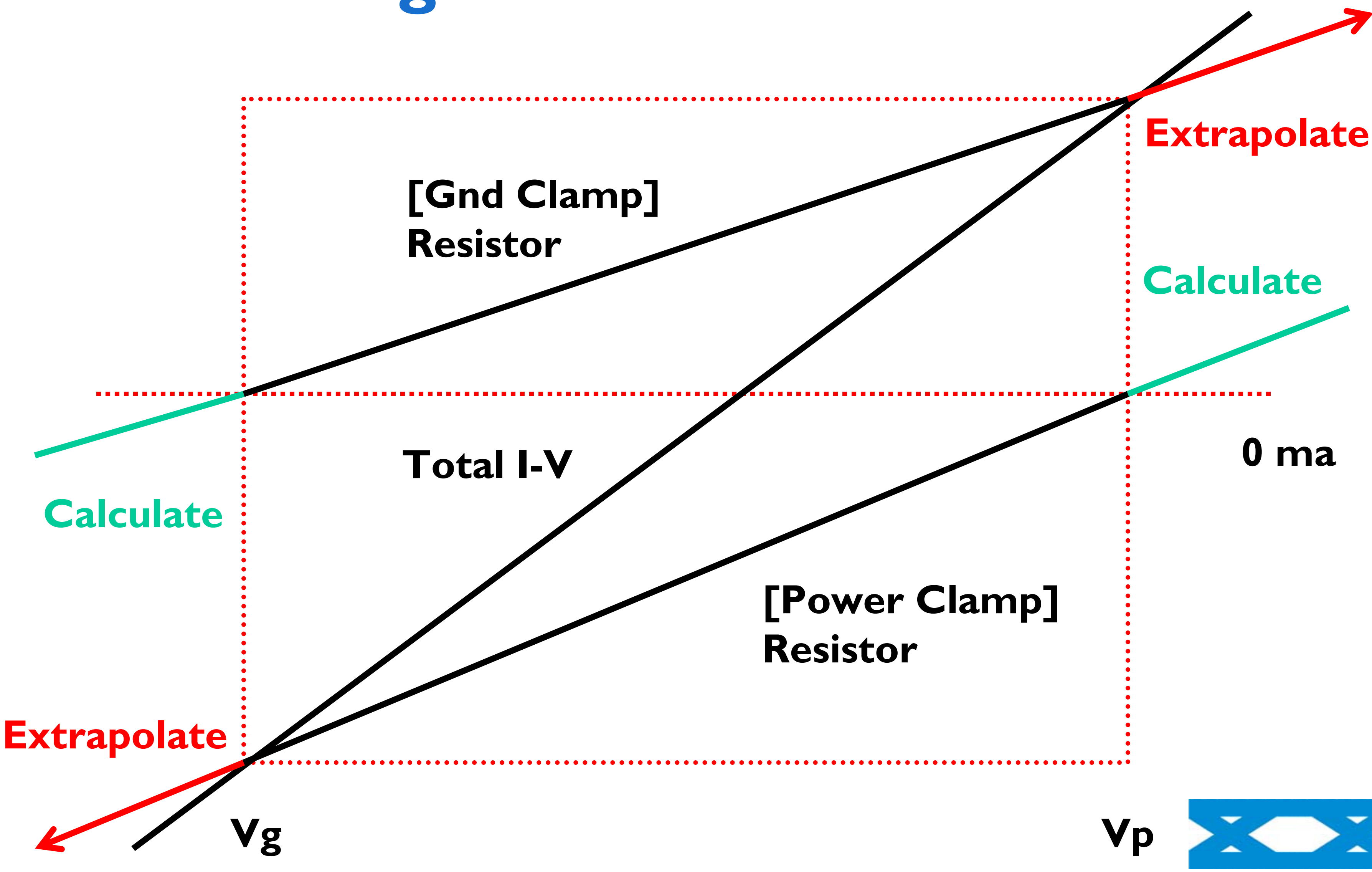
Diagonals and Resistors



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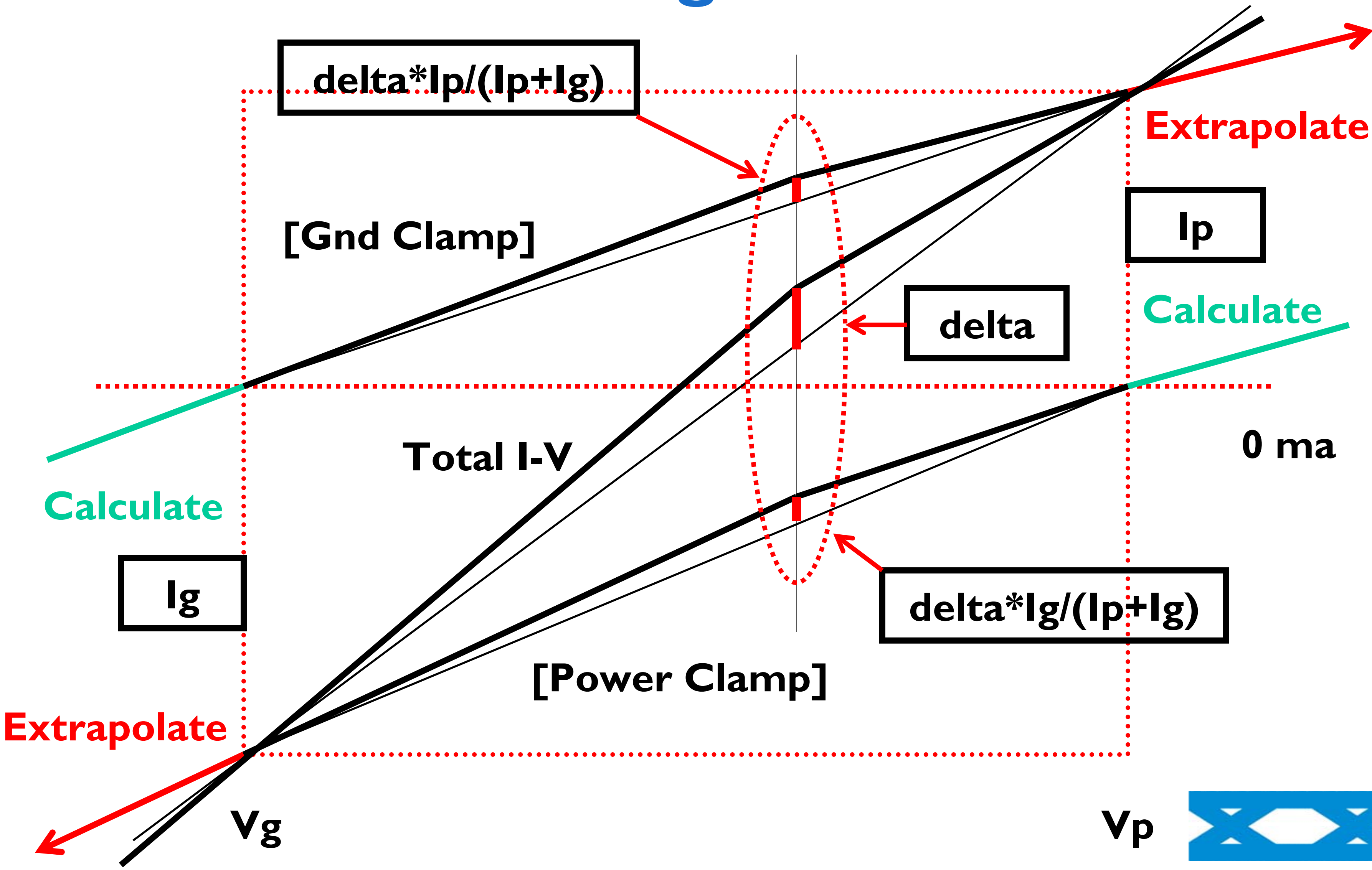
DEC Algorithm



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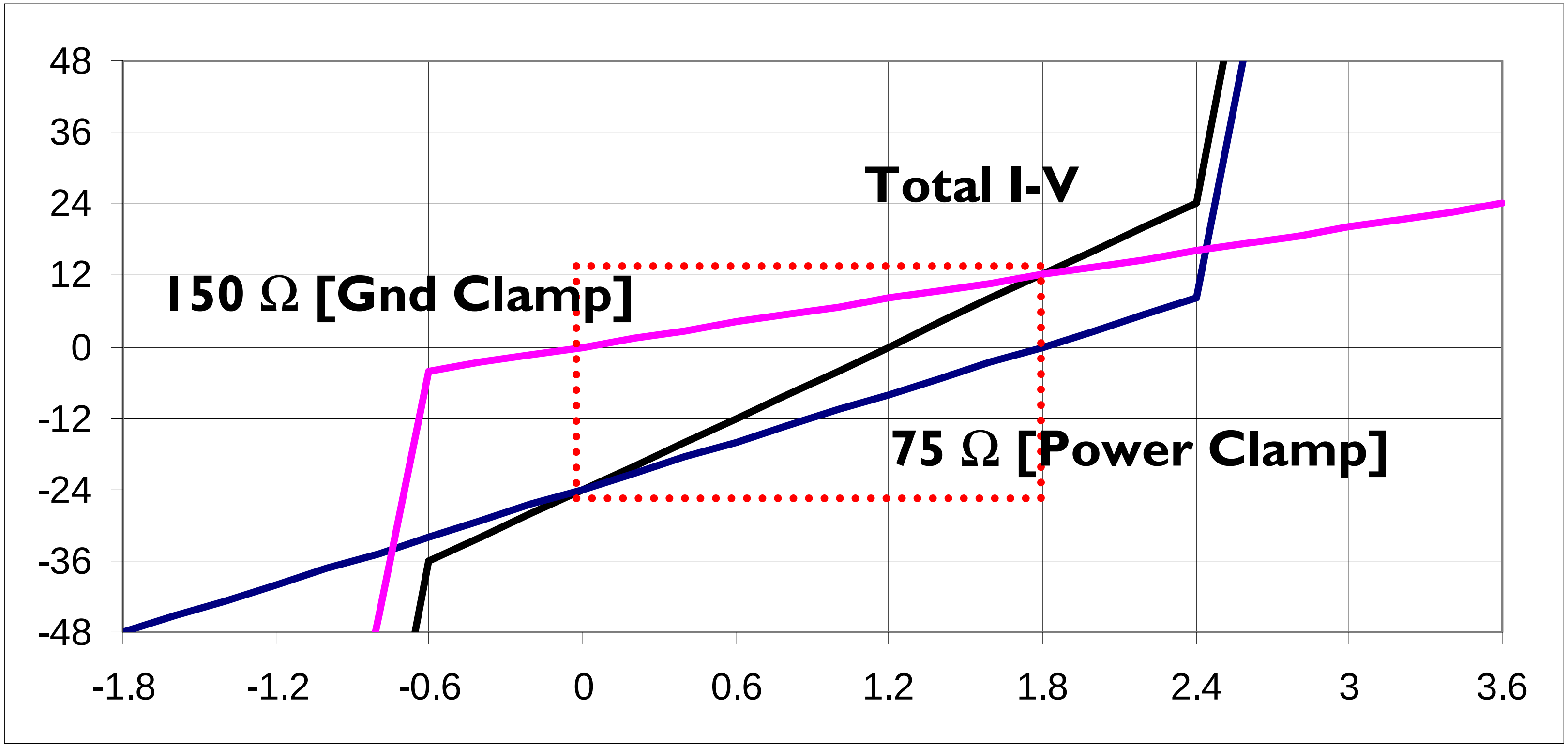
ODT Example (delta=0)



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DEC Observations

- Emulates ODT circuit for Vg and Vp changes
  - At I/O node, Thevenin 1.2 V shifts correctly, and source impedance = 50 Ω
  - Vp to Vg rail-to-rail impedance = 225 Ω
  - Diodes correctly anchored to Vg and Vp
- Supports single resistor ODT subsets
  - "pullup" ODT
  - "pulldown" ODT
- Backup slides for a suggested computation details
  - Typ-min-max data alignment
  - Vcc relative [Power Clamp] calculation
- Shape anchoring and internal reference overrides next

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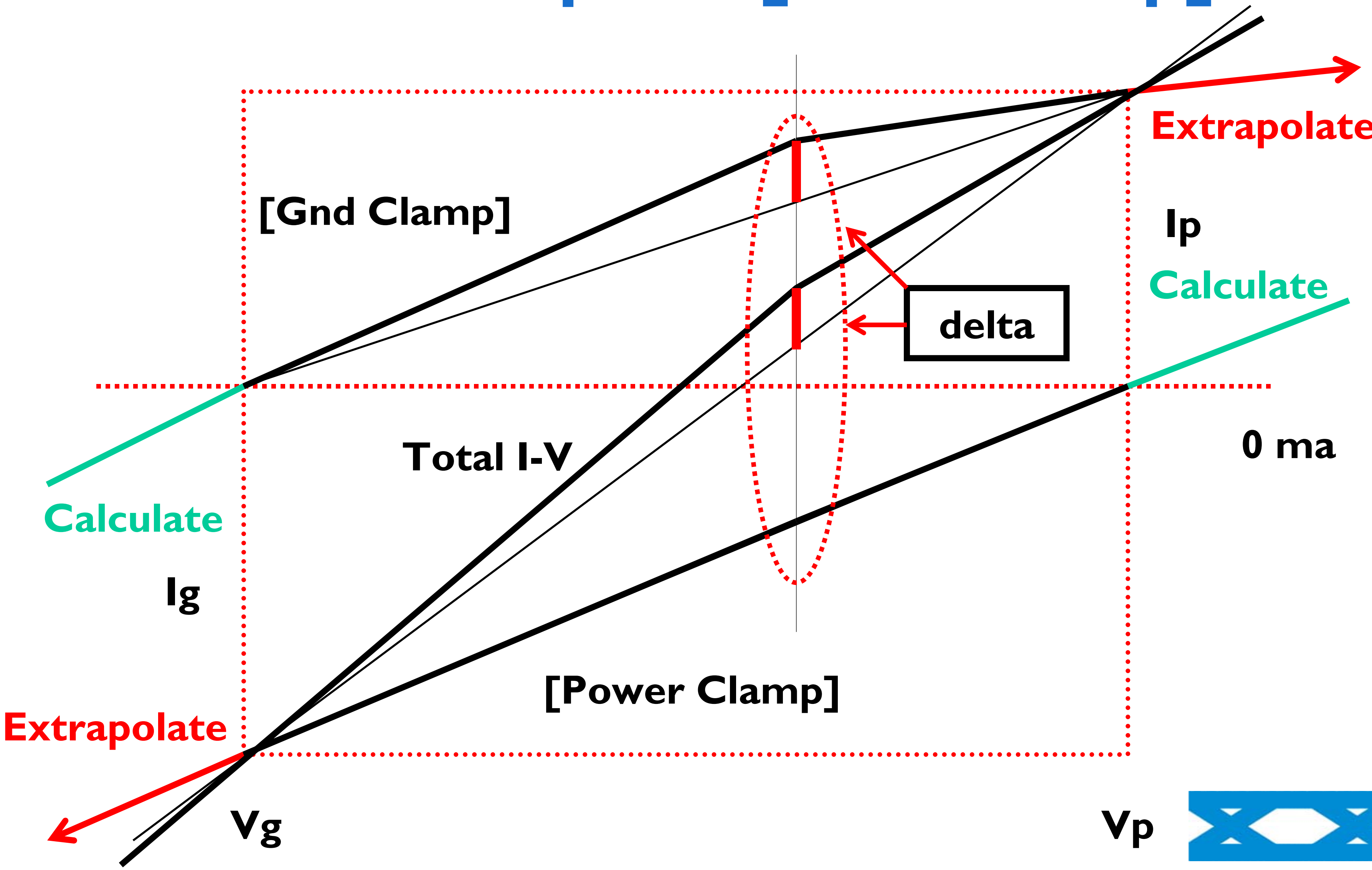
Anchor Shape to [Gnd Clamp]



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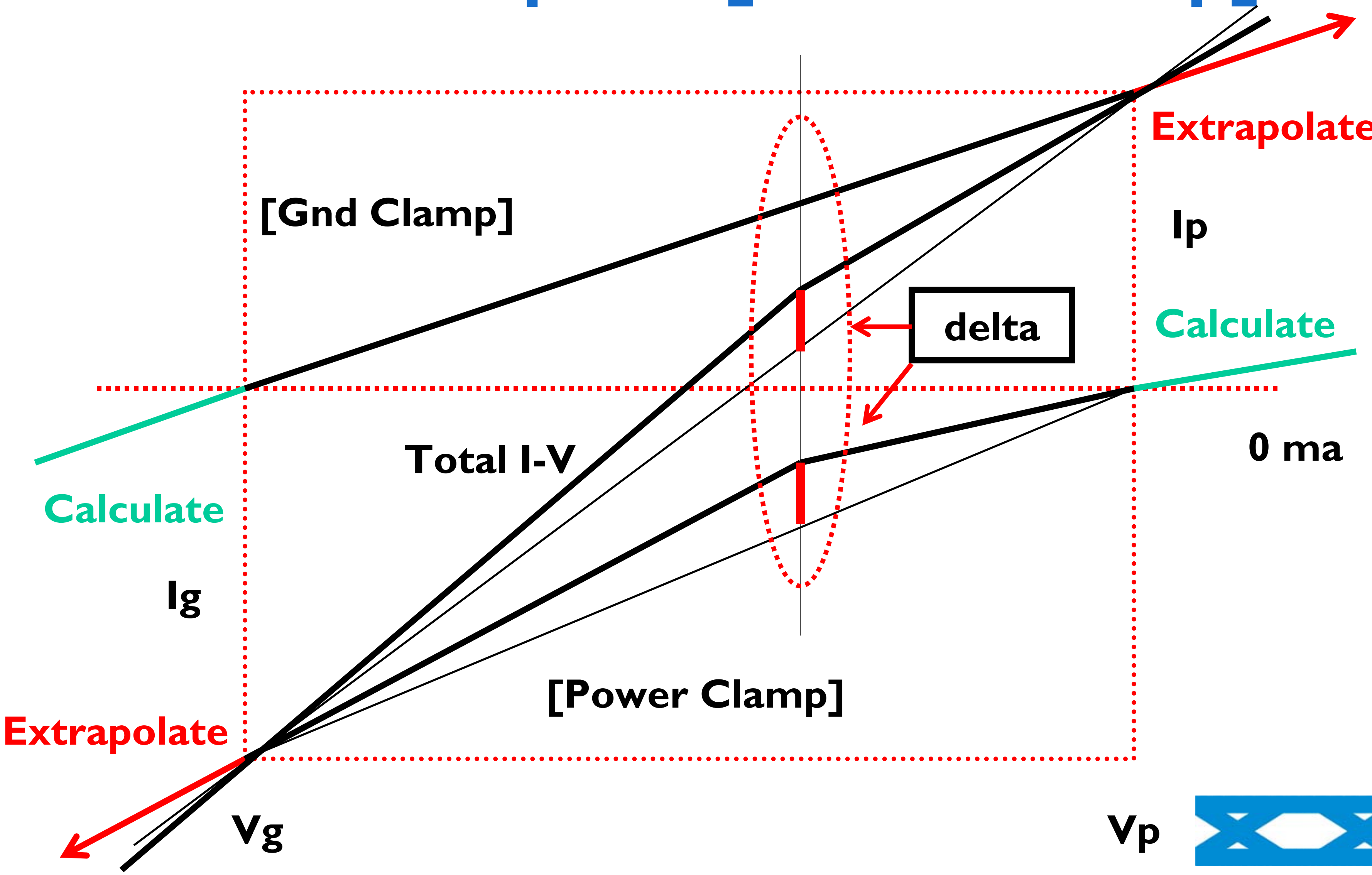
Anchor Shape to [Power Clamp]



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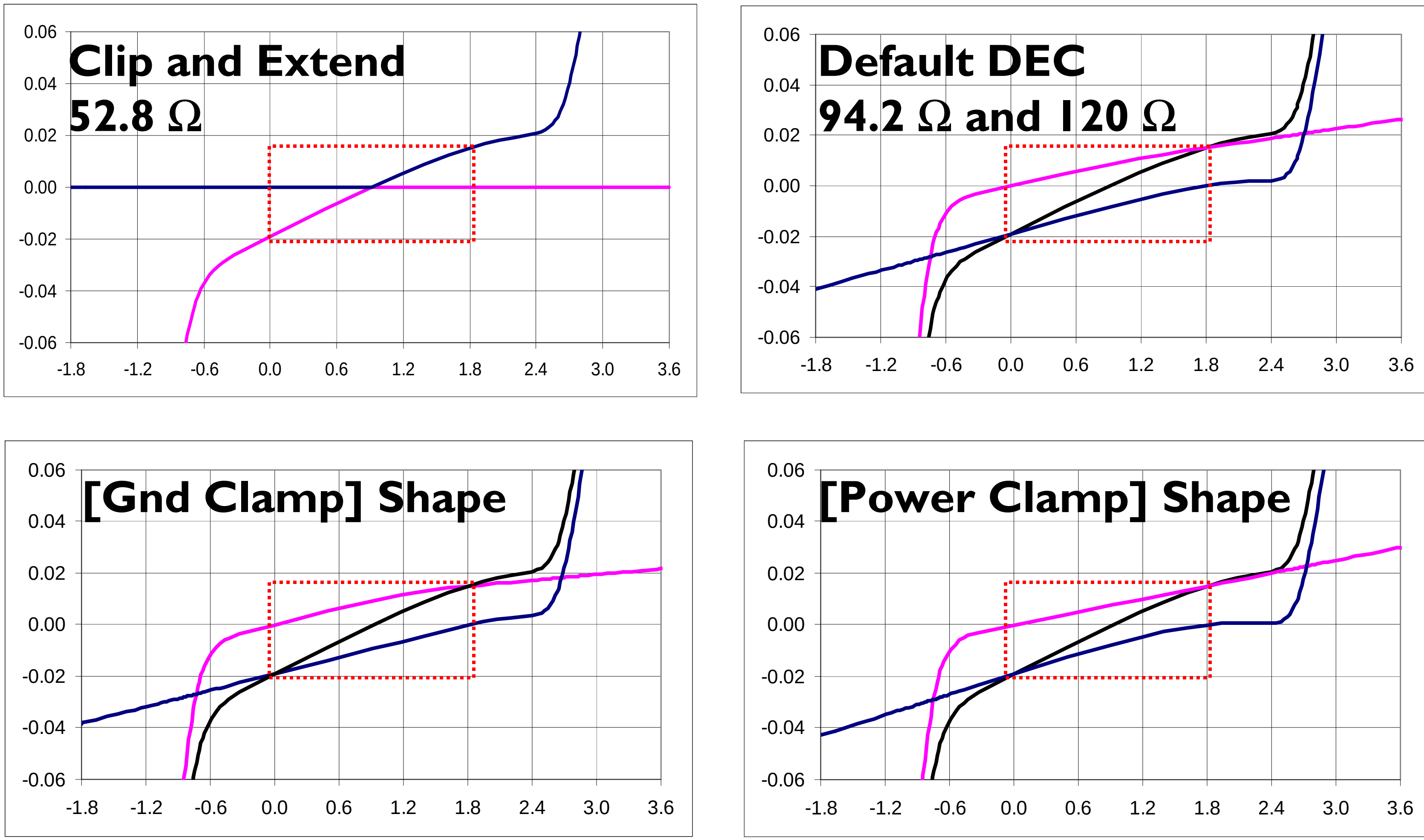
Real “50 Ω” ODT Choices



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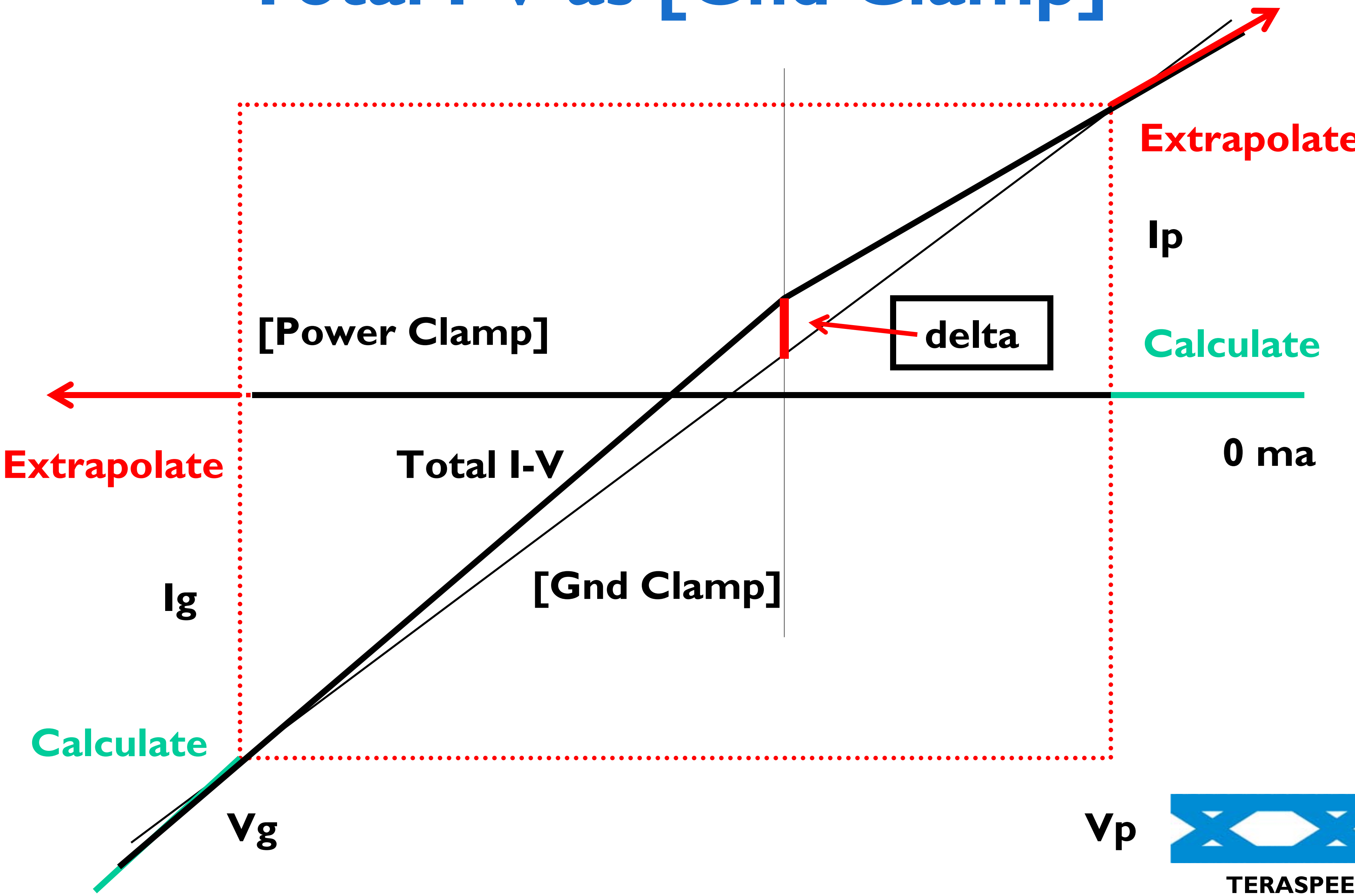
Total I-V as [Gnd Clamp]



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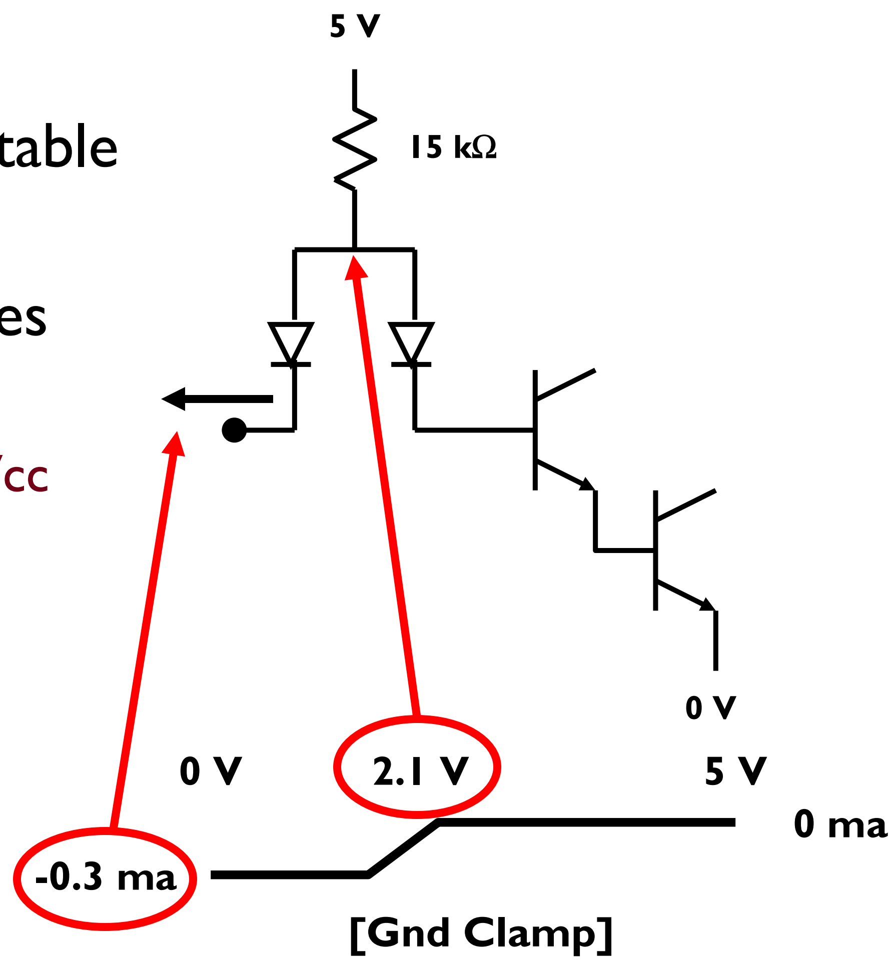
Application

- Total I-V in [Gnd Clamp] table tracks Vg changes
- For legacy IBIS "clip" ranges
  - [Gnd Clamp]: -Vcc to Vcc
  - [Power Clamp]: Vcc to 2*Vcc
- TTL Input: 2.1 V "diode" anchored to Vg per IBIS
- Current could have been anchored to Vp (default)
- Both anchors partially applicable



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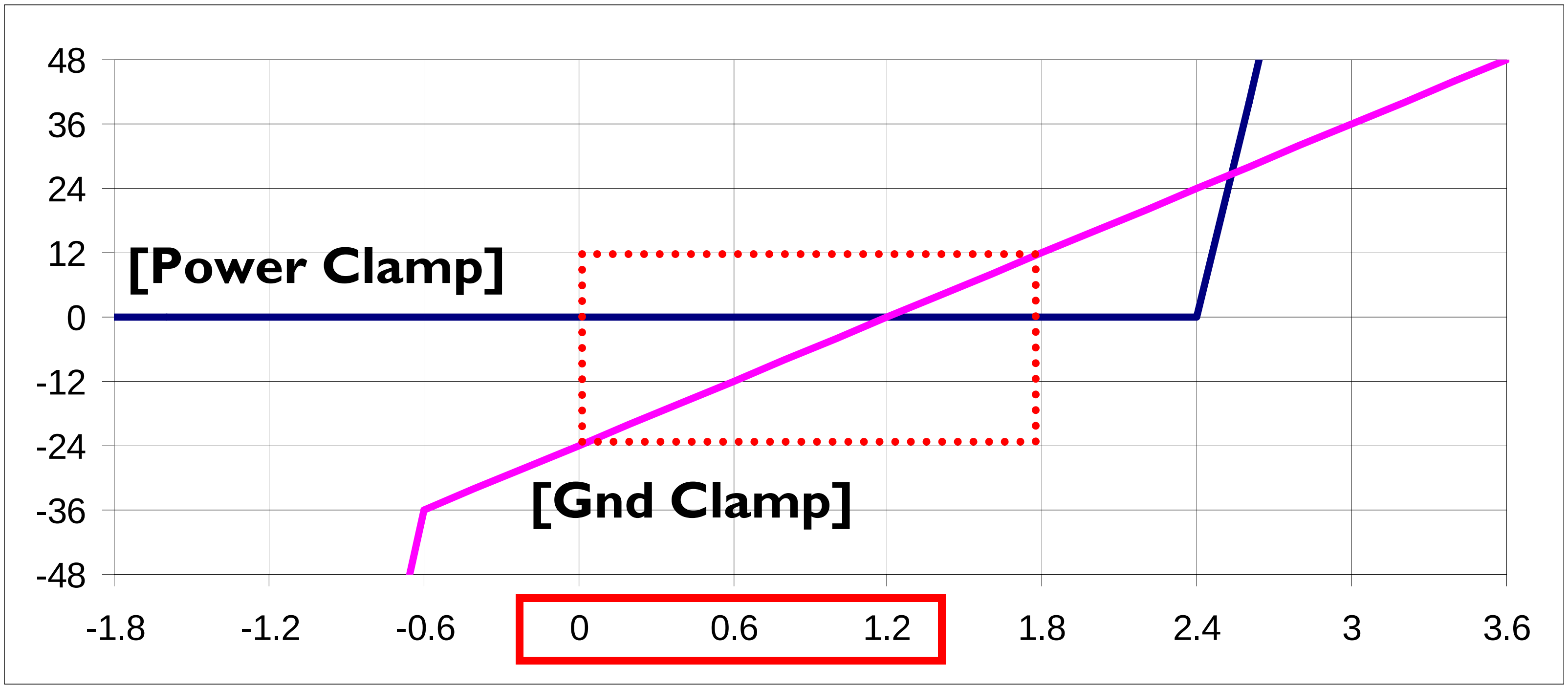
50 Ω, 1.2 V Anchored to Vg



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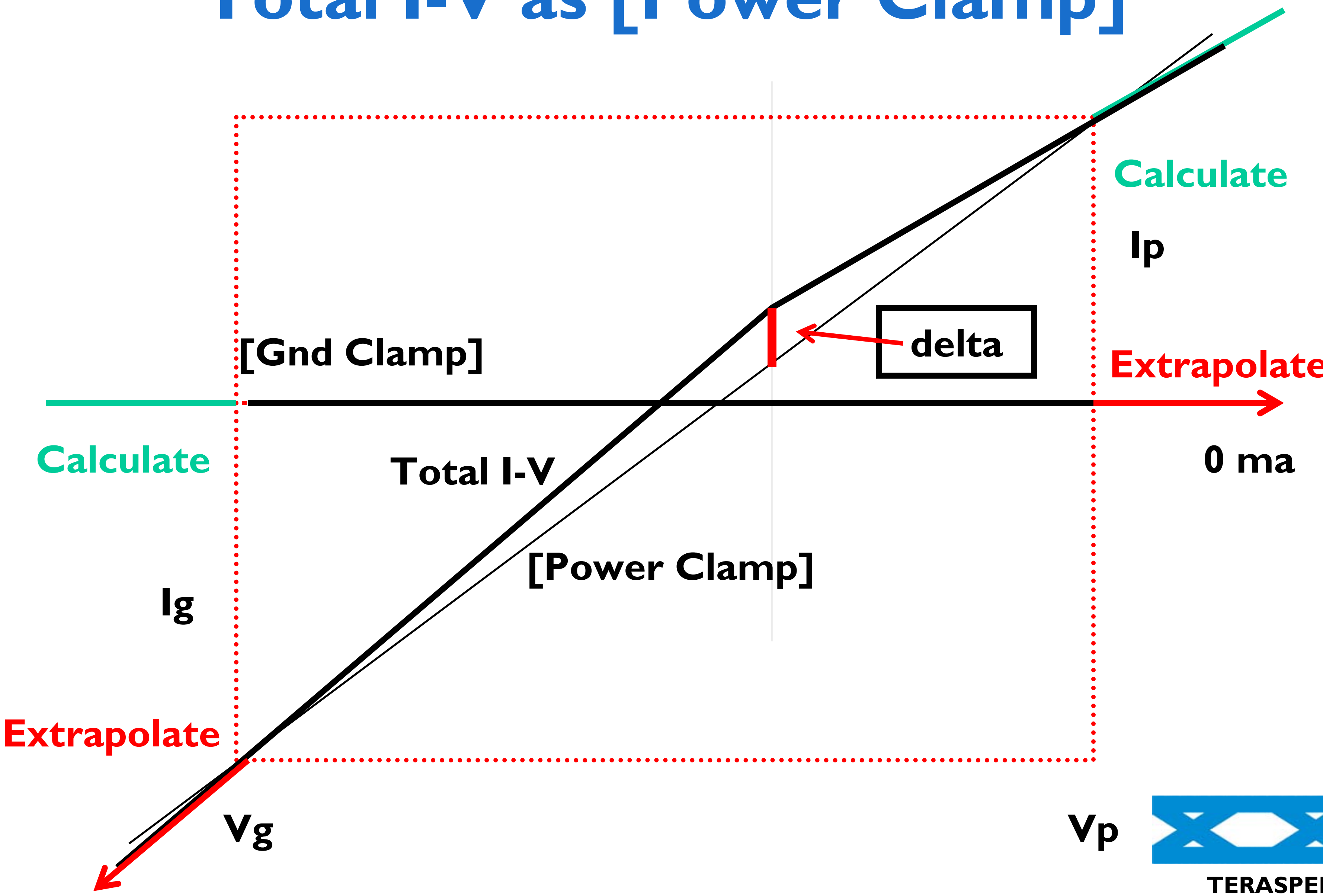
Total I-V as [Power Clamp]



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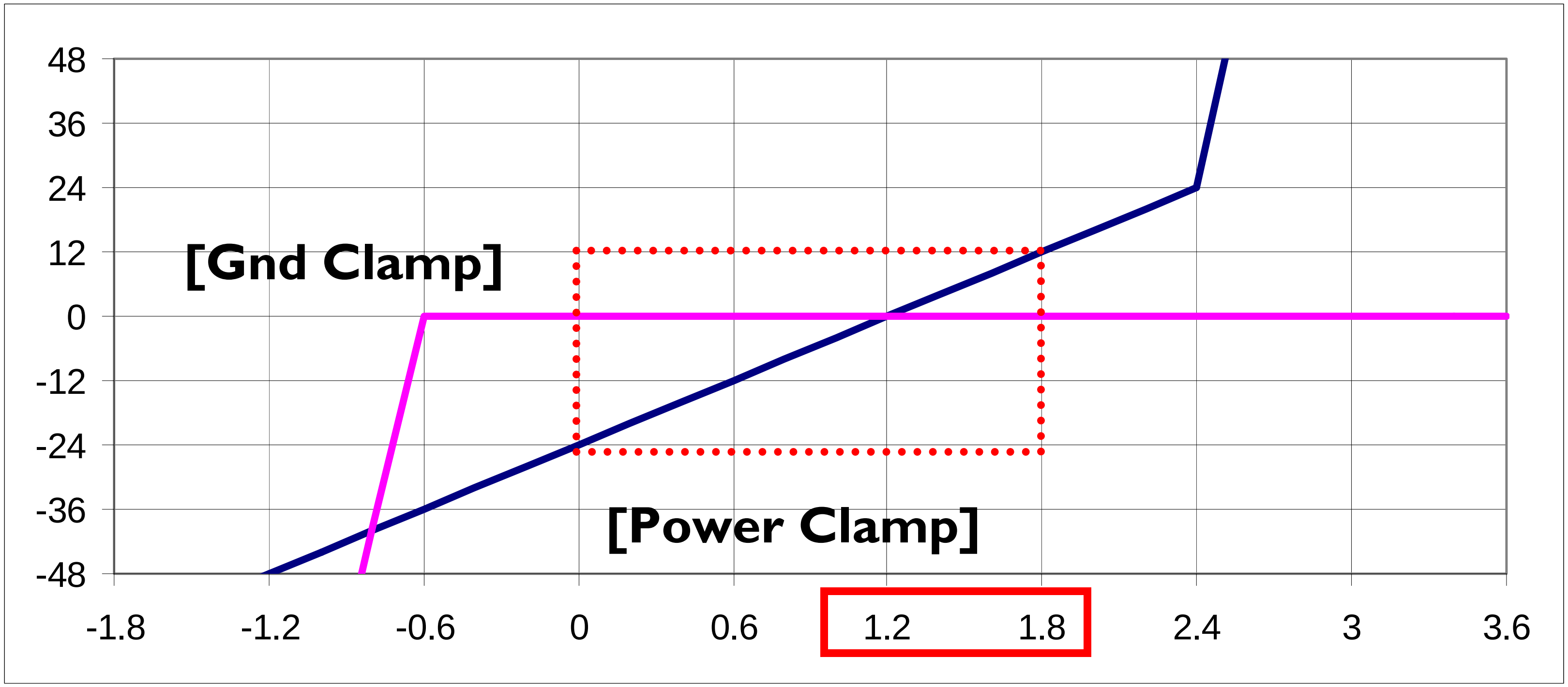
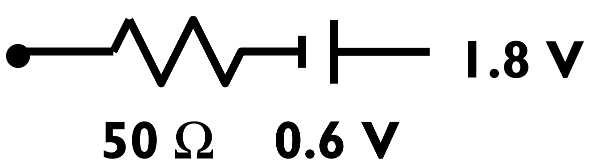
50 Ω, -0.6 V Anchored to Vp





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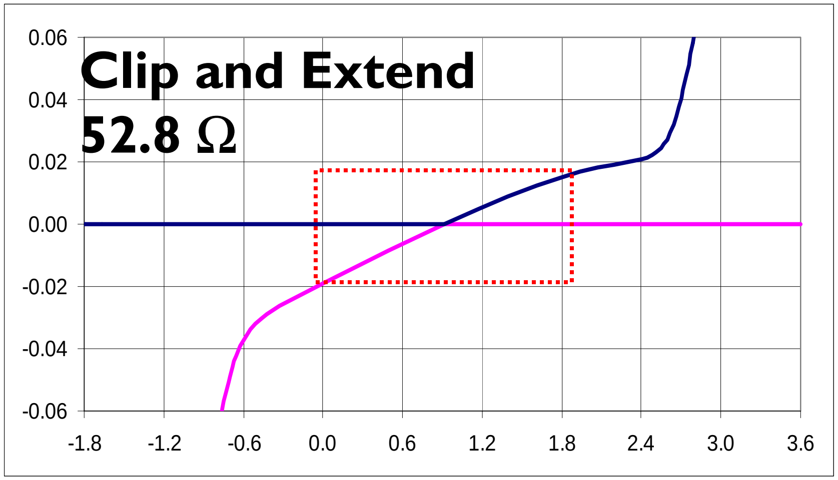
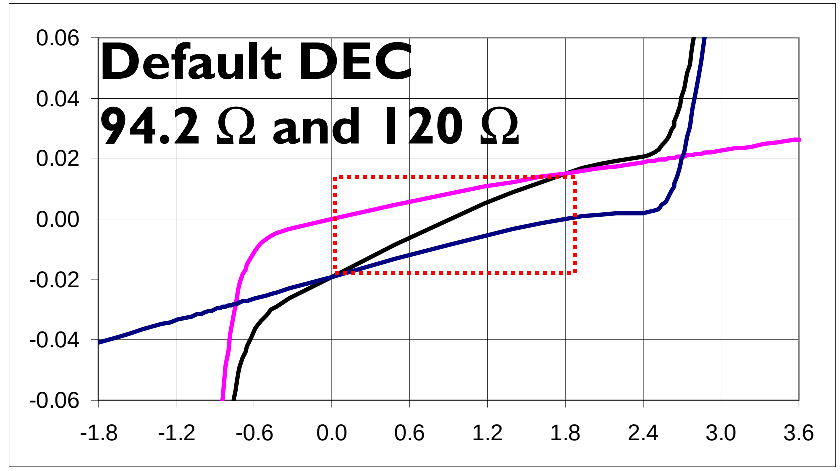
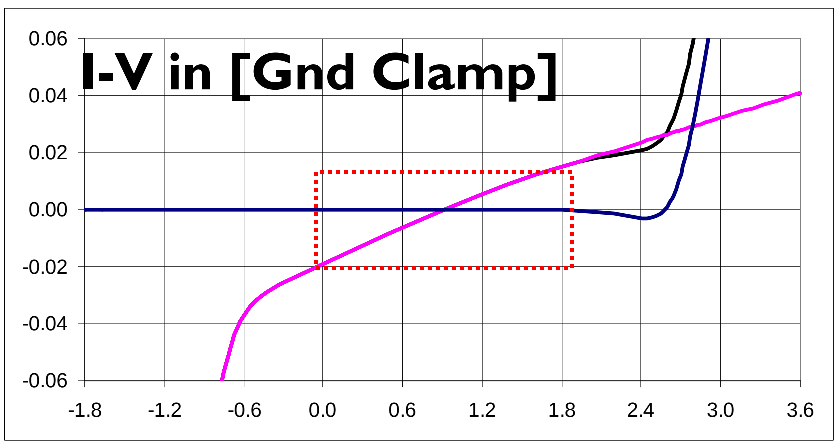
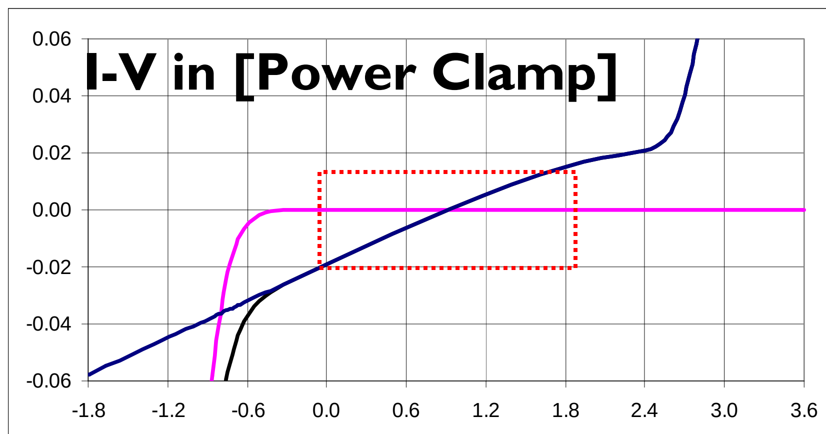
Real "50 Ω" ODT Choices









Shape between Vg and Vp

- In general Total I-V shape between Vg and Vp remains reasonable for Vg and Vp modulation
- DEC method applies for other reference shapes and other overrides
- Such as linear resistor partitioned into quadratic components next

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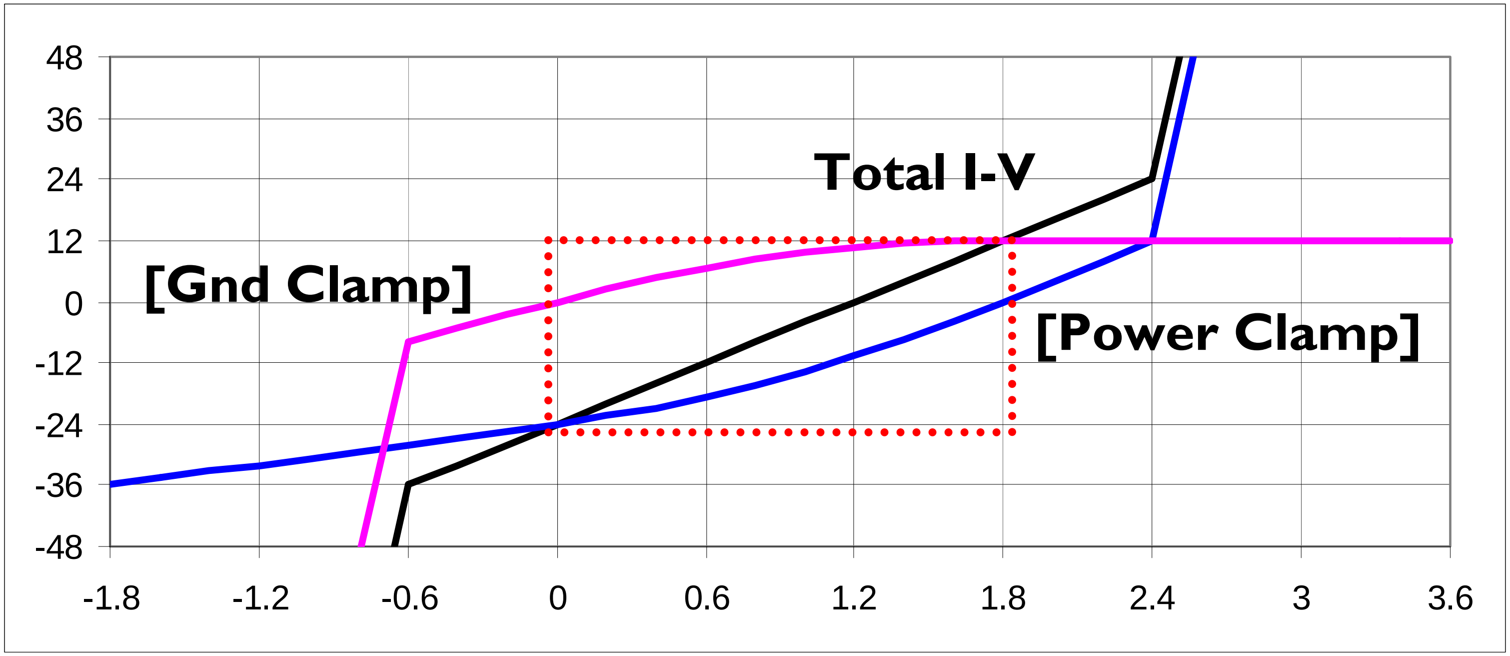
Quadratic Clamps



- Linear Thevenin terminator with "quadratic" resistors
  - [Gnd clamp] chosen with slope = 0 at Vp
  - Use same Extrapolate and Calculate rules

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Conclusions

- Many choices exist to partition an I-V table into clamp tables
- DEC algorithm based on ODT resistor deviation covers practical cases
- Overrides shown, based on additional knowledge (could be expanded)
- DEC favored over "Clip and Extend" for accuracy, robustness, and portability

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Backup – Suggested Calculations

- Uses both a Vg (Gnd) referenced Total I-V and a Vp (typ, min, max Vcc) referenced Total I-V
  - Typ, Min, Max for each case
    - From –Vcc to 2*Vcc
    - Same sample points aligned for typ, min, max data
  - [Gnd Clamp] uses Vg referenced data
  - [Power Clamp] uses Vp referenced data
  - (One Total I-V table could be calculated from the other over a larger sweep range to get aligned data)
- DEC – Extrapolate 0 to –Vcc, Calculate, do simple extrapolation above Vcc to 2*Vcc

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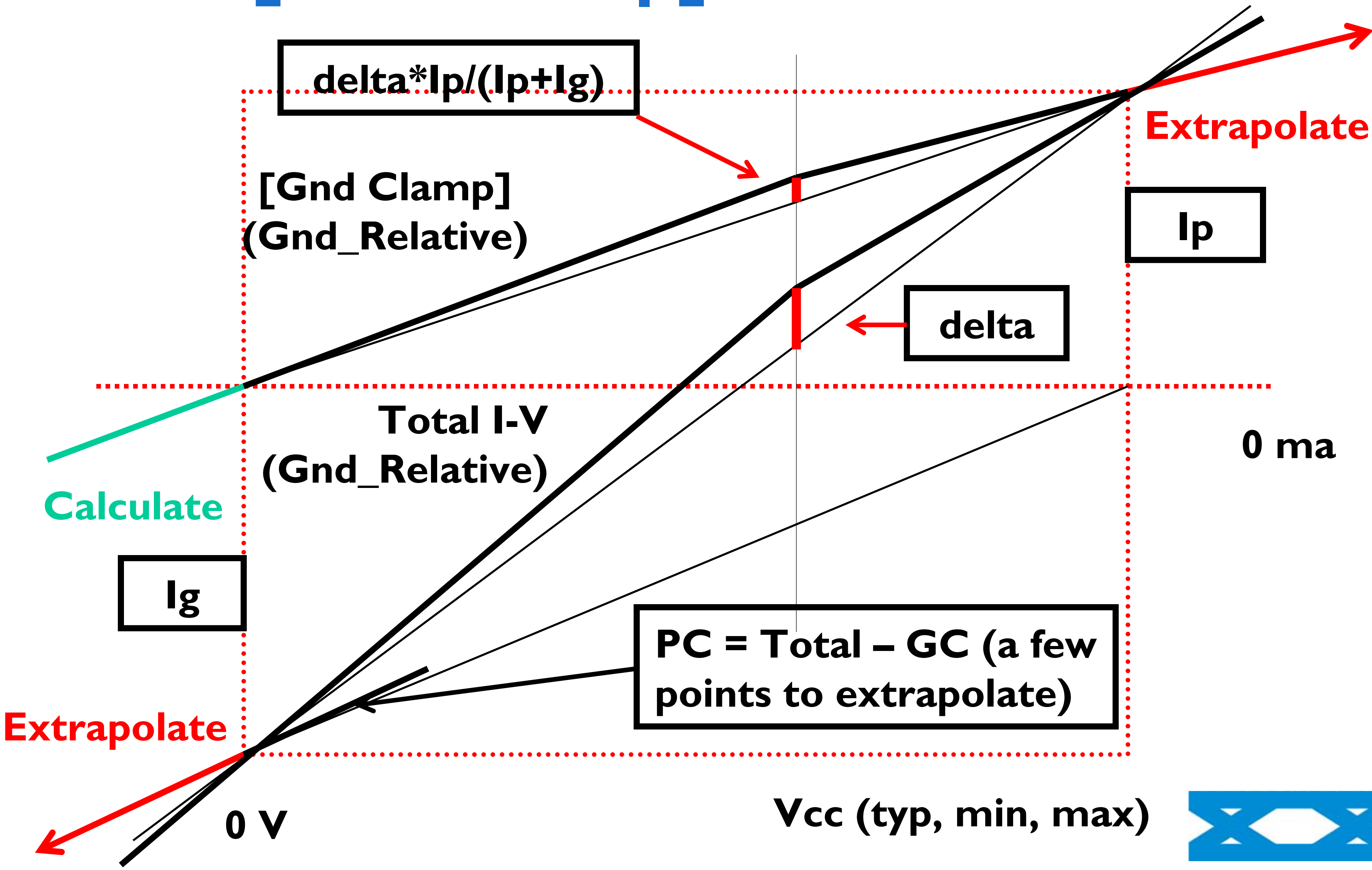
[Gnd Clamp] Calculation



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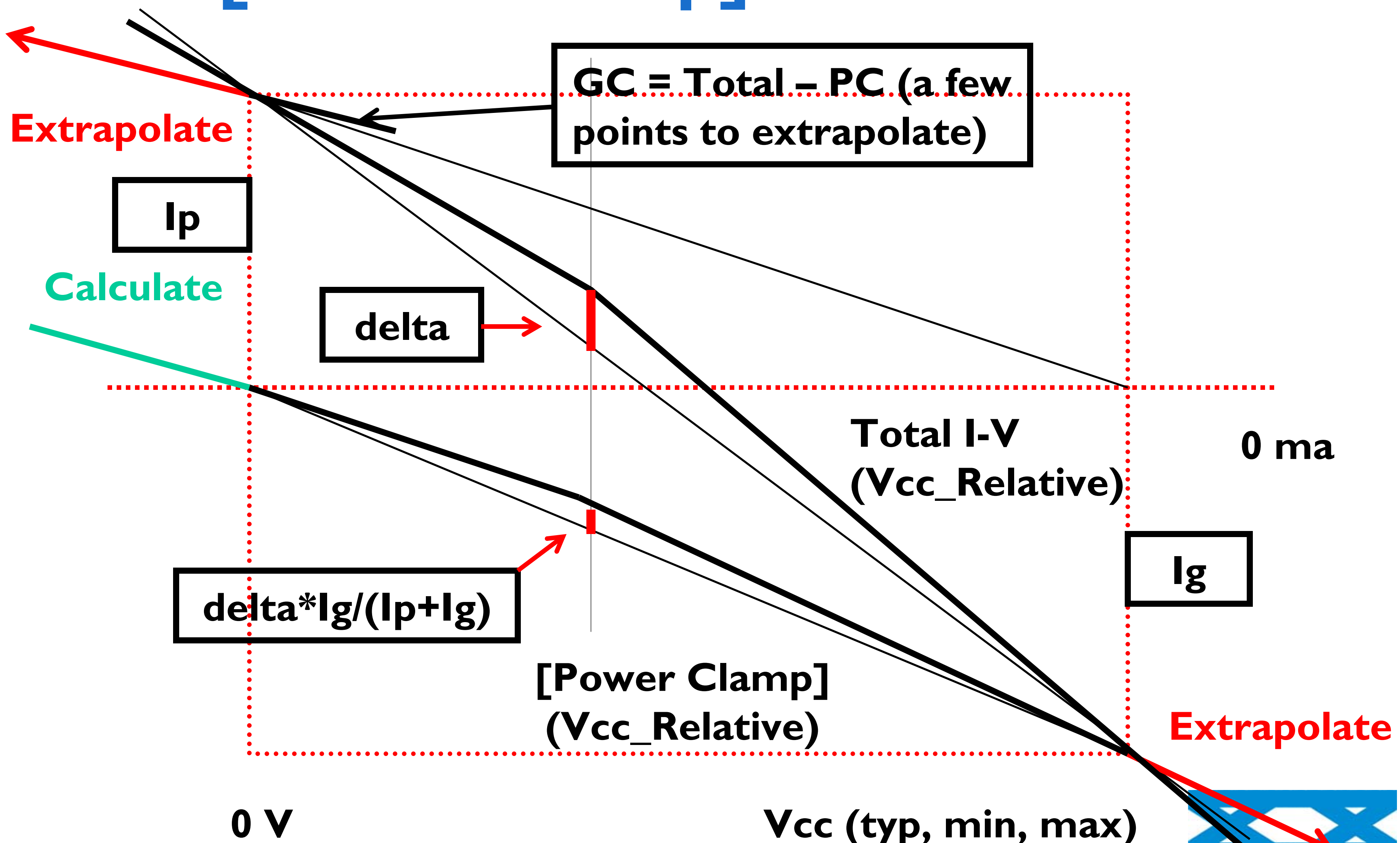
[Power Clamp] Calculation



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Comments

- Extrapolations below 0 V
  - Based on extrapolating a few calculated points
  - All data points at Total I-V voltages
- Extrapolate above Vcc (typ, min, max)
  - The typ and min columns need entries or NA's to Vcc (max)
  - Extrapolate columns to 2*Vcc
    - Fill in remaining values
    - Optionally, one value at 2*Vcc

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