Version 3.2 Experience Modeling
Fast, Two-tap Pre-emphasis Buffer

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GROUP

The Project Constraints

- Semiconductor vendor
  - Two-tap pre-emphasis buffer with On-Die Terminator (ODT)
  - "Cannot be done in IBIS"
  - Encrypted HSPICE under 3-way NDA
- Customer (required IBIS Version 3.2)
  - For specific IBIS tool (with no HSPICE access)
  - Tool supports [Driver Schedule]
  - Minimal customer IBIS knowledge
- Business issue (several final deliverables)
  - Two week delivery for four CML differential buffers within full 400+ pin ASIC model … after legal contract closure delays
- Tips, experiences and unexpected issues here

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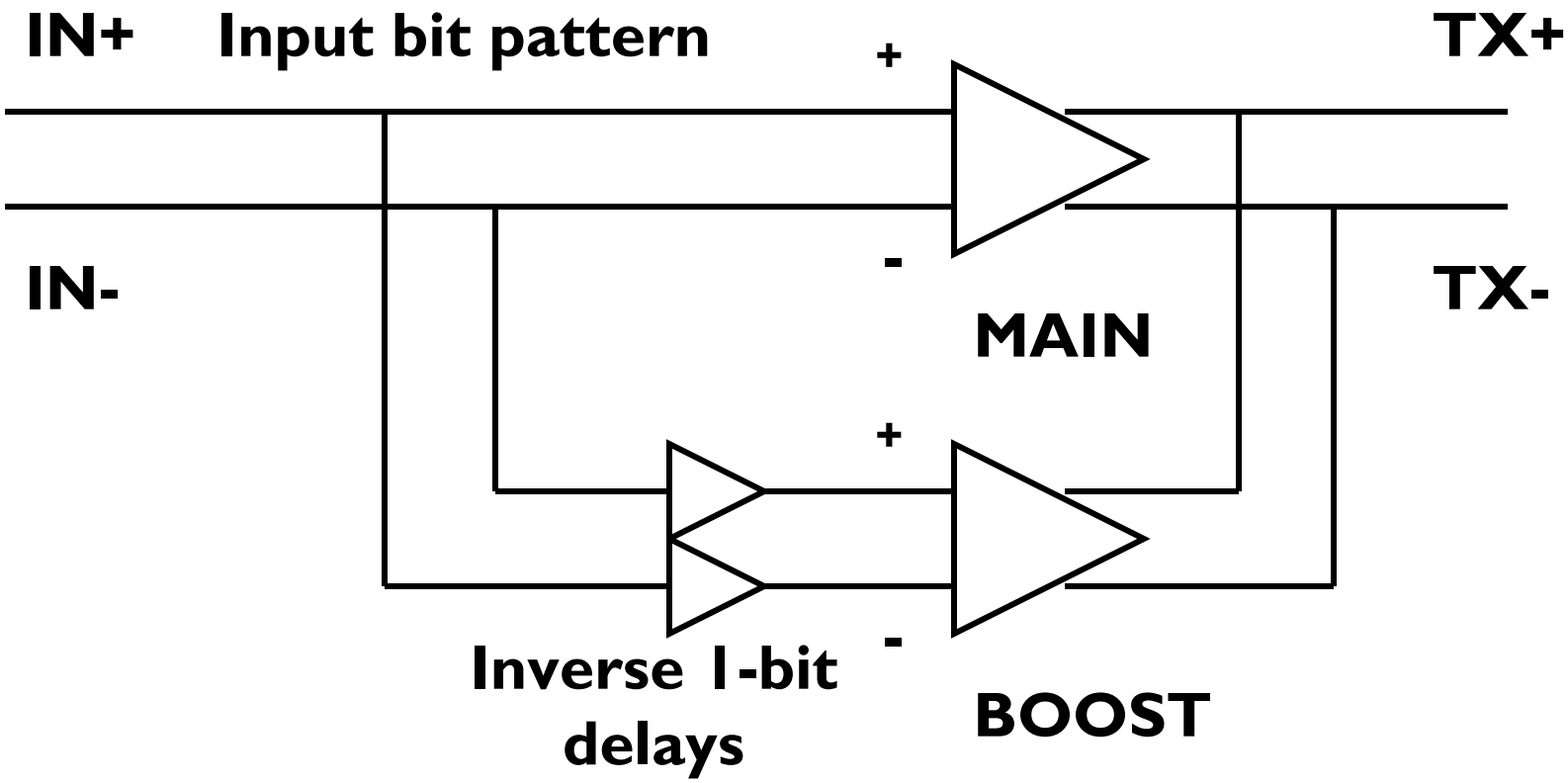
Other Related Discussions

- Arpad Muranyi, March and January 2005, April 2004,
  - Either enhanced or reduced buffer switched in
  - Or main and one-bit delay boost
  - Six individual edges and state machine for *_AMS solution with C_comp
- Hazem Hegazy, LVDS Modeling, June, 2001
  - Either enhanced or reduced buffer switched in
- Michael Mirmak, C_comp Issues, October and April, 2004
  - Factored out C_comp from V-T tables, but more work needed
- Used Cookbook [Driver Schedule] pre-emphasis method
  - Main and one-bit delay boost
- Highlights of real issues, not the full process

Project Factors

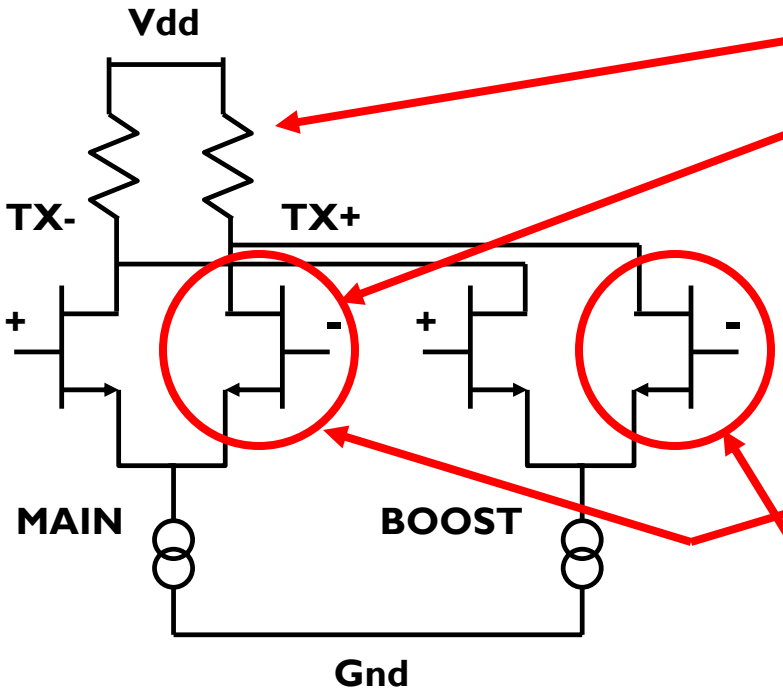
- Process overview
  - Isolate, test SPICE model from limited documentation
  - Set up some SPICE extraction programs
  - Set up spread sheet calculation pages for processing all the buffer setups
  - Resolve unexpected situations
  - Test the prototype IBIS buffer in the EDA tool
  - Refine and deliver
- Customer goal was timely design exploration
  - No time for "perfect" solution or extensive research
  - Compromises needed

SPICE Configuration, Differential Control and [Driver Schedule]



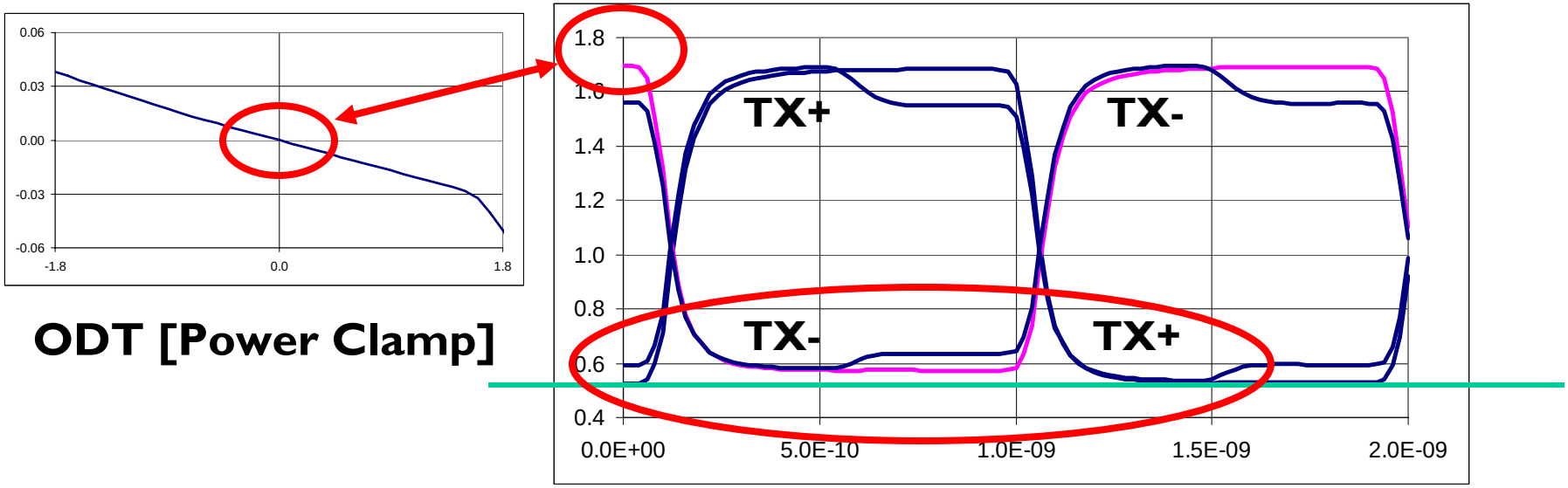

```
[Driver Schedule]
| Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly
MAIN         0           NA           0           NA
BOOST        NA          0.47059ns    NA          0.47059ns
```

CML Structure with IBIS Open_drain Models, Connected by [Diff Pin]



- Top-level
  - ODT [Power Clamp]
  - MAIN [Pulldown]
    - Extracted waveforms with ODT & 50 Ω
    - Pre-emphasis = 0
  - [Driver Schedule]
- MAIN [Pulldown]
  - Scaled waveforms
- BOOST [Pulldown]
  - Scaled waveforms

Unexpected SPICE Offset and TX+ and TX- Differences



- [Power Clamp] ODT predicts no offset from 1.8 V
  - Added top-level [Gnd Clamp] to compensate for offset
  - Some configurations go to 1.8 V
- TX+ and TX- different, but no reason to model this
  - SPICE code appeared symmetrical
  - Used TX+ extractions as reasonable approximation

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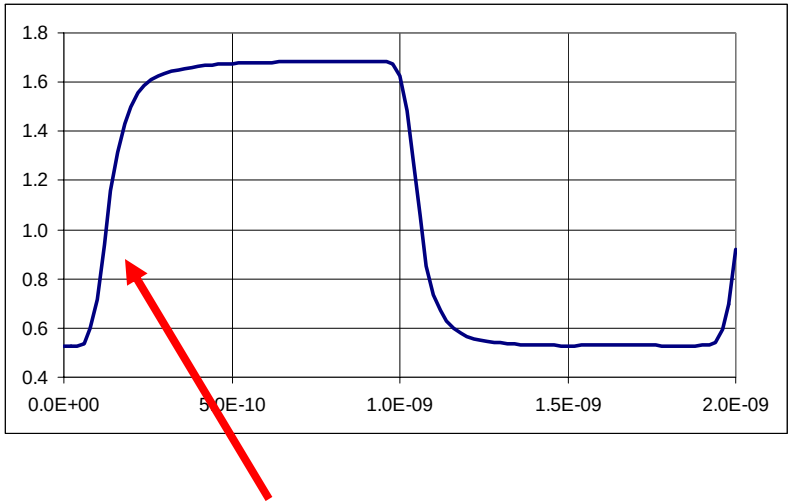
SPICE TX+ and I-V Tables

- Aligned SPICE typ-min-max I-V sweeps to get ODT as a [Power Clamp] and MAIN and BOOST [Pulldown] tables by subtraction
  - ODT: High-state MAIN only for [Power Clamp]
  - ODT+MAIN: Low-state MAIN for [Pulldown]
  - ODT+BOOST: Low-state BOOST for [Pulldown]
- Removed (out of range) non-monotonic data
- Top-level [Gnd Clamp] mismatch adjustment for actual "1.8 V" high side levels, when needed

Time Extraction from TX+

- 50 Ω to 1.8 V, no pre-emphasis captures MAIN plus ODT reference waveform
- Set R_fixture=25 Ω for MAIN and BOOST Open_drain buffers
  - Used ibischk4 to determine low end-point of swing (high is Vdd)
  - Scaled the reference waveform
  - Keeps MAIN over about same voltage range
  - Correlates MAIN, BOOST delays
  - C_comp=0 pF (more later)



Reference waveform for TX+ rising edge

(Falling edge reference for TX+ not shown)

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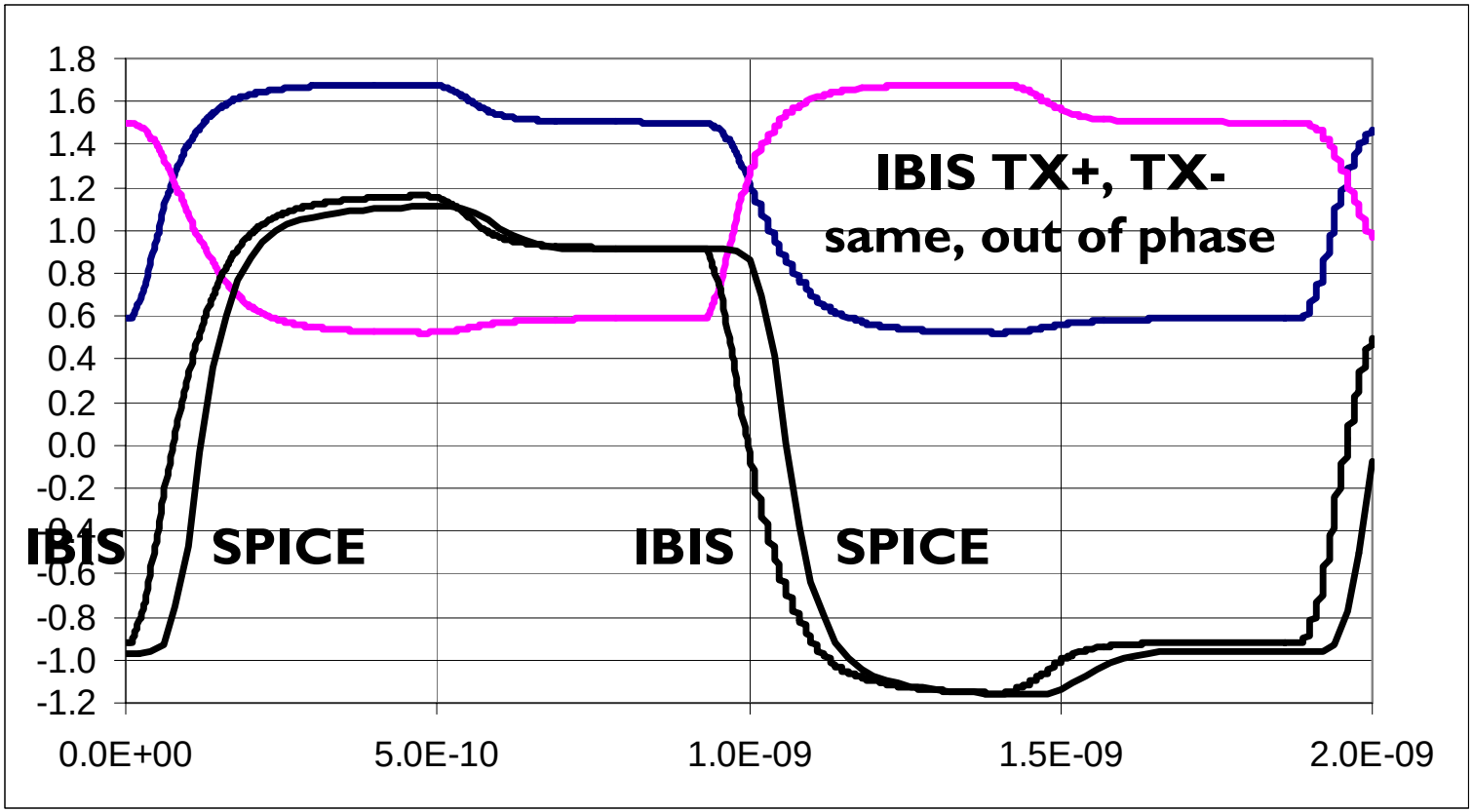
Unexpected Correlation Issues



IBIS leading edge truncation and slope difference skews

Ending levels near (non-symmetrical) SPICE levels

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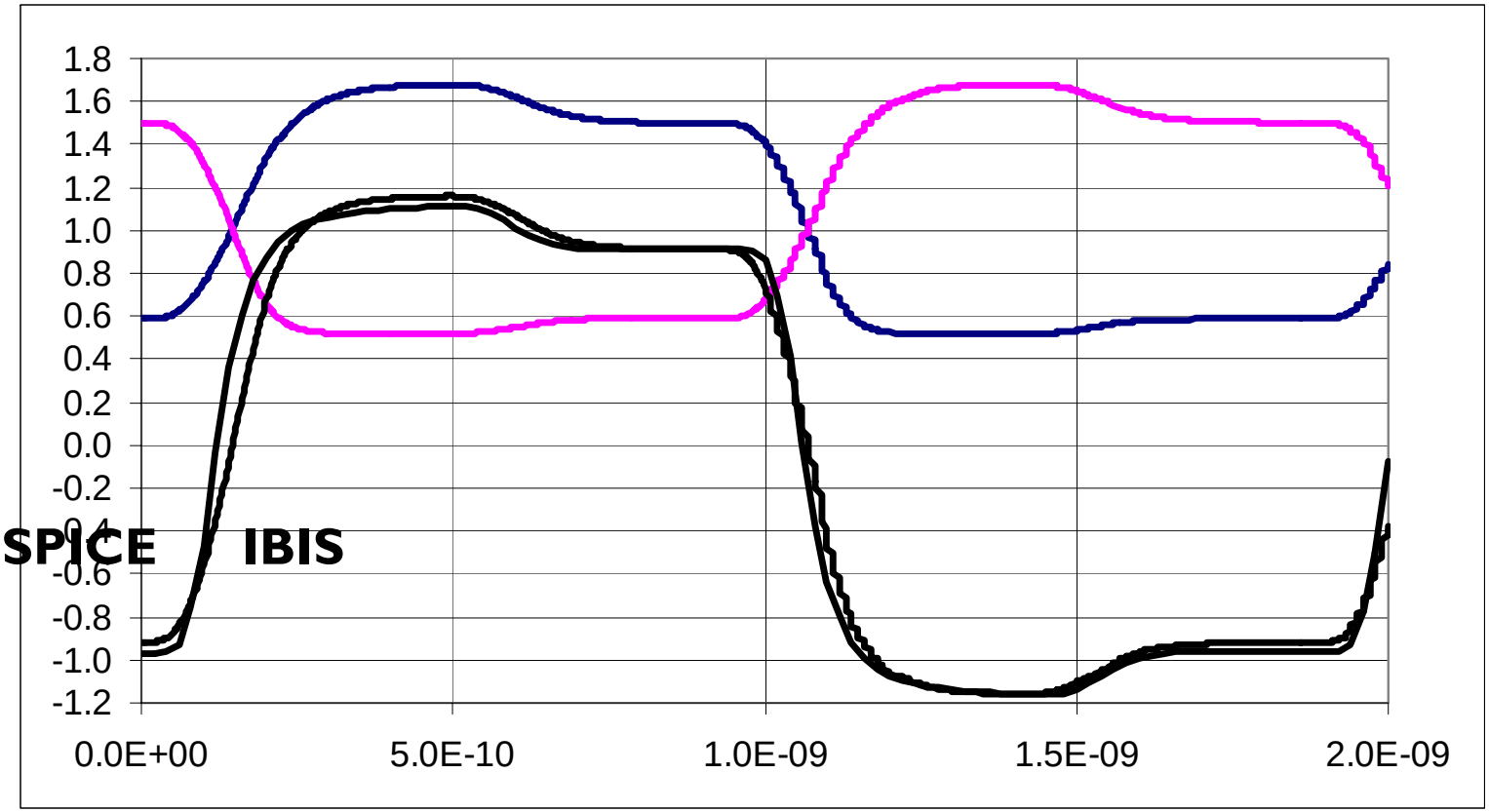
Tested with C_comp (later)



Unexpected IBIS shift without response degradation

Either a tool or tool setup issue, but could produce better (tool dependent) results

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Expected C_comp Degradation

- C_comp in IBIS [Driver Schedule]
  - IBIS should add C_comp as top-level load
  - Buffer impedance reduces driving mode degradation
  - (Bad??) IBIS choice
- Up to 3 pF, 25 Ω = 75 ps time constant or about 165 ps rise time degradation (less with pulldown impedance)
- Simulation rise time of less than 100 ps
- Total rise time approximately sqrt ($t_1^2 + t_2^2$) or 193 ns (or less)

Further C_comp Investigation

- Compensate using C_fixture with R_fixture
  - Algorithm could use total specified loads (C-fixture, L_fixture, R_fixture, V_fixture, C_dut, L_dut, R_dut)
  - Or simplified with C_fixture (C_dut) added to C_comp – no change in mathematics
  - Use same waveforms
- Add C_fixture to both MAIN and BOOST waveform tables (but keep C_comp=0.0 pF)
- Use only top-level C_comp
- Extra MAIN, BOOST capacitive currents drive top-level C_comp
- (Similar programmed approach, which still needed further tuning, Mirmak, 2004)

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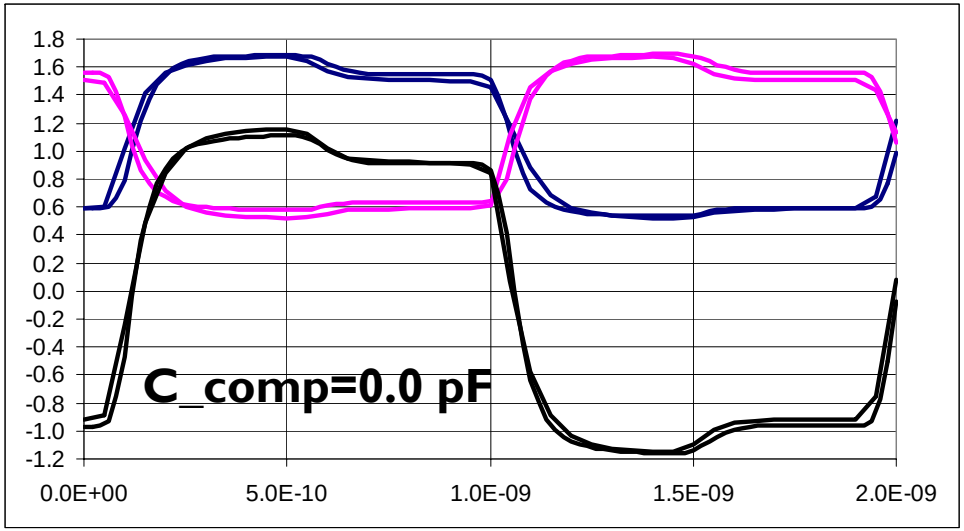
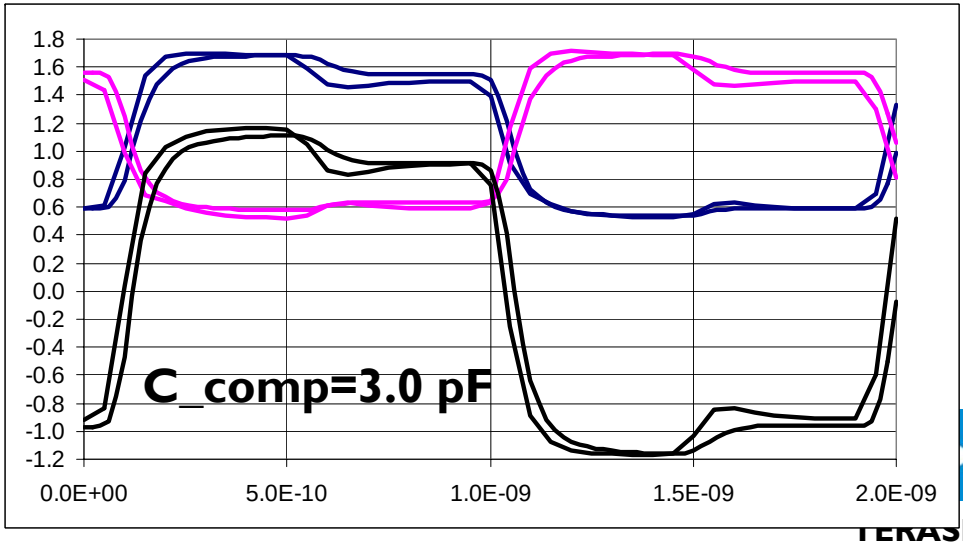
Investigation with Another IBIS Tool

- C_comp=0.0 pF
  - Better delay correlation with SPICE
- C_comp=3.0 pF
  - C_fixture=3.0 pF
  - Left shifted edges and some distortion
  - Promising approach





More C_comp Comments

- Why Top-Level C_comp
  - Simple, known receiving mode C_comp for I/O
  - Avoids inheritance of all Driver Schedule C_comps question
    - Is it always there or under certain scheduled conditions?
  - Avoids estimating C_comps for scheduled buffers
- Other C_comp issues
  - Voltage dependent, frequency dependent (or effective reactance)
  - Can be split among rails
  - Driving and receiving modes differences not supported
  - C_comp corners specified by magnitude rather than correlated with process, temperature, voltage
  - Plus differential C_comp issues
- So C_comp is an effective value, and refinement requires many IBIS additions

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Conclusions

- Unresolved (further checking) issues
  - Reasons for SPICE model issues
  - Possible tool setup and operation issues
  - C_comp tool issues
- C_comp handling within [Driver Schedule] approach could be improved
- IBIS Version 3.2 model satisfied customer's immediate needs
- Unfortunately, target EDA tool(s) and operation remain a practical consideration