IBIS “Over Clocking” Case

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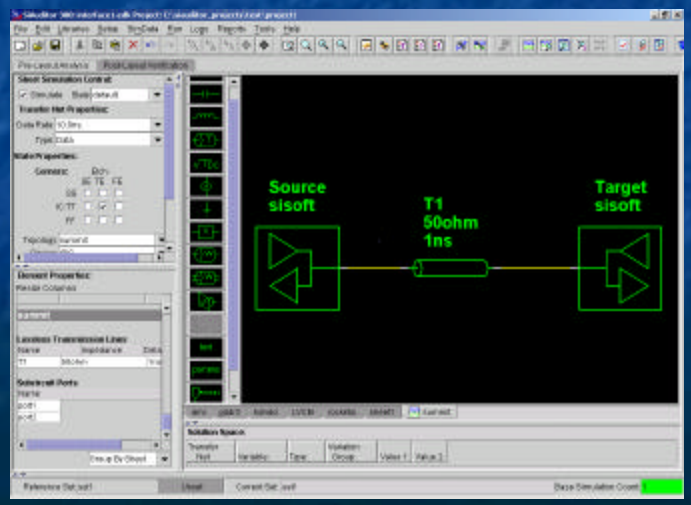

When Does “Over Clocking” Occur

- VT curve time comparable to simulation data rate
  - Excessive Dead time in VT curves
  - Large variation between Slow and Fast VT Curves
- Results in Unpredictable Simulator Behavior
  - i.e. SPICE
  - Others ?

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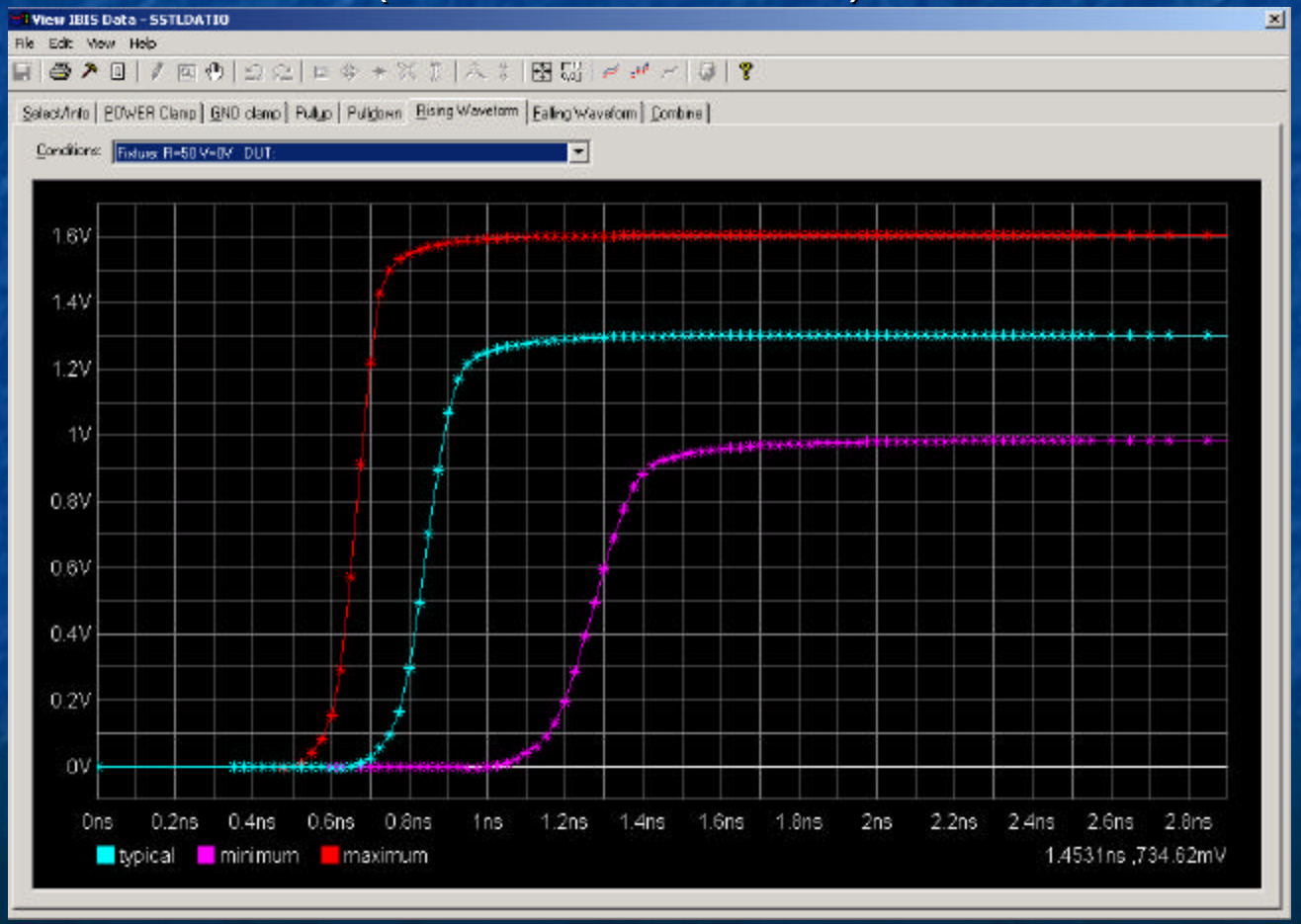
Example VT Curve

- VT curve time small versus data rate (Final DC levels ~ 3.5ns)
  - 1 of 4 VT curves shown (Rise, Fall, VDD, Ground) ~ 1ns Delta



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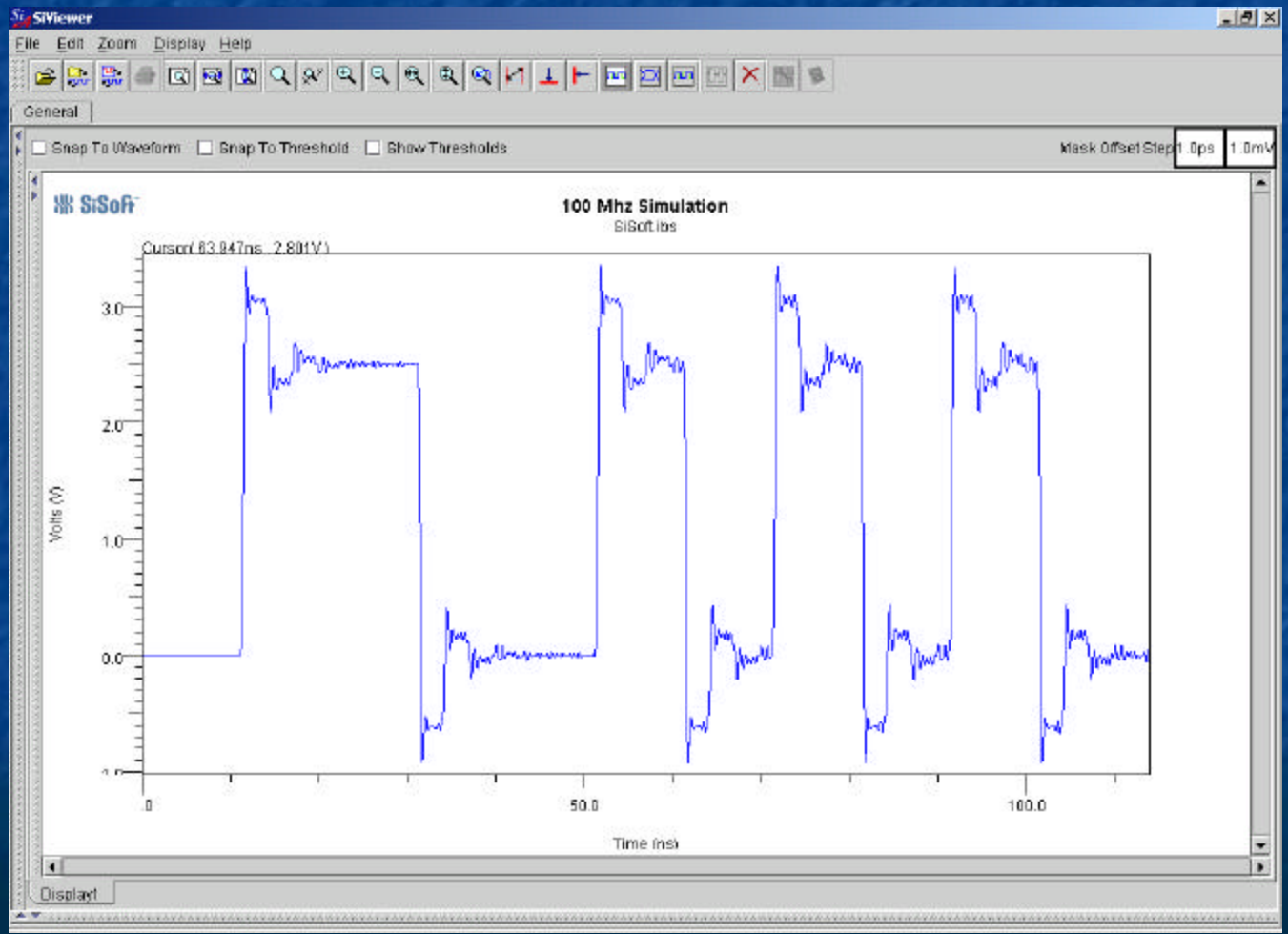
Example Simulation

- Simulation results 100 MHz (10ns Cycle time, 5 ns Data rate)



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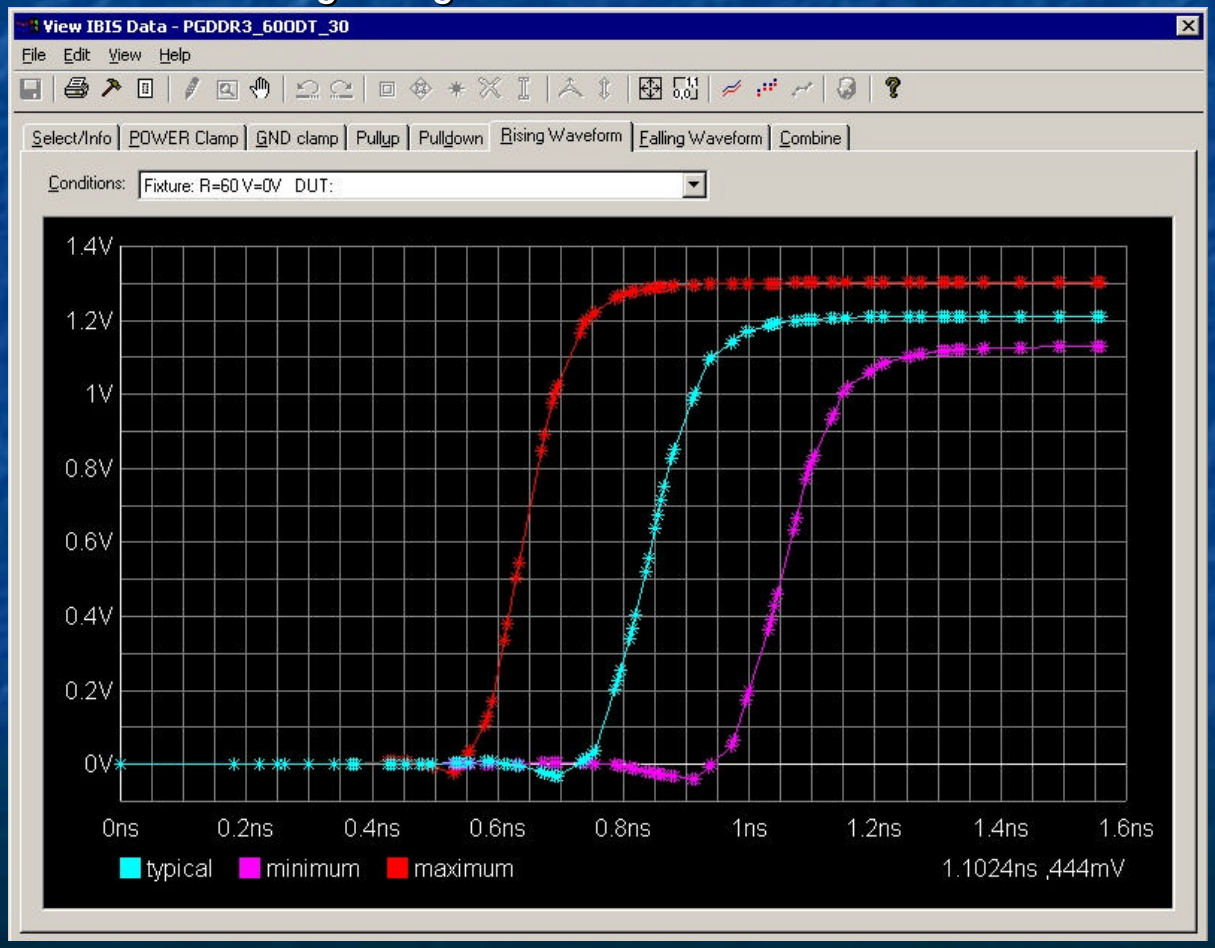
Over Clocked Case – VT Before

- VT curve time comparable to data rate
  - Large delta between beginning of Fast and end of Slow Process corners ~.7ns



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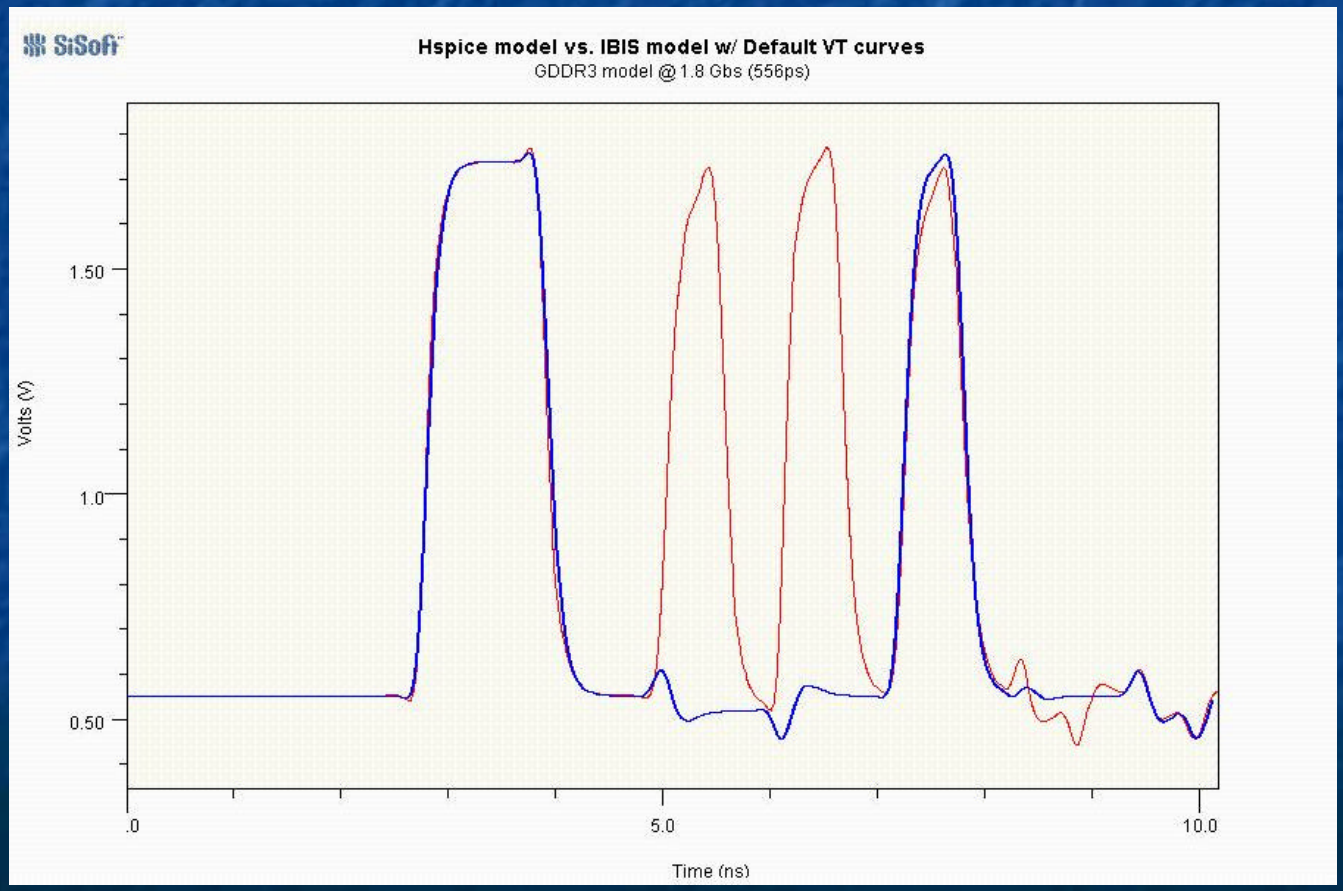
Over Clocked Case – Simulation Before

- Hspice versus IBIS Correlation
- Simulation results 1.8 GHz (0.556 ns Data rate)



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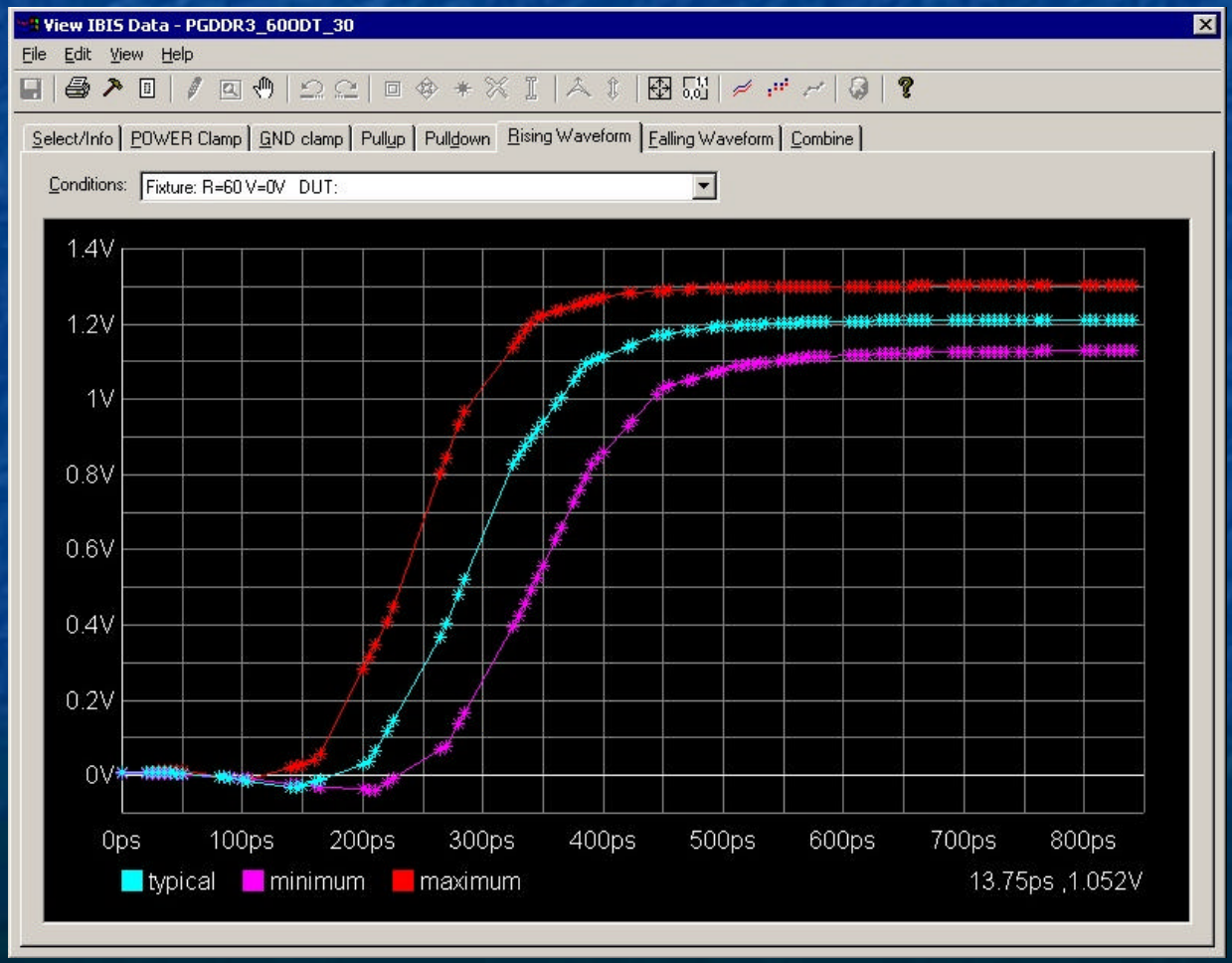
Over Clocked Case – VT After

- VT curve time Shifted
  - Reduce delta between Fast and Slow Process corners (~ 450ps)



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Over Clocked Case – Simulation After

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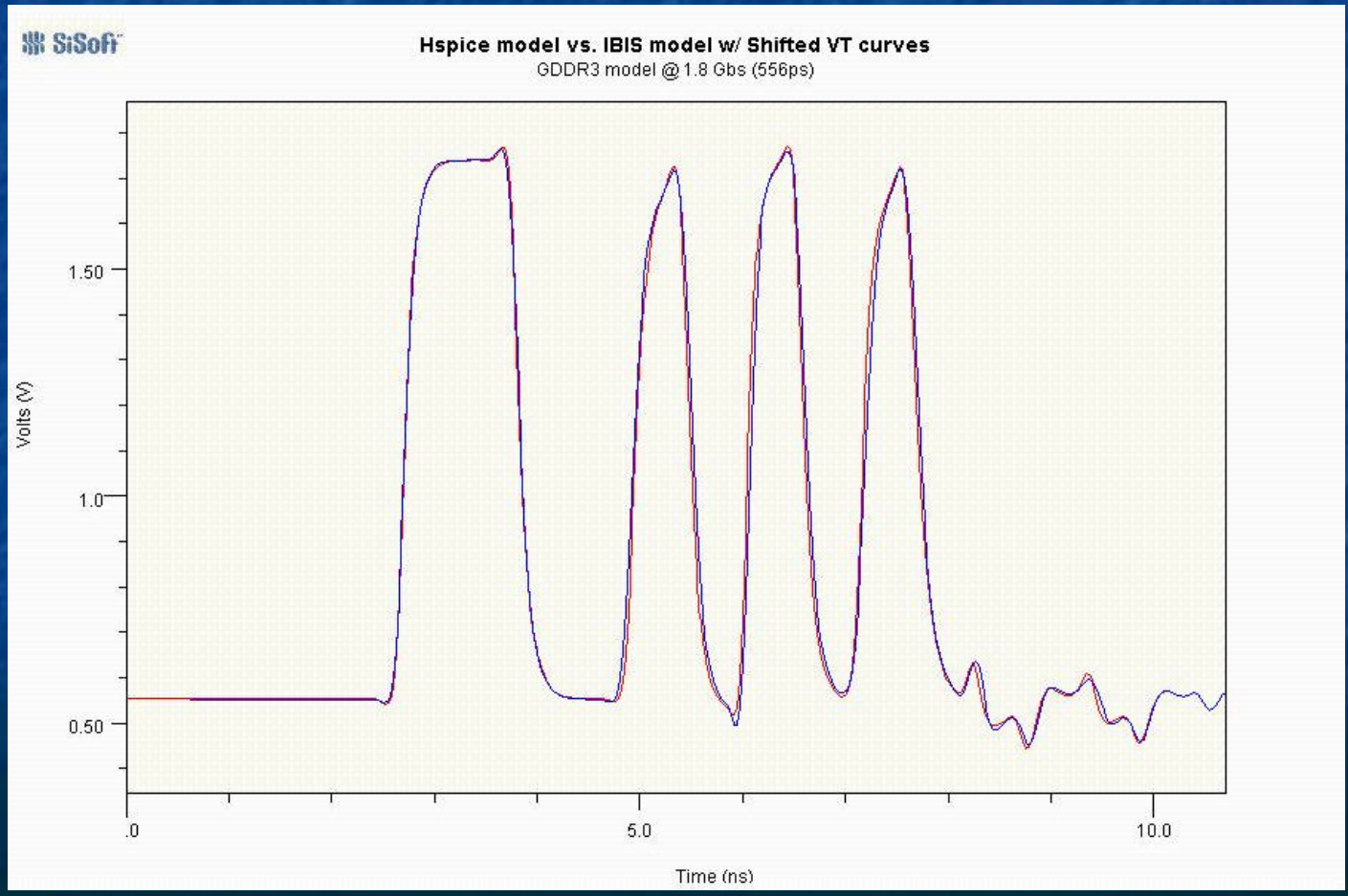

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SiSoft Implementation

- Implemented parameter (in .ibs file)
- SiSoft uses “|Sisoft” parameters to augment IBIS capabilities
- “|” character is a comment character for IBIS
  - Industry tools will ignore
  - |SiSoft is Keyword in SiAuditor / Quantum SI
- SiSoft parameter used
  - SPICE2IBIS processing
  - |SiSoft VT_offset typ, min, max
- Lost FF to SS timing relationship
  - Comment in .ibs file to document

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