

Modeling the Radiated Emission of Micro-controllers

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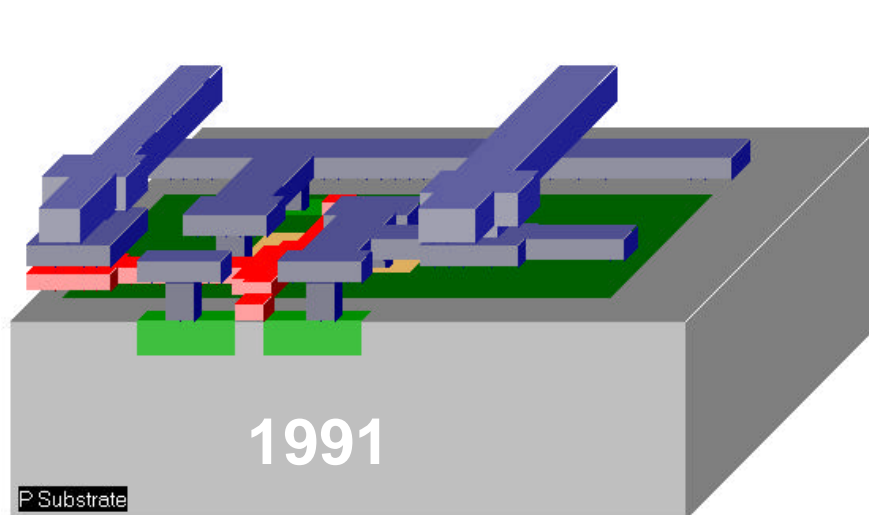
Etienne SICARD



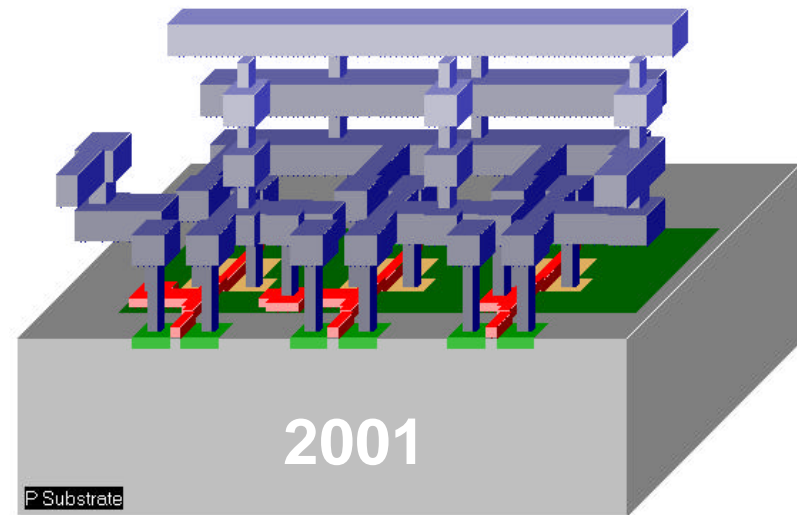
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2. System design methodology for EMC
3. The IERSET project on EMC for ICs
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6. Emission model in TEM cell
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1. Context of the study



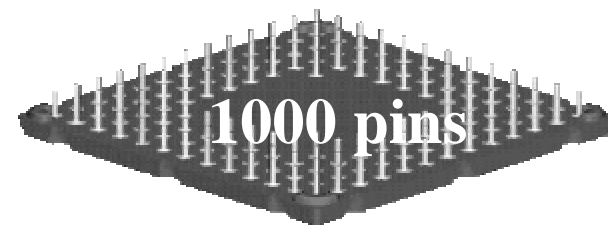
- ☺ 0.7 μ m, 2 metal layers
- ☺ Up to 100,000 devices on a chip
- ☺ CPU frequency 50MHz



- ☺ 0.12 μ m, 6 metal
- ☺ Up to 200,000,000 devices
- ☺ CPU frequency 1GHz

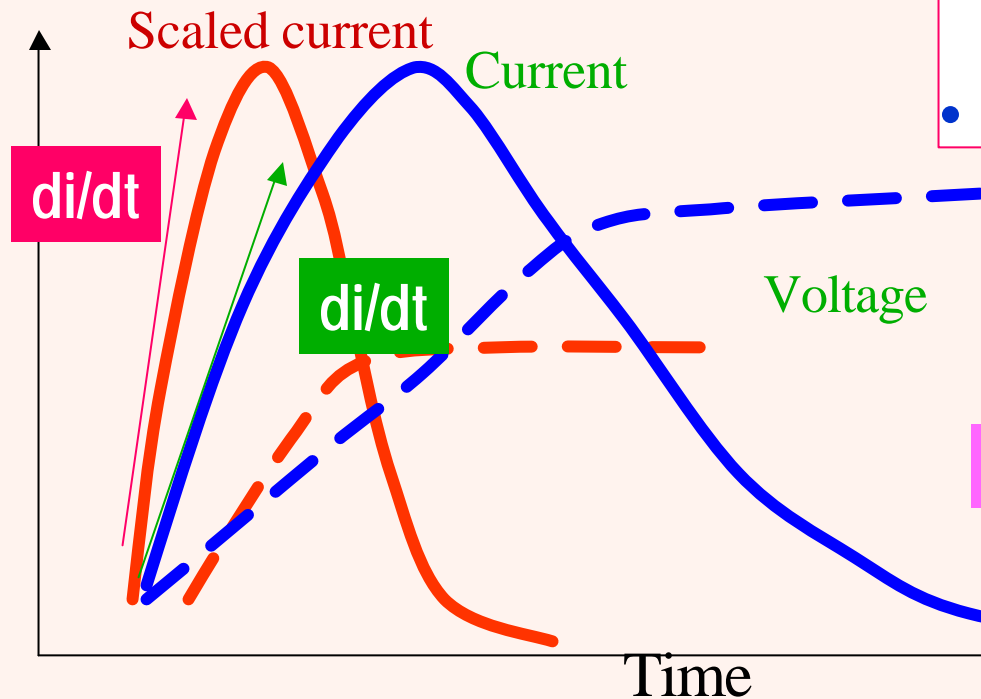


10 years of
evolution



1. Context of the study

Voltage & Current



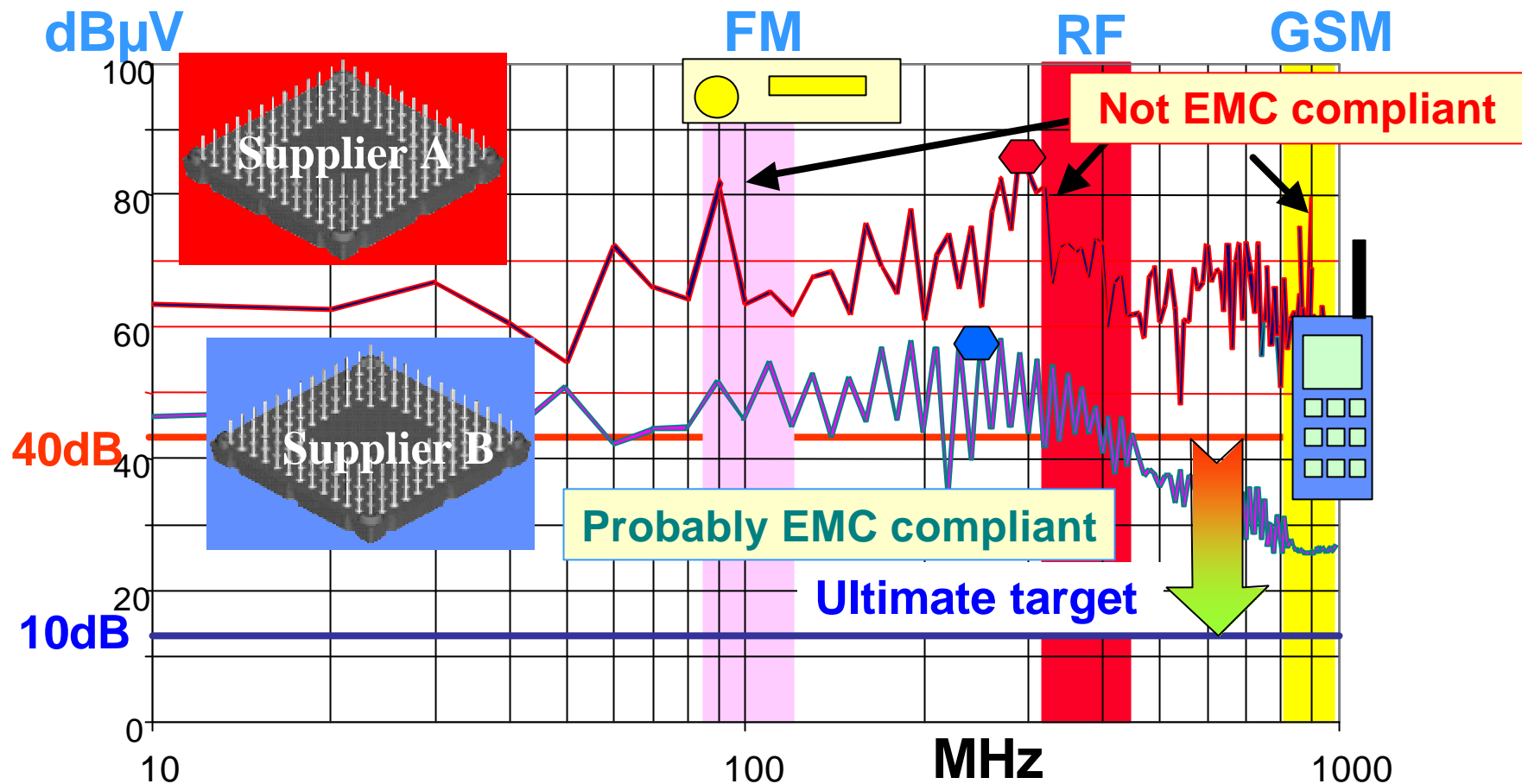
- Voltage supply decreases
- Current amplitude keeps constant
- Faster switching

Stronger di/dt

Increased EMC problems

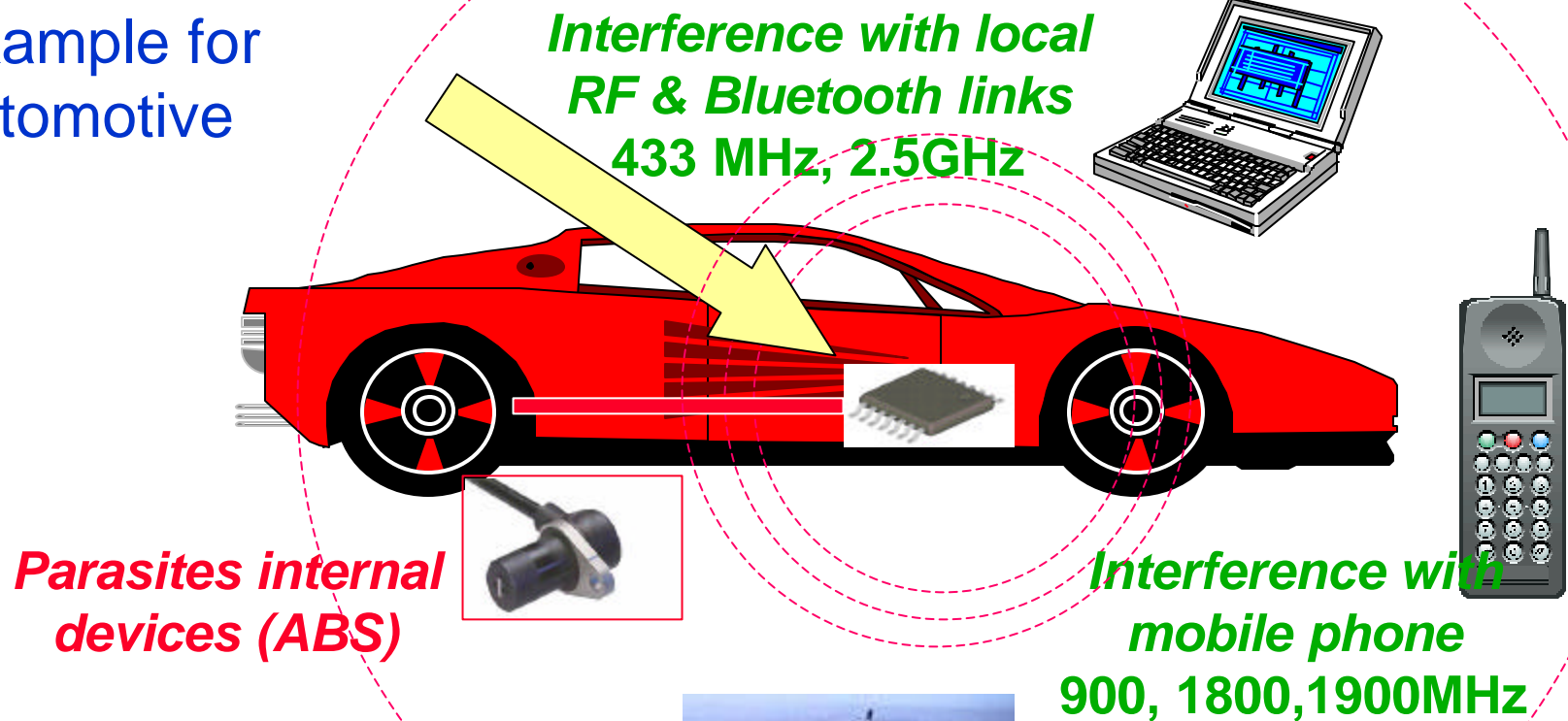
1. Context of the study

Low parasitic emission is a key argument



1. Context of the study

Example for
automotive

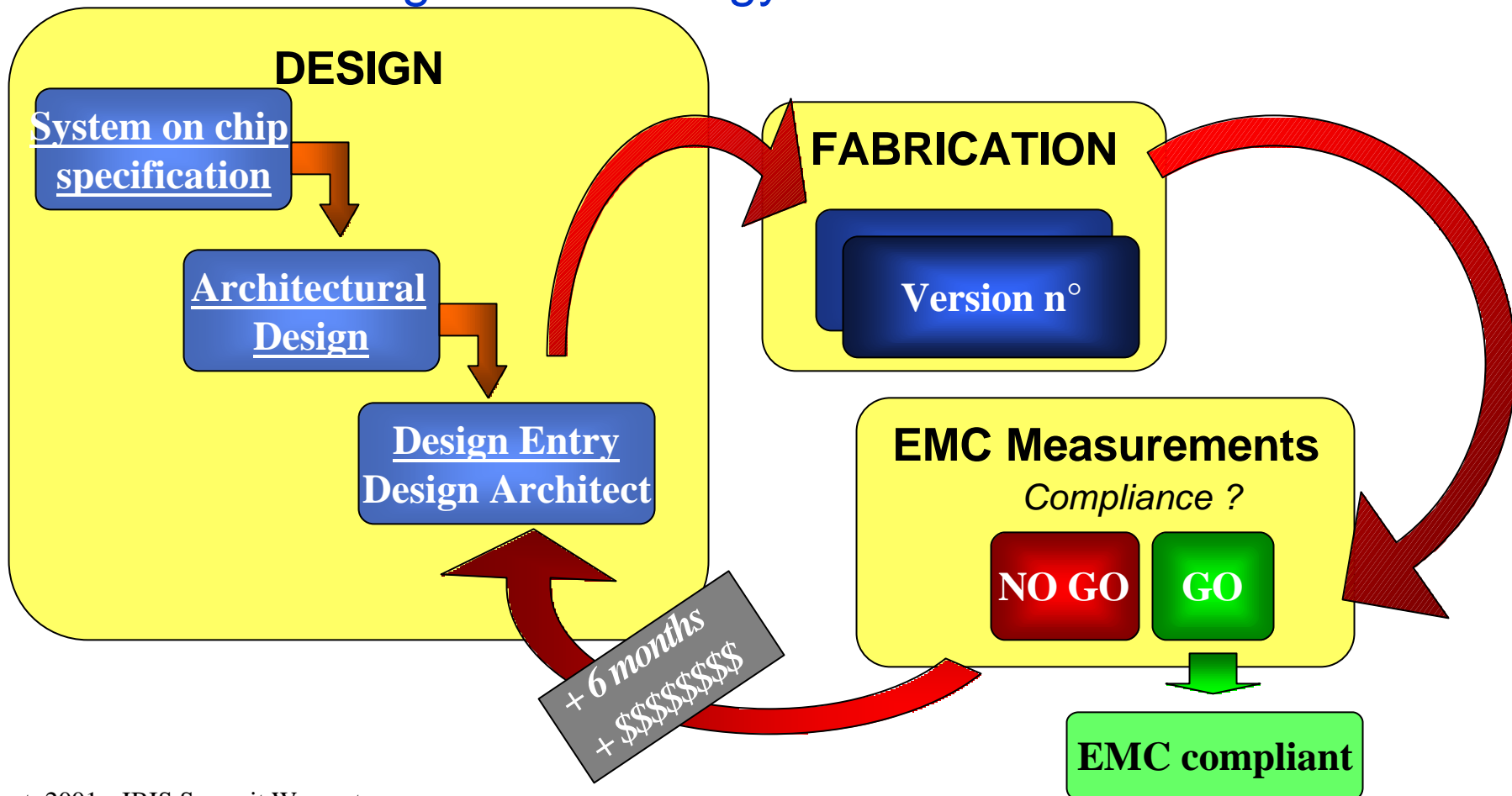


Similar EMC problems
in aerospace



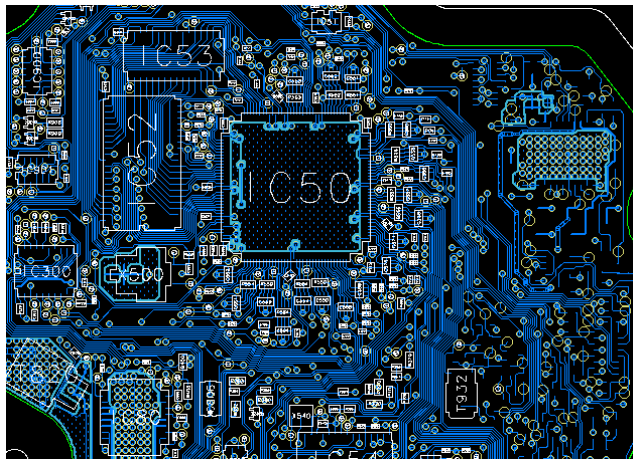
2. System Design Methodology for EMC

Obsolete Design Methodology

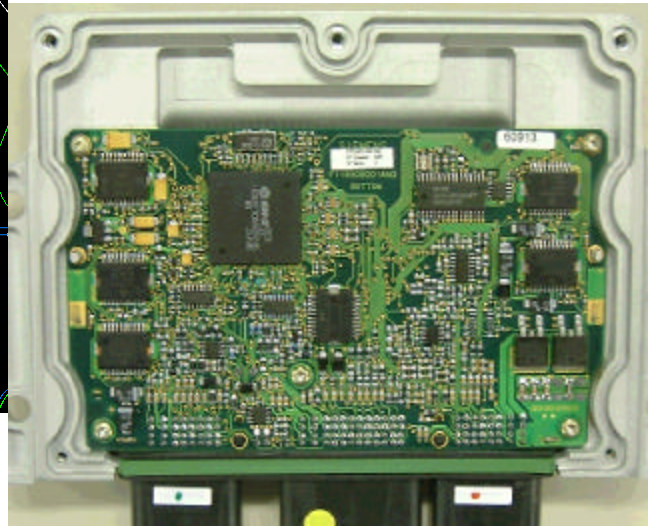


2. System Design Methodology for EMC

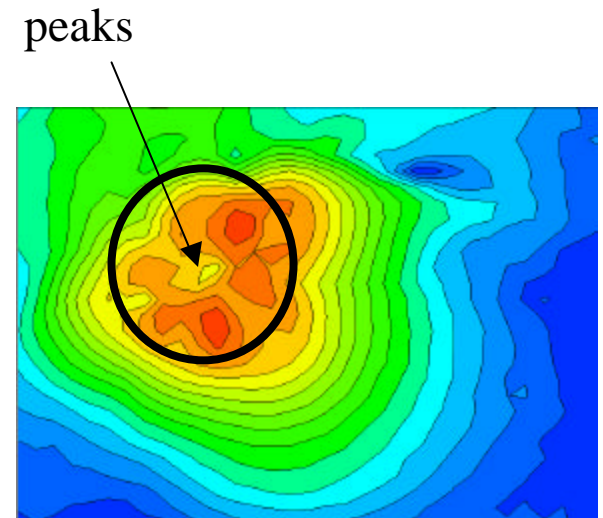
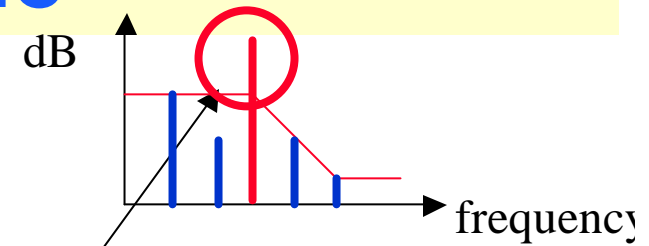
Obsolete Design Methodology



PCB design



Prototype board

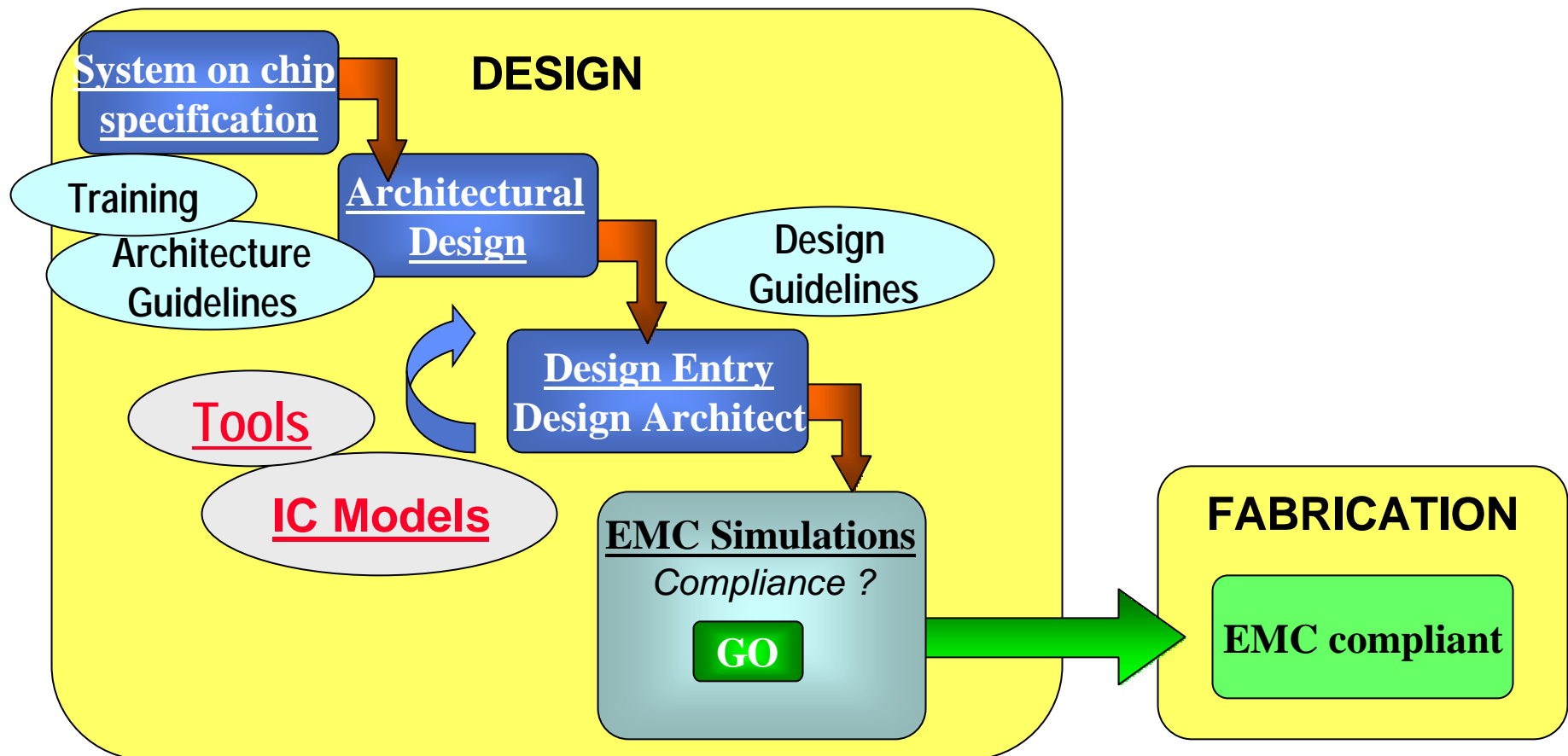


EMC scan

Electromagnetic incompatibility found too late

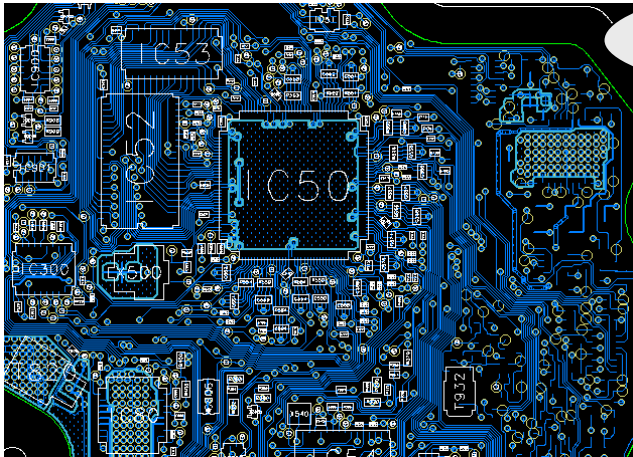
2. System Design Methodology for EMC

Target Design Methodology



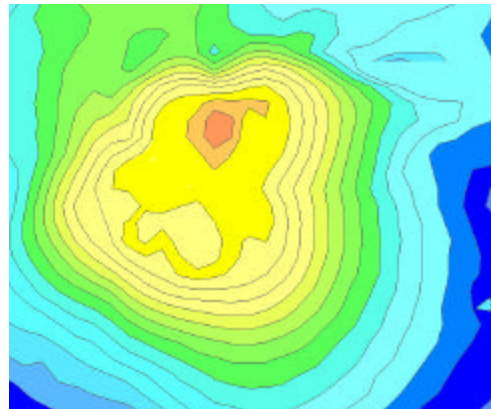
2. System Design Methodology for EMC

Target Design Methodology



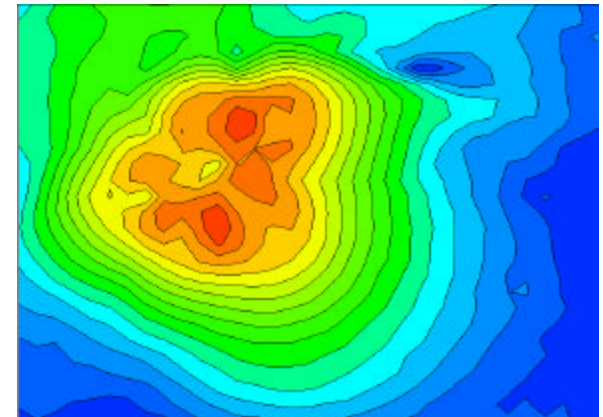
PCB design

With IBIS



Wrong prediction of the
radiated emission

With IBIS and
core model

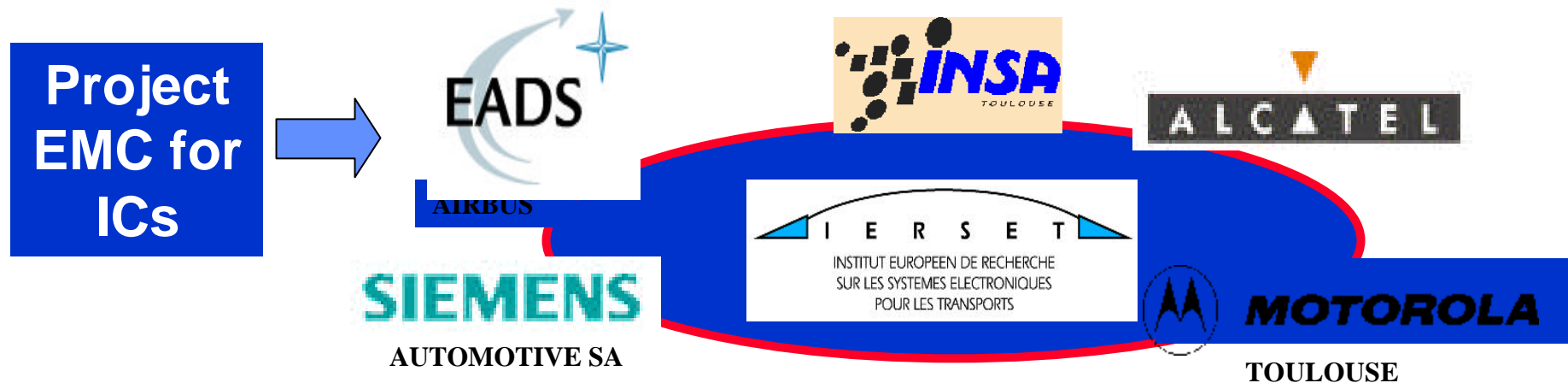


Good forecast of radiated
emission

A core model is mandatory for accurate emission prediction

2. The IERSET project

European Research Centre on Electronics for Transportation
identifies and co-ordinate co-operative research.

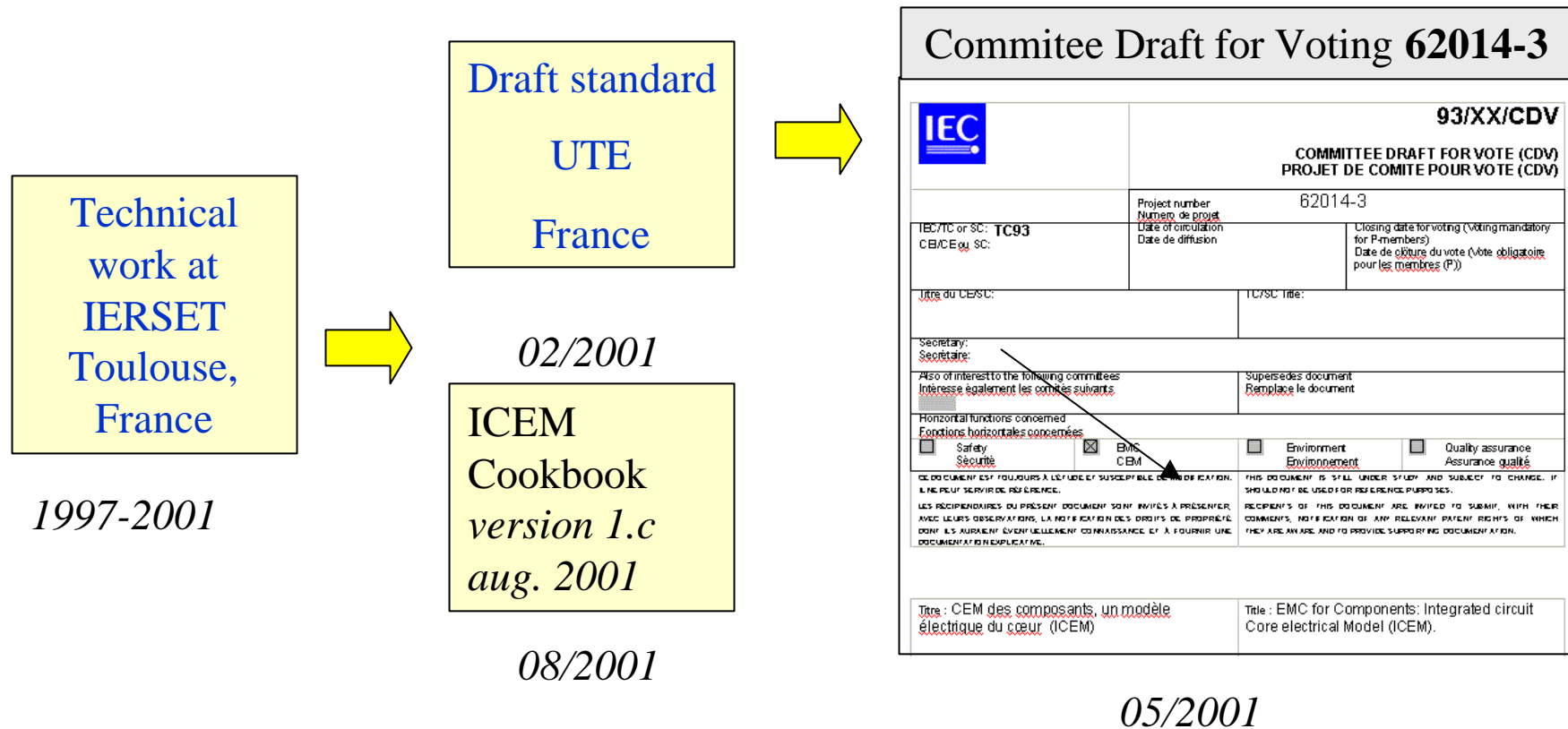


Objectives

- Definition and validation of a model to be used in PCB CAD tools to guarantee the EMC of electronic systems
- One model from 1MHz to 1GHz, for conducted *and* radiated emission

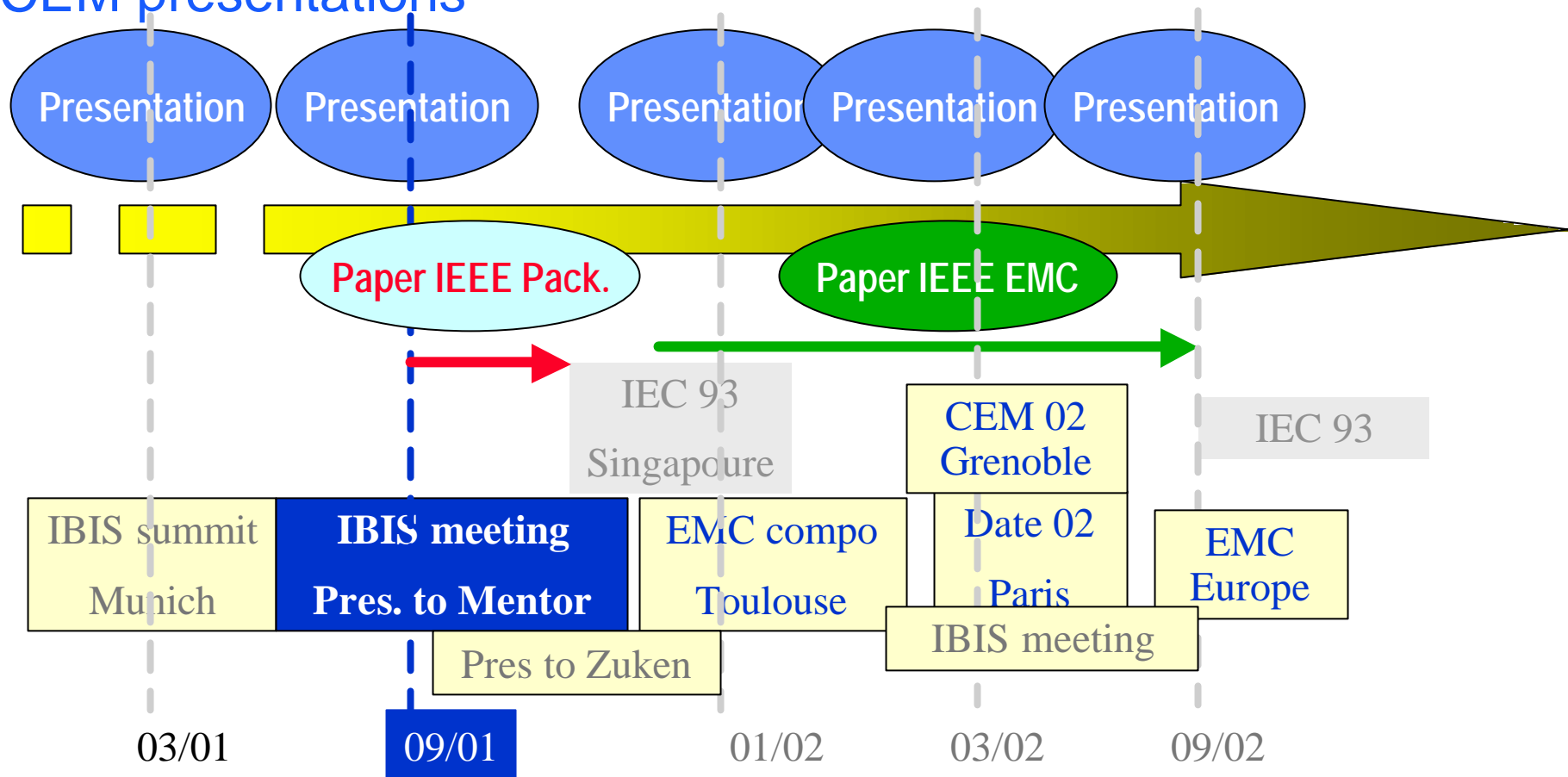
2. The IERSET project

ICEM (*Integrated Circuit Electromagnetic compatibility Model*)



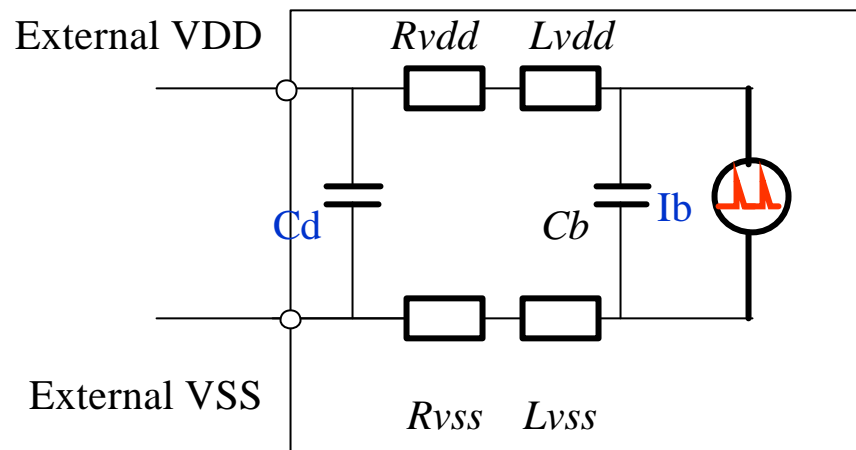
2. The IERSET project

ICEM presentations

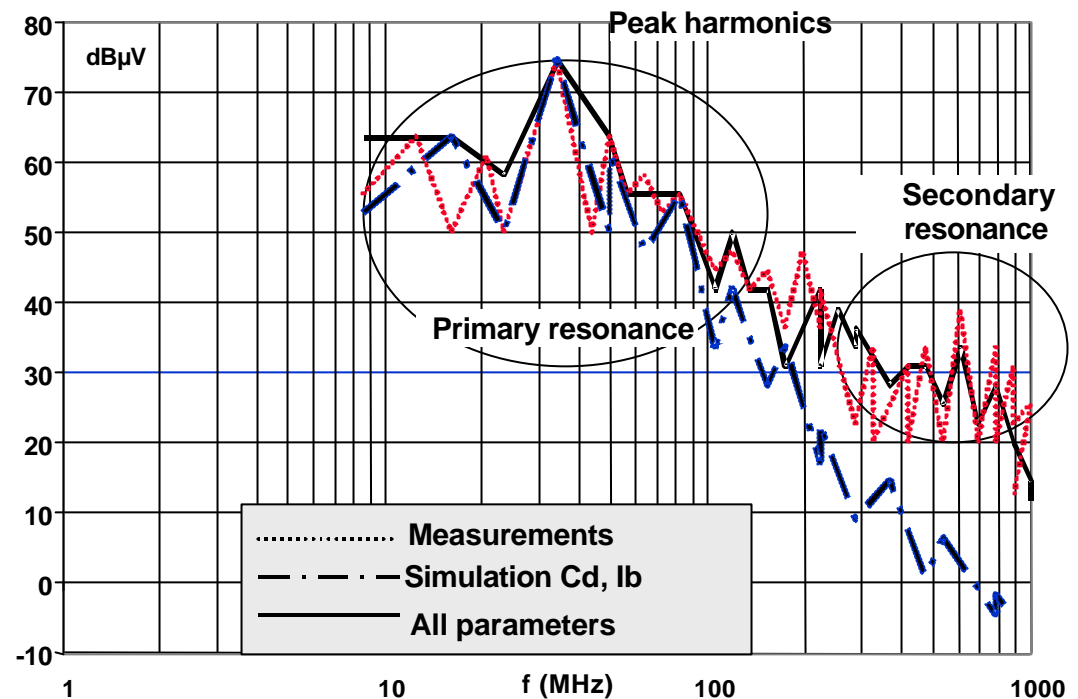


4. Core Emission Model

ICEM includes a simple core model, not handled by IBIS



Basic parameters	Cd, Ib
Advanced param.	R,L,Cb



4. Core Emission Model

Current generator estimation

Physical Transistor
level (*Spice*)



Huge simulation
*Limited to analog
blocks*

Interpolated
Transistor level
(*Powermill*)

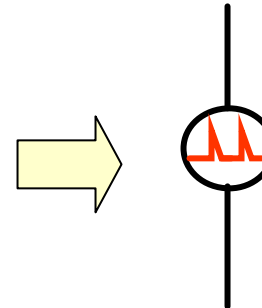
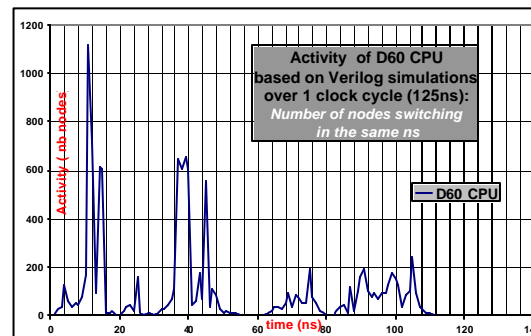


*Difficult adaptation to
usual tools*
Limited to 1 M devices

Gate level
Activity



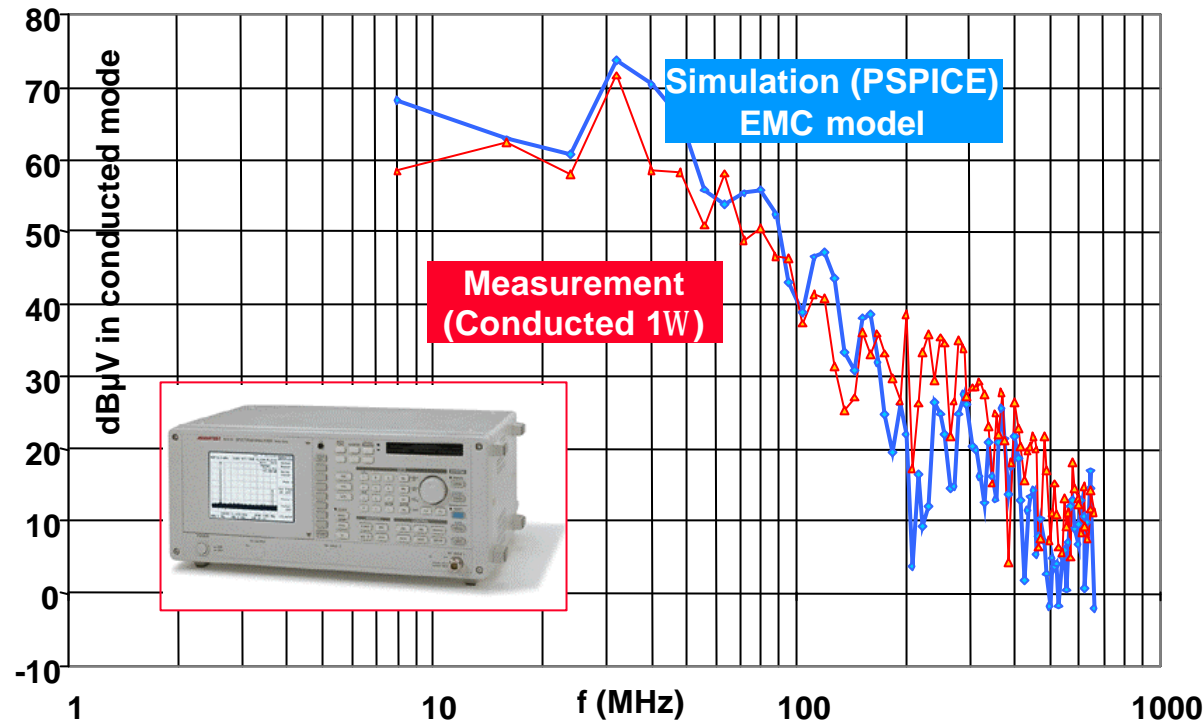
Simple, not limited
Fast
Not very accurate



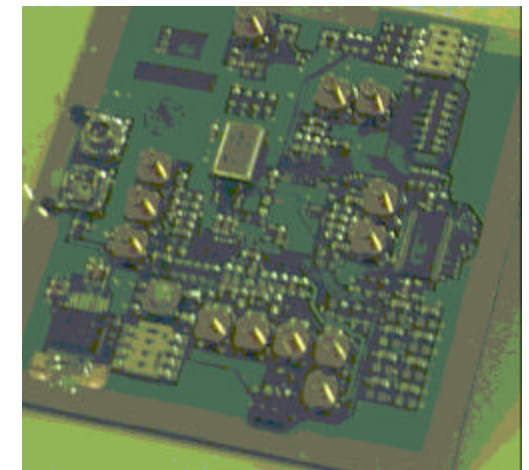
Equivalent
Current
generator I_b

5. Emission Model with IOs

Validation for a 16 bit micro-controller



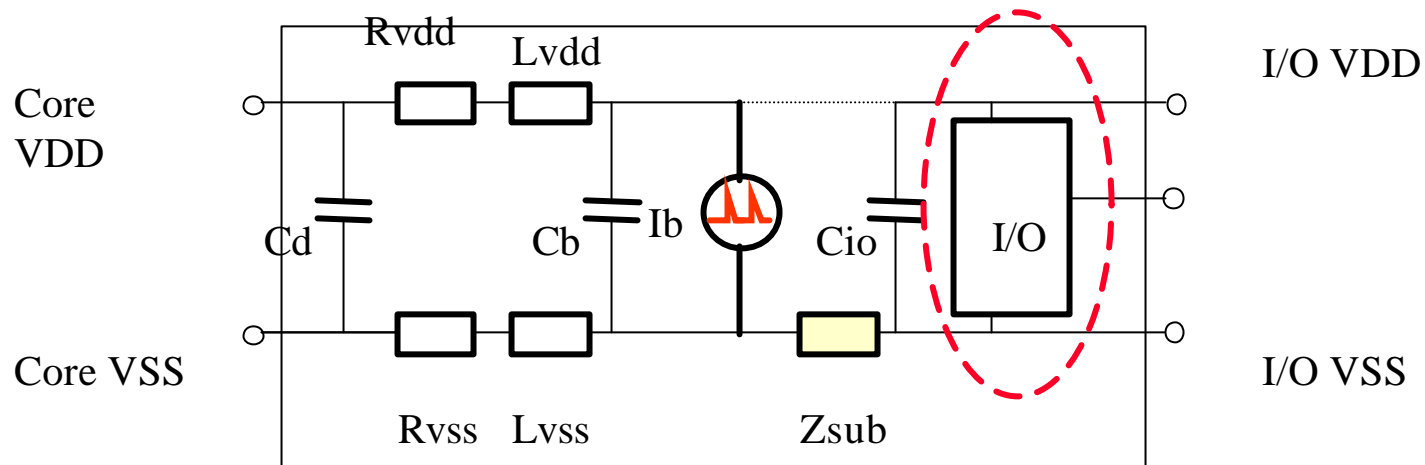
Within 10dB, but I/Os not handled



Comparison between
simulation and
measurement on a 16 bit
micro-controller

5. Emission Model with IOs

Add IBIS I/O data



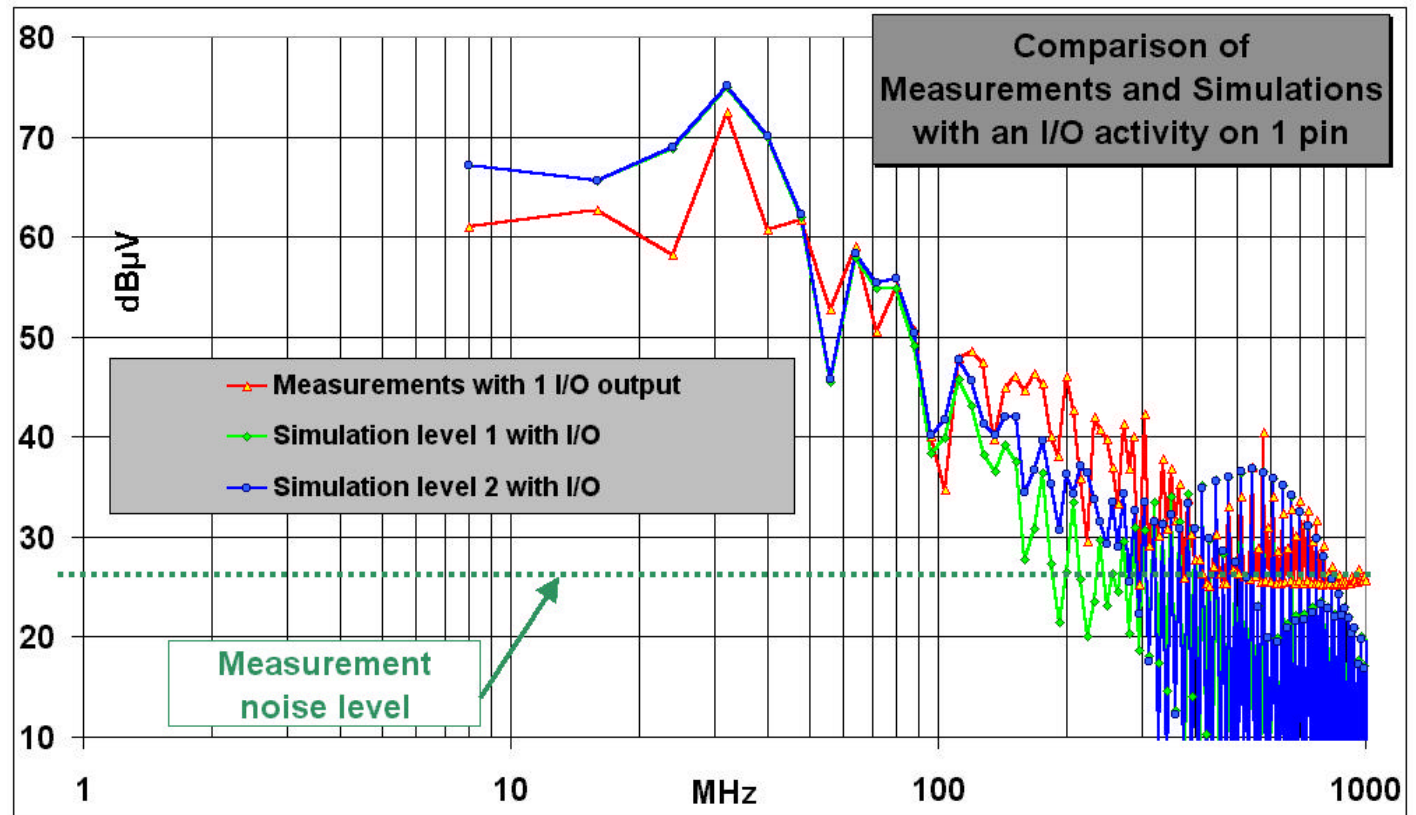
Z_{sub} : basically a 1-10 Ω serial resistance

C_{io} : decoupling capacitance for IO supply

IO block: reuse of IBIS

5. Emission Model with IOs

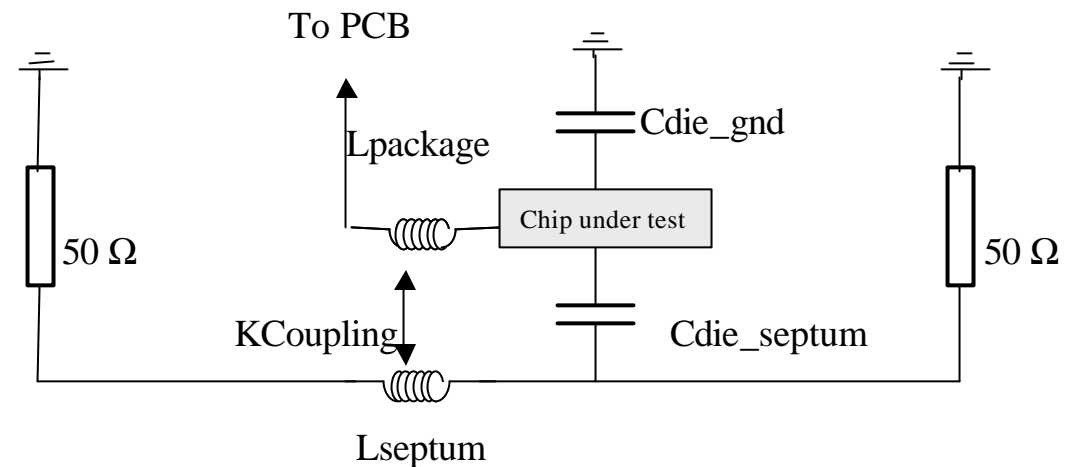
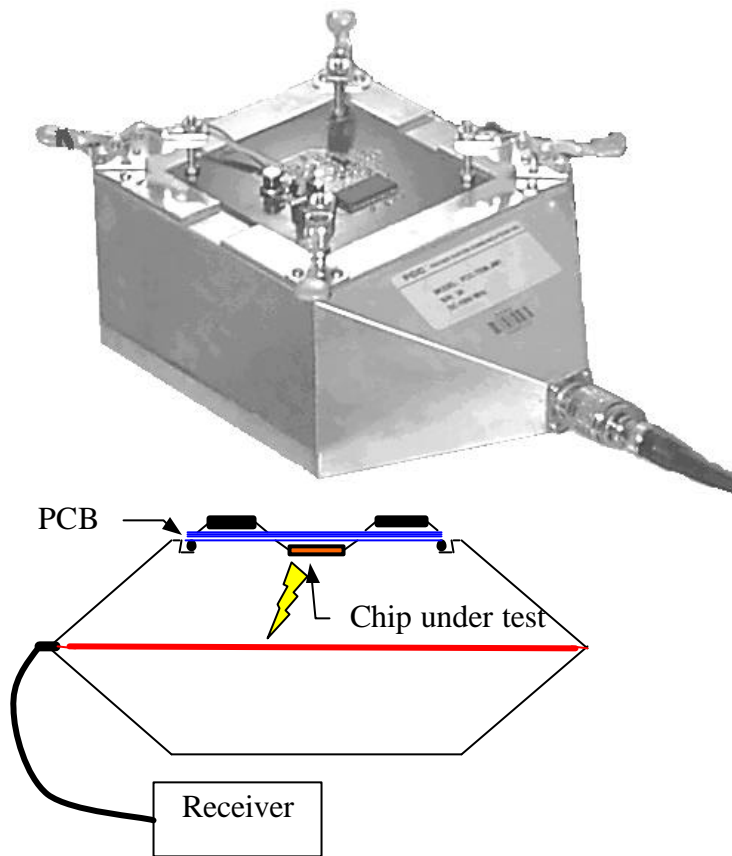
Validation



IO modify the spectrum at high frequencies (>300MHz)

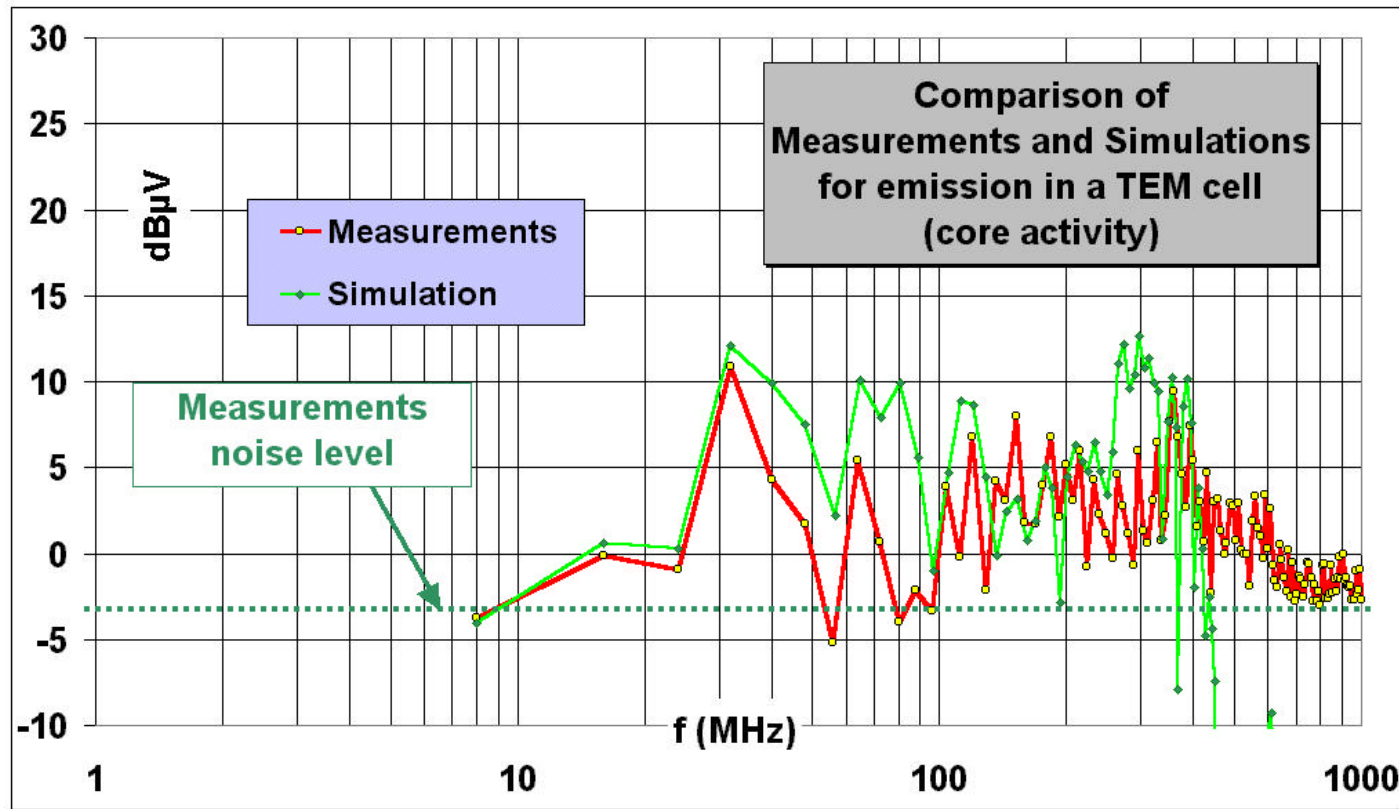
6. Emission in TEM cell

Proposed model: capacitance & inductance coupling



6. Emission in TEM cell

Validation for the core alone

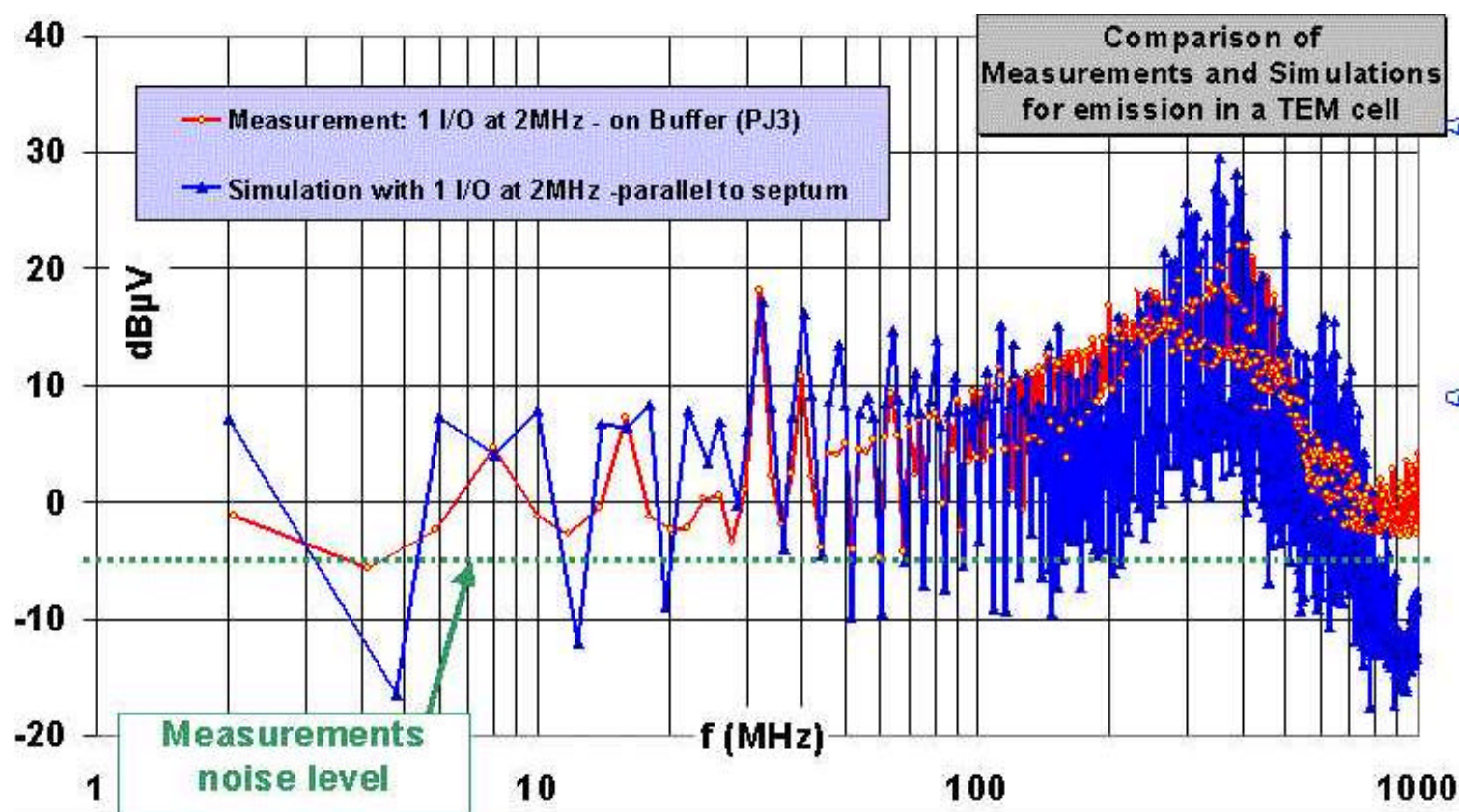


Model fits correctly up to 400MHz

At high frequencies, close from noise floor

6. Emission in TEM cell

Validation for the core & IOs



Model fits correctly up to 800MHz

At high frequencies, IO effects dominate

Conclusion

- ◆ Technology scale down illustrated
- ◆ More complex chips increase parasitic emission
- ◆ An EMC model for Ics is mandatory
- ◆ A simple model has been proposed
- ◆ Satisfactory prediction of conducted emission
- ◆ Prediction of the core emission in TEM investigated
- ◆ Model proposal standardized by UTE (ICEM)
- ◆ Presentation and promotion to CAD & IC providers