Modeling and Simulation of High Speed Serial Link Systems

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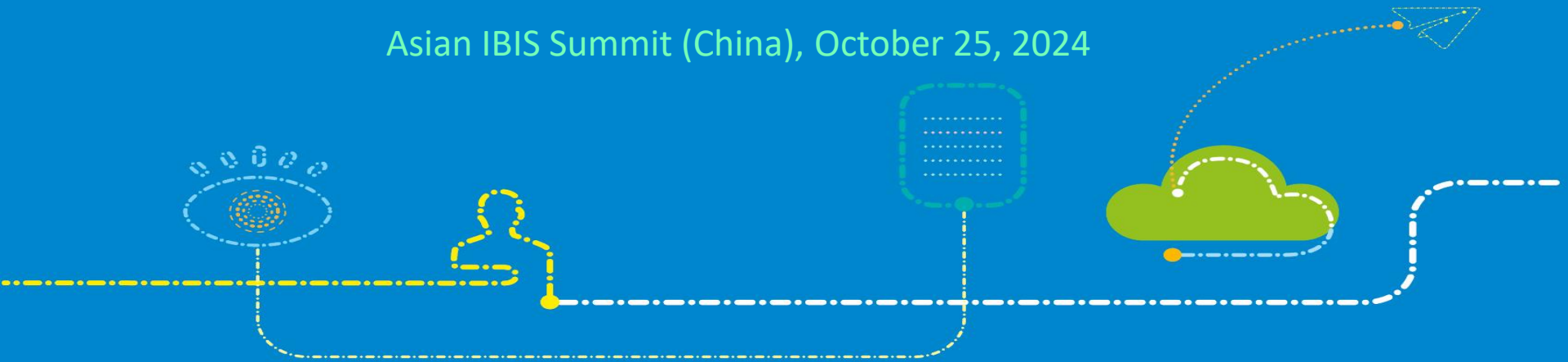

Outline

- Problem Statement
- Quick Recap on ADC-Based SerDes
- Tips for Faster Simulations
- Model Correction Based on Realistic Channels
- Conclusion

Problem Statement

Problems occur during the channel evaluation when the electrical interfaces rate reach 112Gbps：

- It is difficult to filter out failed channels, based on passive channel specifications like ICN, FOM_ILD and ERL.
- Channel Operating Margin, a channel compliance evaluation method.
  - ▪Based on certain prerequisites, there may be some difference from actual situation.
- Models from IP vendors.
  - ▪In some instances, simulation may prove to be time-consuming.
  - ▪Simulation results supposed to be calibrated according to test results and test environment.

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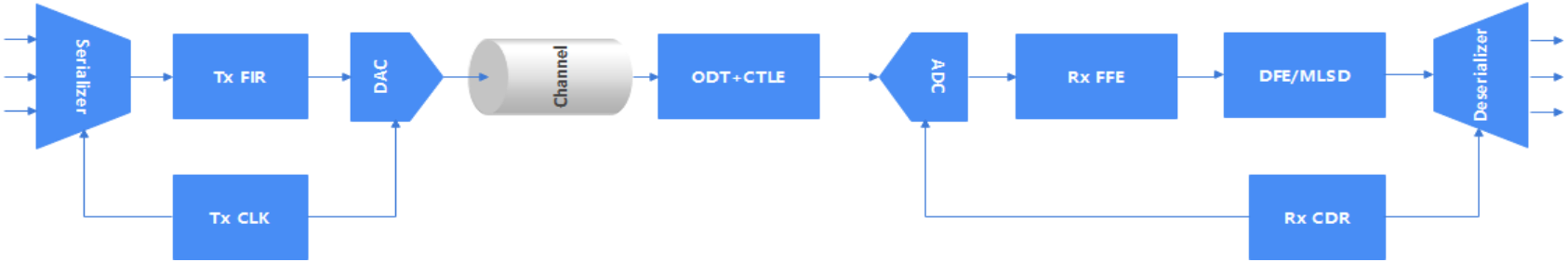
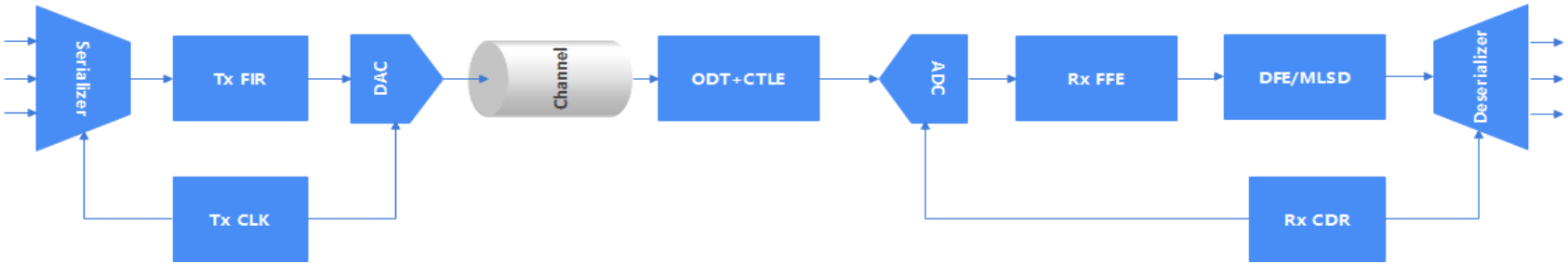
Quick Recap on ADC-Based SerDes



- Modulation, Mapping, Tx swing.
- Control transmitter equalization through normalized FIR coefficients.
- CTLE is modeled by three poles, two zeros and DC gain that equalizes for channel losses.
- The receiver includes a digital equalizer which filters the ADC samples and compensates for channel losses.

Quick Recap on ADC-Based SerDes



- Hard-decision/Soft-decision.
- DFE is a non-linear feedback equalizer, ISI is directly subtracted from the incoming signal.
- Maximum Likelihood Sequence Estimator.

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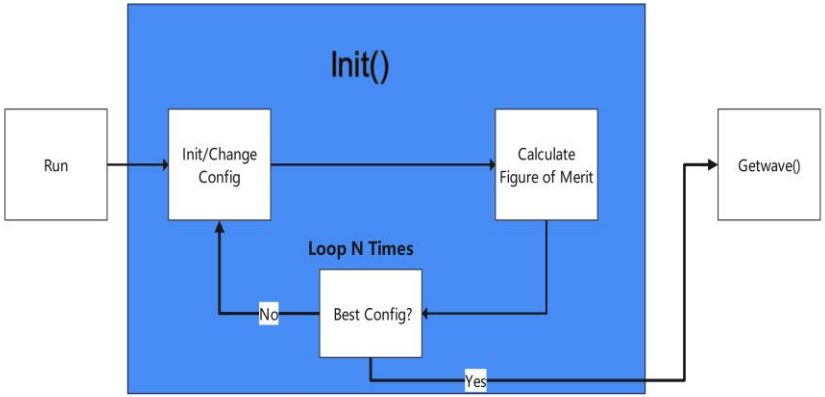
Why is Time-Consuming: Equalizer Configuration



Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.54	—
Transmitter equalizer, 3rd pre-cursor coefficient Minimum value Maximum value Step size	$c(-3)$	 –0.06 0 0.02	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.12 0.02	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.34 0 0.02	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.2 0 0.02	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB

- Full scan in typical automatic link training scenarios, for example, N=4*7*18*11*21*7>800,000 times. Simulation may take several hours at a time.

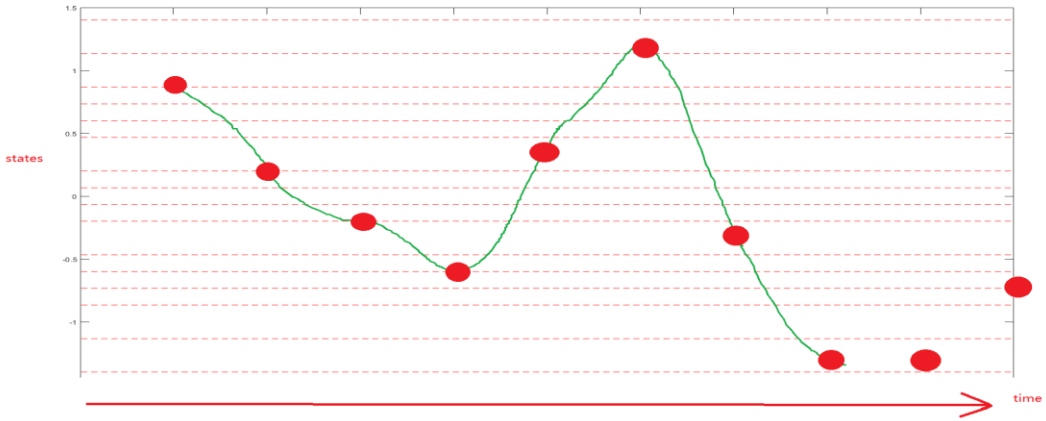
Proposed Method

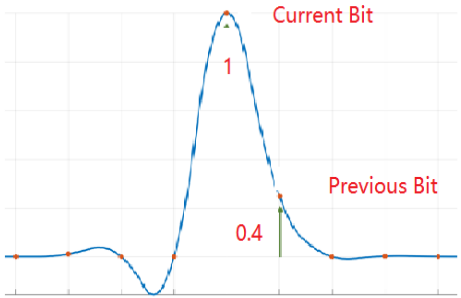
▪Preset Tx FIR and CTLE config according to channel loss.
For example:

Channel Loss	Tx Taps Presets
20dB	[0 0.02 -0.16 0.82 0]
25dB	[0 0.02 -0.18 0.8 0]
30dB	[0 0.04 -0.2 0.74 -0.02]
35dB	[0 0.04 -0.22 0.72 -0.02]
40dB	[0 0.06 -0.24 0.68 -0.02]

▪Instead of a full scan, a small-scale scan is performed based on presets.
▪Simulation takes several minutes at a time.

Maximum Likelihood Sequence Estimator





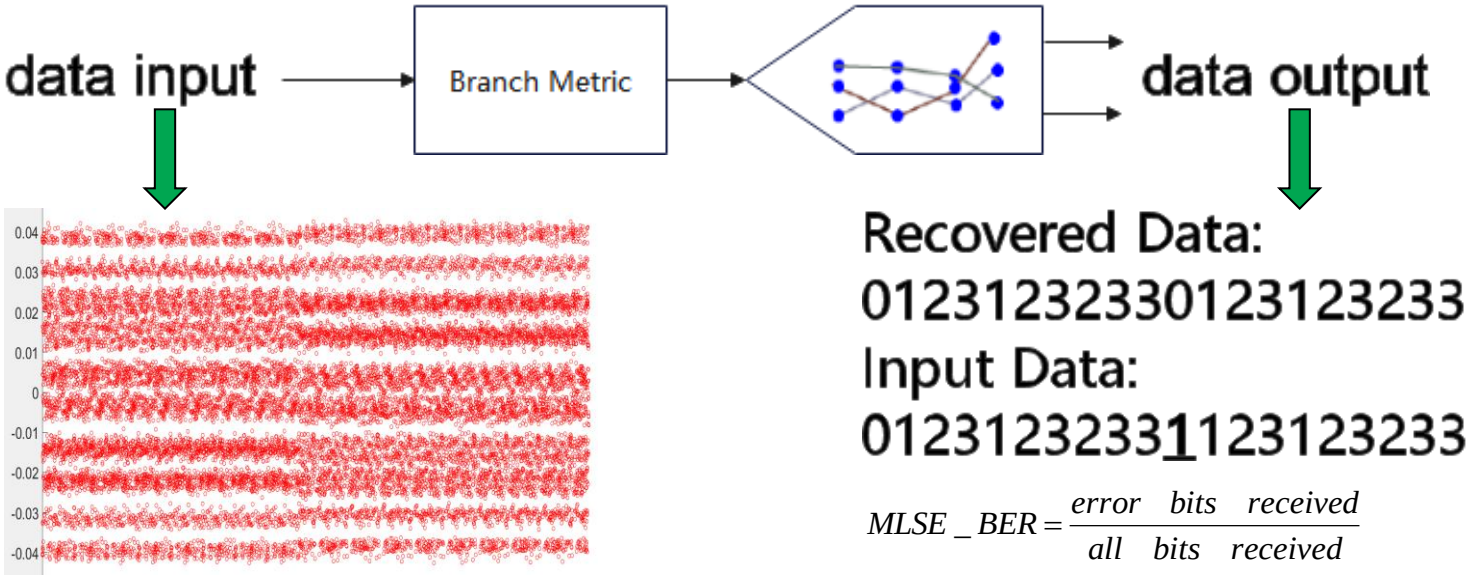
Full State MLSD, Number of States: 16.

- Accumulate the "likelihood" over a "sequence" and then pick the most likely sequence.

$$Find(\hat{x})\ to \quad \min imize \sum_k e_k^2 = \sum_k [r_k - (\hat{x}_k + h_1 \hat{x}_{k-1})]^2$$

- Number of States S=N^M
- N= PAM levels, N=4 for PAM4
- M=Number of taps

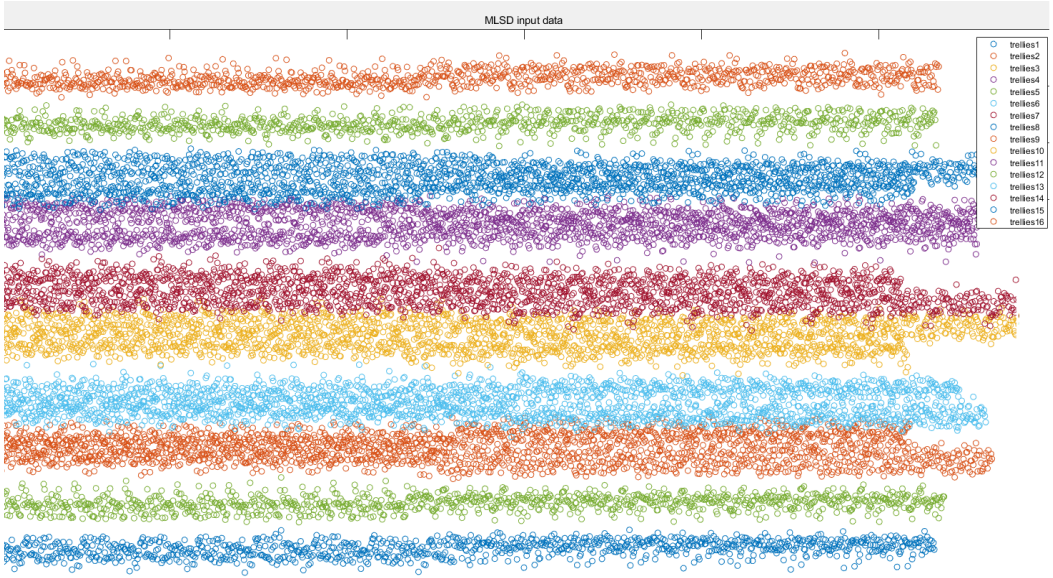
Typical Way for MLSE Decoder



$$MLSE\_BER = \frac{error\ \ bits\ \ received}{all\ \ bits\ \ received}$$

- To achieve a reasonable bit error ratio, the input sequence should be long enough.
- It may take tens of minutes.

Proposed Method for MLSE Decoder



$$\mu^2 = \frac{1}{N}\sum_{i=1}^{N}\left(\frac{1}{M}\sum_{i=1}^{M}\left|inputdata[i]\right|\right)^2$$

$$\sigma^2 = \frac{1}{N}\sum_{j=1}^{N}\left(\frac{1}{M}\sum_{i=1}^{M}\left|inputdata[i]-\mu\right|\right)^2$$

$$SNR = 10\times\log_{10}(\mu^2/(\sigma^2+n^2))$$

n^2 stands for noise energy.

$$trellisN = inputdata(current\_state = i, previous\_state = j), i,j \in (1,4)$$

- Different from the bit-by-bit simulation, this method can be used to obtain SNR in a relatively short sequence.

How Many Bits Need to Run

run bits	SNR	BER
1e5	21.0226	2.15e-7
4e5	21.0677	1.99e-7
1e6	21.0198	2.17e-7
1e7	21.0542	1.96e-7

- Based on the data comparison in the above table, the precision of the 1e5 bit is similar to that of the 1e7 bit.
- It may take less than one second.

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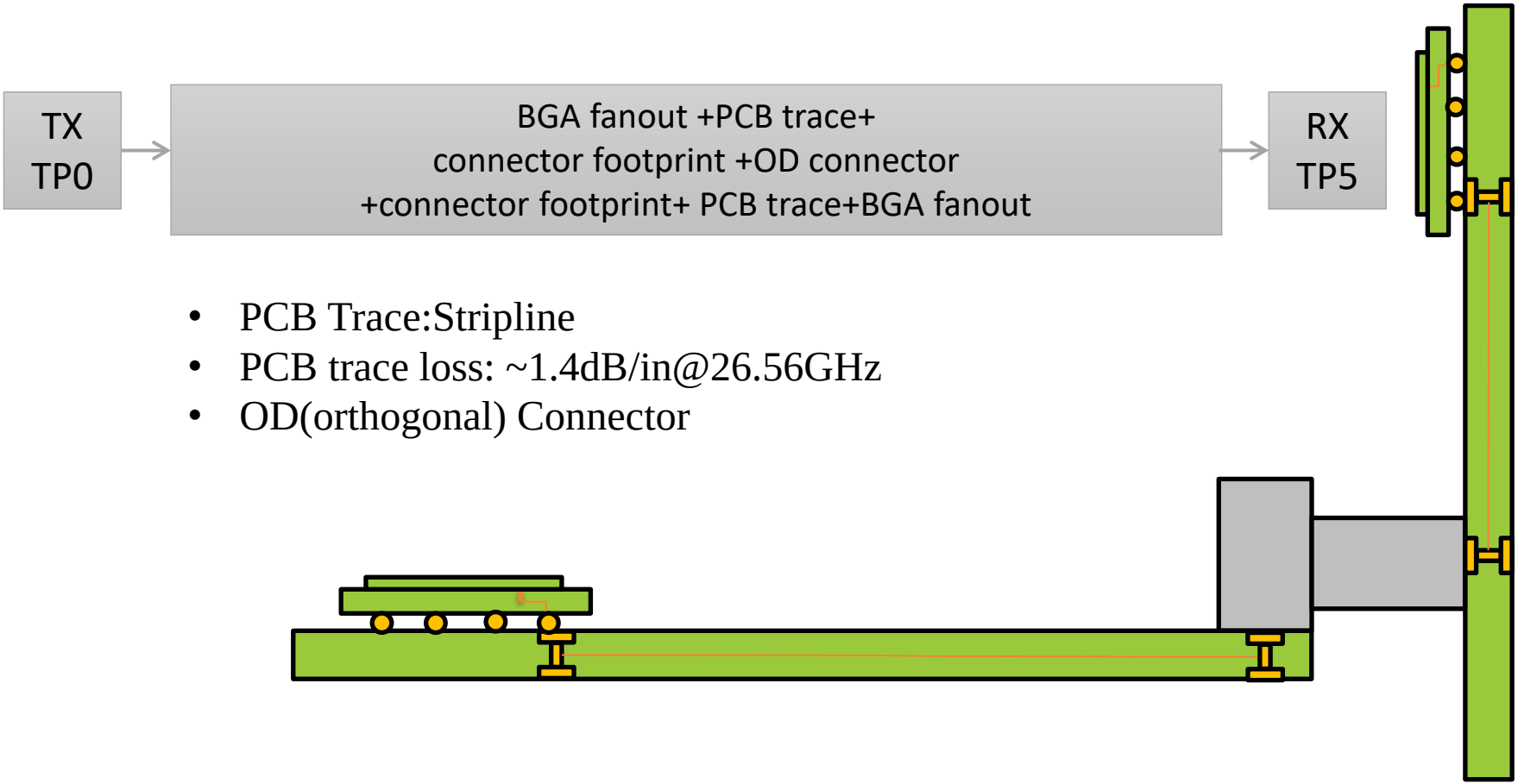
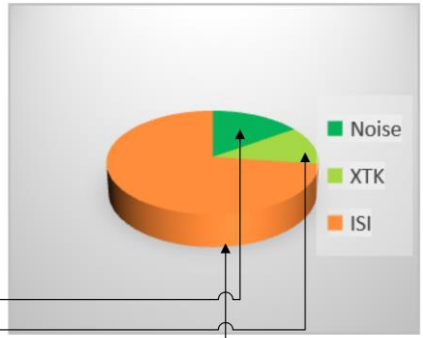
Channel Characteristics



- PCB Trace:Stripline
- PCB trace loss: ~1.4dB/in@26.56GHz
- OD(orthogonal) Connector

Model Correction

$$SNR = 10\log_{10}\left(\frac{A_s^2}{\sigma_{ISI}^2 + \sigma_{XT}^2 + \sigma_N^2}\right)$$

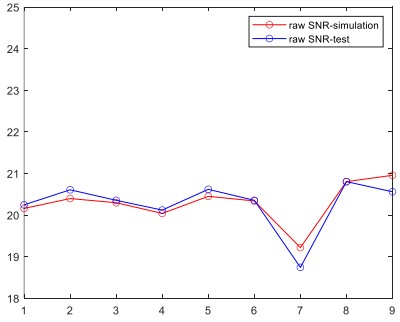


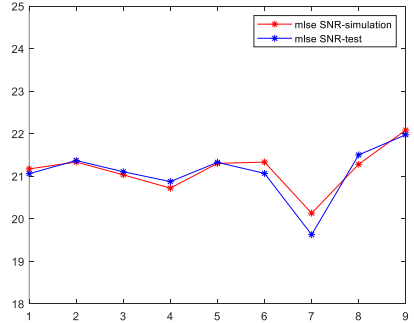
- There are four main factors that affect SNR of the model: signal energy, ISI, crosstalk, noise.
- Change the bump-to-bump interconnect loss, and modify equalizer configuration, especially the zeros and poles of CTLE.
- Change the crosstalk amplitude, and adjust noise configuration accordingly.

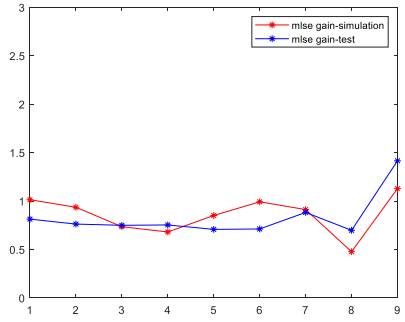
Simulation and Measured Results

	ICN/ mV	IL/dB	ILD/dB	Channel descriptions	Raw BER	MLSE BER	Raw BER	MLSE BER
channel1	0	40.24	0.286	PCB Trace 13.5inch	2.1e-6	1.4e-7	1.8e-6	1.9e-7
channel2	0.17	39.36	0.27	PCB Trace 13inch	1.2e-6	8.5e-8	6.8e-7	7.6e-8
channel3	0.33	39.36	0.27	PCB Trace 13inch	1.5e-6	2.1e-7	1.3e-6	1.7e-7
channel4	0.42	39.36	0.27	PCB Trace 13inch	2.8e-6	5.0e-7	2.3e-6	3.3e-7
channel5	0.42	38.63	0.262	PCB Trace 12.5inch	1.0e-6	9.4e-8	6.6e-7	8.7e-8
channel6	0.53	38.33	0.26	PCB Trace 12inch	1.4e-6	8.6e-8	1.3e-6	1.9e-7
channel7	0.42	41.1	0.279	PCB Trace 14inch	1.6e-5	2.3e-6	3.8e-5	7.0e-6
channel8	0.33	38.33	0.26	PCB Trace 12inch	4e-7	1e-7	4.0e-7	5.0e-8
channel9	0.42	36.76	0.248	PCB Trace 11inch	2.6e-7	6.7e-9	7.7e-8	1.0e-8

- simulation data
- measured data







- Based on the proposed method, we are able to get MLSE performance gain over DFE and predict BER while maintaining a reasonable simulation time.

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Conclusion

- The challenges arise when designing a system channel and evaluating its end-to-end performance, as we described in “Problem Statement” part. This method is performed on LR channels of an orthogonal system in a real-world application, the results indicate that it has quite good performance both in terms of simulation time and precision.

- Two tips for faster simulation.
  - Preset Tx FIR and CTLE config according to channel loss.
  - Proposed a more efficient way to perform MLSE.

- Using the aforementioned method, we are capable of capturing the enhancement in MLSE performance over DFE and predicting BER, all while preserving a reasonable simulation duration.

Thank You!

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