Priorities and Alternatives for Touchstone 3.0 Port Mapping – *Updated*

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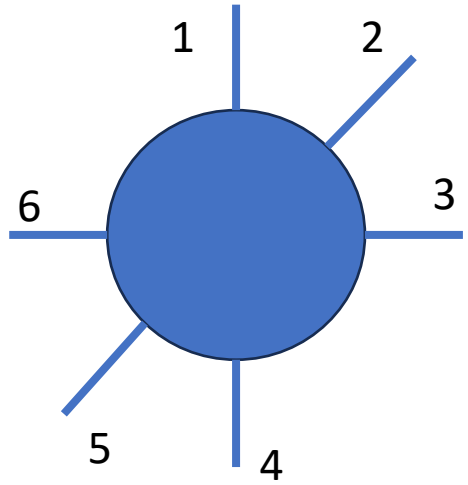
The Problem

- In current Touchstone and Touchstone 2.0, what can I say about the component shown?
  - Interconnect or device?
  - If interconnect, relationship between ports?
  - Can I make inferences from the data?
- Need to know interconnect port arrangement to focus properly on losses vs. crosstalk
  - Is S21 insertion loss? Or is S21 crosstalk?




```
# MHz Y RI R 50
5.00 8.0 9.0 2.0 -1.0 3.0 -2.0 1.0 3.0 1.0 0.1 0.2 -0.2
2.0 -1.0 7.0 7.0 1.8 -2.0 -1.0 -1.0 -0.5 0.5 0.2 -0.1
3.0 -2.0 1.8 -2.0 5.8 6.0 1.2 0.8 0.9 0.7 0.3 -0.5
1.0 3.0 -1.0 -1.0 1.2 0.8 6.3 8.0 2.0 -0.5 1.5 0.6
1.0 0.1 -0.5 0.5 0.9 0.7 2.0 -0.5 4.7 -6.0 -1.0 2.0
0.2 -0.2 0.2 -0.1 0.3 -0.5 1.5 0.6 -1.0 2.0 5.5 -7.0
```

For interconnects, industry wants a structure that establishes expectations for port behavior automatically and in advance of detailed data analysis

A Proposal for Unambiguous Port Mapping

- The IBIS Interconnect Task Group is developing a comprehensive port-mapping proposal for Touchstone 3.0

- The structure so far is LISP-like, similar to that used in .ami
  - (<parameter name> <parameter value>)
  - Not all features proposed or under development are shown in the examples

- Additional features in separate TSIRDs (Touchstone Issue Resolution Documents)

You can find the most recent proposals at
https://ibis.org/interconnect_wip/

Proposed Requirements

REVISED!

(O) = optional

- TSIRD 9: [Begin Port Map]/[End Port Map]
  1. Define unambiguous connections for simulation
     A. Declaration of differential ports, chord ports (not data)
  2. Support generation & verification of:
     A. [Interconnect Model]s in .ibs files
     B. [EMD Model]s in .emd files
     C. [C Comp Model]s in .ibs files
  3. (O) Support automated creation of:
     A. Schematic symbols
     B. Test probe locations
  4. (O) Identify port locations (e.g., xyLayer in PCB) – *encoded in Physical Name x;y;z*
  5. (O) Support user-defined parameters – *(User: <name> <value>)*
  6. (O) Support Swathing through (separately defined) “Schemas”

Does this satisfy industry needs for port *identification* as well as *connectivity*?

Additional Features – Separate TSIRDs

- TSIRD 10: [Start IEEE 370]/[End IEEE 370]
  - A “synonym” of [Begin Information]/[End Information]
  - Allows IEEE 370 data to be included in Touchstone files without syntax checking
  - No passive, causal, or reciprocity calculations
- TSIRD 11: Expected_Passive Yes/No
  - Allows quick identification & separation of active device from interconnect data sets
- TSIRD 12: Swathing Schema definitions

What, if anything, is missing?

Courtesy Walter Katz

Port-Mapping Syntax Examples (1 of 2)

- Transistor Example
  - [Begin Port Map]
  - Port 1 (Logical Emitter)
  - Port 2 (Logical Base)
  - Port 3 (Logical Collector)
  - Symbol_left 1
  - Symbol_right 3
  - Symbol_bottom 2
  - [End Port Map]

- IBIS Package Model Between Pad and Pin 7
  - [Begin Port Map]
  - Port 1 (Physical pin.7) (Side Pin) (Net 7) (Logical DQ3pin)
  - Port 2 (Physical pad.7) (Side Pad) (Net 7) (Logical DQ3pad)
  - [End Port Map]

- "Physical" identifies, e.g., probing location
- "Logical" identifies schematic symbol node
- "Side" groups ports without connecting them
- "Symbol_left", etc. organize ports for schematic symbols
- Dot notation helps connect to IBIS, EMD, etc.
- Not shown: "Type" S or P for signal or power

Courtesy Walter Katz

Port-Mapping Syntax Examples (2 of 2)

- Connection to EMD for 4-bit DQ Nibble in a 2-rank DIMM (corrected)

```
[Begin Port Map]
Port 1 (Physical   20)  (Side EMD)  (Net DQ0) (Logical DQ0)
Port 2 (Physical   21)  (Side EMD)  (Net DQ1) (Logical DQ1)
Port 3 (Physical   22)  (Side EMD)  (Net DQ2) (Logical DQ2)
Port 4 (Physical   23)  (Side EMD)  (Net DQ3) (Logical DQ3)
Port 5 (Physical   25)  (Side EMD)  (Net DQS+) (Logical DQS+) (Diff_port 6)
Port 6 (Physical   26)  (Side EMD)  (Net DQS-) (Logical DQS-) (Diff_port 5)
Port 7 (Physical   27)  (Side mem1)  (Net DQ0) (Logical mem1_DQ0)
Port 8 (Physical   28)  (Side mem1)  (Net DQ1) (Logical mem1_DQ1)
Port 9 (Physical   29)  (Side mem1)  (Net DQ2) (Logical mem1_DQ2)
Port 10 (Physical   30)  (Side mem1)  (Net DQ3) (Logical mem1_DQ3)
Port 11 (Physical   31)  (Side mem1)  (Net DQS+) (Logical mem1_DQS+) (Diff_port 12)
Port 12 (Physical   32)  (Side mem1)  (Net DQS-) (Logical mem1_DQS-) (Diff_port 11)
Port 13 (Physical   33)  (Side mem2)  (Net DQ0) (Logical mem2_DQ0)
Port 14 (Physical   34)  (Side mem2)  (Net DQ1) (Logical mem2_DQ1)
Port 15 (Physical   35)  (Side mem2)  (Net DQ2) (Logical mem2_DQ2)
Port 16 (Physical   36)  (Side mem2)  (Net DQ3) (Logical mem2_DQ3)
Port 17 (Physical   37)  (Side mem2)  (Net DQS+) (Logical mem2_DQS+) (Diff_port 18)
Port 18 (Physical   38)  (Side mem2)  (Net DQS-) (Logical mem2_DQS-) (Diff_port 17)
[End Port Map]
```

- "Diff_port" identifies differential pairs
- "Net" idenfities ports in an extended net
- "Physical" identifies, e.g., probing location
- "Logical" identifies schematic symbol node
- "Side" groups ports without connecting them
- Not shown: "Reference"

Your Input is Needed!

- Is industry looking for increased connectivity features in Touchstone?
  - Are package connections to IBIS, EMD, and IBIS Interconnect directly in the file needed? Or is a “wrapper file” approach acceptable?
  - Should connections to IEEE 370, IEEE 2401 LPB, and/or JEDEC JEP-30 be directly included?
- Is the majority usage model interconnect (as opposed to RF devices)?
- Are naming and functional descriptions per port needed?
- What priority should be given to these new features?
- What has been missed?

Remember that adding features to the specification may add time for finalization and parser development