Interconnect Modeling: New Features for Rail Connections

Bob Ross, Teraspeed Labs
bob@teraspeedlabs.com

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Purpose

- **Some new keywords or features introduced for IBIS Version 7.0 that allow for simplified Rail (POWER or GND) nets**
- **Just a top-level introduction of some advanced features – details not important here**

Overview

- New, expanded Version 6.1 [Pin Mapping] options and new support for BIRD189 Interconnect Modeling features
- Existing [Pin Mapping] introduced as starting point
- New rules and new keywords and why
  - For "Rail" nets
  - Options for combining similar Rails (e.g., VDD rails)
- Appendix I – Example summary that combines everything
- Appendix II – Special case

V6.1 Syntax for [Pin Mapping]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1          IO1
2     IO2          IO2
3     IO3          IO3
4     IO4          IO4
|
| ... Rails with different bus_label entries
10    VSS          GND
11    VDD          POWER
12    VDD          POWER
13    VDD          POWER
14    VDD          POWER
|
```

- All POWER or GND pins required in [Pin Mapping] (pins 10-14)
- All I/O pins are documented (pins 1-4)
- pulldown_ref, pullup_ref and other column entries are bus_labels and show "shorted" bus_label names mapped to I/O buffers as their power terminals

```
[Pin Mapping] pulldown_ref pullup_ref
|
1               VSS          VDD   | BL0, BL1
2               VSS          BL2
3               VSS          BL3
4               VSS          BL4
|
| ... Rails and bus_label definitions
10              VSS          NC    | BL0 for VSS
11              NC           VDD   | BL1
12              NC           BL2
13              NC           BL3
14              NC           BL4
```

Version 6.1 [Pin Mapping] Limits

- **All rail pins must be listed (this can be a large number)**
- **Sometimes electrical field solvers "short" common rails for electrical extractions (e.g., all VSS as a reference terminal)**

BIRD182 [Pin Mapping]

- **Sets bus_label <value> = signal_name <value> for unlisted rail pin_names <names> in [Pin Mapping]**
- **[Pin] signal_name <entry> now has syntactical meaning, not just data sheet documentation**
- **Reduces pin_name <value>s that need to be listed**

BIRD182 [Pin Mapping]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1         IO1
2     IO2         IO2
3     IO3         IO3
4     IO4         IO4
|
| ... Rails with different bus_label entries
10    VSS         GND
11    VDD         POWER
12    VDD         POWER
13    VDD         POWER
14    VDD         POWER
|
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1               VSS           VDD   | BL0, BL1
2               VSS           BL2
3               VSS           BL3
4               VSS           BL4
|
| ... Rails and bus_label definitions
| 10              VSS             NC    | BL0 for VSS
| 11              NC              VDD   | BL1
12              NC            BL2
13              NC            BL3
14              NC            BL4
```

bus_label = signal_name by default

BIRD189 [Bus Label]

- **Directly associates bus_label <value> with signal_name <value>**
- **Allows for more bus_label values than available through direct pin_name references**
- **Supports rails split into many paths**

BIRD189 [Bus Label]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1          IO1
2     IO2          IO2
3     IO3          IO3
4     IO4          IO4
|
| ... Rails with different bus_label entries
10    VSS          GND
11    VDD          POWER
12    VDD          POWER
13    VDD          POWER
14    VDD          POWER
|
```

```
[Bus Label]   signal_name
|
BL3           VDD
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1             VSS          VDD   | BL0, BL1
2             VSS          BL2
3             VSS          BL3
4             VSS          BL4
|
| ... Rails and bus_label definitions
| 10            VSS            NC    | BL0 for VSS
| 11            NC             VDD   | BL1
12            NC           BL2
| 13            NC             BL3
14            NC           BL4
```

BIRD189 [Die Supply Pads]

- Declares rail pad_name <values> for only the die pad interface (Pad_Rail)
- Associates pad_name <value> with a signal_name <value> and optionally as a bus_label <value>
- Provides another way to define a new bus_label <value>
- Special default case in Appendix II

BIRD189 [Die Supply Pads]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1       IO1
2     IO2       IO2
3     IO3       IO3
4     IO4       IO4
|
| ... Rails with different bus_label entries
10    VSS       GND
11    VDD       POWER
12    VDD       POWER
13    VDD       POWER
14    VDD       POWER
|
```

pad_name (Pad4) defined for the die pad interface but not used in this example

```
[Die Supply Pads] signal_name bus_label
|
Pad4              VDD         BL4
```

```
[Bus Label]   signal_name
|
BL3           VDD
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1             VSS          VDD   | BL0, BL1
2             VSS          BL2
3             VSS          BL3
4             VSS          BL4
|
| ... Rails and bus_label definitions
| 10            VSS            NC    | BL0 for VSS
| 11            NC             VDD   | BL1
12            NC           BL2
| 13            NC             BL3
| 14            NC             BL4
```

What is Supported?

- **Rails connections: one-to-many or many-to-one**
  - **More pad_name connections than pin_name connections**
  - **Less pad_name connections than pin_name connections**
  - **Rail simplification to single path by signal_name <value> or bus_label <value>**
- **More ways to create bus_labels**

Appendix I Summary
Four Ways (with Simple Example)

- **[Pin Mapping] (existing Version 6.1)**
- **Default [Pin] signal_name ([Pin Mapping] extension)**
  - **BIRD182**
- **[Bus Label]**
  - **BIRD189**
- **[Die Supply Pads]**
  - **BIRD189**
- **Any combination of above**
- **"Simple" means one net per example here**

Version 6.1 Syntax [Pin Mapping]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1       IO1
2     IO2       IO2
3     IO3       IO3
4     IO4       IO4
|
| ... Rails with different bus_label entries
10    VSS       GND
11    VDD       POWER
12    VDD       POWER
13    VDD       POWER
14    VDD       POWER
|
```

bus_label for each GND and POWER pin_name

```
[Pin Mapping] pulldown_ref pullup_ref
|
1             VSS          VDD    | BL0, BL1
2             VSS          BL2
3             VSS          BL3
4             VSS          BL4
|
| ... Rails and bus_label definitions
10            VSS          NC     | BL0 for VSS
11            NC           VDD    | BL1
12            NC           BL2
13            NC           BL3
14            NC           BL4
```

BIRD182 [Pin Mapping]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1         IO1
2     IO2         IO2
3     IO3         IO3
4     IO4         IO4
|
| ... Rails with different bus_label entries
10    VSS         GND
11    VDD         POWER
12    VDD         POWER
13    VDD         POWER
14    VDD         POWER
|
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1               VSS           VDD   | BL0, BL1
2               VSS           BL2
3               VSS           BL3
4               VSS           BL4
|
| ... Rails and bus_label definitions
| 10              VSS             NC    | BL0 for VSS
| 11              NC              VDD   | BL1
12              NC            BL2
13              NC            BL3
14              NC            BL4
```

bus_label = signal_name by default

BIRD189 [Bus Label]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1       IO1
2     IO2       IO2
3     IO3       IO3
4     IO4       IO4
|
| ... Rails with different bus_label entries
10    VSS       GND
11    VDD       POWER
12    VDD       POWER
13    VDD       POWER
14    VDD       POWER
|
```

```
[Bus Label]   signal_name
|
BL3           VDD
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1             VSS          VDD   | BL0, BL1
2             VSS          BL2
3             VSS          BL3
4             VSS          BL4
|
| ... Rails and bus_label definitions
| 10            VSS            NC    | BL0 for VSS
| 11            NC             VDD   | BL1
12            NC           BL2
| 13            NC             BL3
14            NC           BL4
```

BIRD189 [Die Supply Pads]

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1       IO1
2     IO2       IO2
3     IO3       IO3
4     IO4       IO4
|
| ... Rails with different bus_label entries
10    VSS       GND
11    VDD       POWER
12    VDD       POWER
13    VDD       POWER
14    VDD       POWER
|
```

```
[Bus Label]   signal_name
|
BL3           VDD
```

```
[Die Supply Pads] signal_name bus_label
|
Pad4              VDD         BL4
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1             VSS           VDD   | BL0, BL1
2             VSS           BL2
3             VSS           BL3
4             VSS           BL4
|
| ... Rails and bus_label definitions
| 10            VSS             NC    | BL0 for VSS
| 11            NC              VDD   | BL1
12            NC              BL2
| 13            NC              BL3
| 14            NC              BL4
```

All Together

- Simple example shows all four methods:
  - One POWER or GND net for each bus_label
  - Normally more nets would be combined
- Explicit pin_name definitions for bus_label entries
- signal_name for bus_labels:
  - by default
  - by [Bus Label]
  - by [Die Supply Pads]
- Any or all methods can be used at once
- Buffer_Rail in Interconnect BIRD189 needs [Pin Mapping] for buffer rail terminals

Appendix II
[Die Supply Pads] Default Note

- **[Die Supply Pads] without bus_label entry defaults to bus_label <value> = signal_name <value_>**
- **If [Pin Mapping] uses [Pin] signal_name = bus_label, then [Die Supply Pads] default entry is redundant**

- **Usage limits outside of the scope of this presentation**
- **Fifth way to define and use bus_label**

[Die Supply Pads] Default Note

```
[Pin] signal_name  model_name
|
| ... IO Models
1     IO1          IO1
2     IO2          IO2
3     IO3          IO3
4     IO4          IO4
|
| ... Rails with different bus_label entries
10    VSS          GND
11    VDD          POWER
12    VDD          POWER
13    VDD          POWER
14    VDD          POWER
|
```

bus_label = signal_name, either redundant with BIRD182 or may be used with Pad_Rail or Pin_Rail (*)

```
[Die Supply Pads] signal_name bus_label
|
Pad4                VDD     | VDD by default
```

```
[Bus Label]   signal_name
|
BL3           VDD
```

```
[Pin Mapping] pulldown_ref pullup_ref
|
1             VSS          BL1   | BL0, BL1 (was VDD)
2             VSS          BL2
3             VSS          BL3
4             VSS          BL4
|
| ... Rails and bus_label definitions
| 10            VSS            NC    | BL0 for VSS
11            NC           BL1   | BL1 (was VDD)
12            NC           BL2
| 13            NC             BL3
14            NC           BL4   | Explicitly defined
```

*** Buffer_Rail bus_label VDD not with any I/O here**