Introducing IBIS Version 6.1

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Agenda

IBIS 6.1 Overview and Development

Key Features

- AMI Improvements
- Traditional IBIS Improvements

Methods for Providing Feedback

References

Specifications and Activities

- IBIS Version 6.1 approved Sept. 11, 2015
  - Nearly two years to the day after Ver. 6.0 approval
  - Freely available at http://www.ibis.org/ver6.1/

- Waiting for IBIS 6.2 for possible SAE standardization

- A free syntax checker/parser under development
  - Release tentatively expected in November
  - Source code license is available for purchase
  - Current ibischk6 licensees will receive a free update

Key Features of IBIS 6.1

- AMI improvements
  - Extending IBIS-AMI for PAM4 Analysis
  - Model dependencies are supported through a new API
  - Buffer directionality for AMI models

- “Traditional” IBIS improvements
  - V-t table delay and overclocking
  - Package RLC Matrix Diagonals
  - Power Pin Package Modeling
  - New keyword [Initial Delay] for Submodels and Driver Schedules

- Plus corrections, clarifications, and a recommendation

AMI Improvements

- PAM4 Signaling
  - Expands IBIS's AMI support beyond 2 levels (NRZ) to 4 (PAM4)
  - Adds "Modulation", "PAM4_Mapping", offset and threshold Reserved Parameters
  - Re-defines bit-time and clock-times concepts

- Model Dependencies
  - Allows the final values of some .ami parameters to depend on the values of others, or of IBIS [Model]s
  - New flow resolves dependencies before simulation
  - Adds "AMI_Resolve" and "AMI_Resolve_Close" functions
  - Adds "Resolve_Exists" and "Model_Name" Reserved Parameters
  - Adds "Dep" Usage Type

AMI Improvements (2)

- Buffer Directionality
  - Paving the way for DDR4 and beyond under AMI
  - Associates all Reserved Parameters and Model_Types with directions (Tx, Rx)
    - Most Serdes buffers are Tx-only or Rx-only
    - DDR4 DQ buffers are I/O (bi-directional)
  - Enables explicit information to be used by EDA tools about the direction for a given I/O buffer in a particular simulation
  - Adds “Direction” descriptor to all Reserved Parameters
  - Adds “Executable_Tx” and “Executable_Rx” subparameters to the [Algorithmic Model] keyword

Traditional IBIS Improvements

- Overclocking and delay
  - [Initial Delay] defines the explicit amount of time, before transitions, embedded in the V-t and any I-t tables
  - Supported for both single-Model and [Driver Schedule] structures

- Package and Power Pin Modeling
  - Diagonal package matrix values are enforced positive-only, and more mathematical assumptions are documented
  - More rigorous rules are defined for EDA tool interpretation of partial Package Models which do not cover the entire [Pin] list
  - Added support for [Merged Pins] where a single pin covers the parasitics of multiple physical pins

Feedback is Welcome

- Anyone may submit IBIS specification change proposals (BIRDs – Buffer Issue Resolution Documents)
  - This is the primary mechanism for making IBIS changes
  - http://ibis.org/birds/
- Bugs and enhancement requests may also be proposed
  - The BUG report covers both
  - http://ibis.org/bugs/ibischk
- The IBIS Open Forum and Task Group teleconferences welcome public participation

Your feedback is vital for keeping IBIS relevant and useful to the industry!

References

- IBIS Web site: www.ibis.org
  - Links to Task Groups available there
- Specifications
  - IBIS 6.1: www.ibis.org/ver6.1/
  - IBISCHK6 parser (6.1 in progress): www.ibis.org/ibischk6/
  - Touchstone: www.ibis.org/touchstone_ver2.0/
- Summit Presentations
  - www.ibis.org/summits/
- IBIS 4.0 Cookbook
  - www.ibis.org/cookbook/
- Training
  - www.ibis.org/training/