JEITA EDA -WG Activity

Oct 31, 2006
IBIS Summit in Japan

JEITA EDA-WG
Takeshi Watanabe (NEC Electronics)

JEITA ; Japan Electronics and Information Technology Industries Association

Outlines

1. JEITA EDA-WG Activities
2. Short Term Direction of JEITA EDA WG
3. Study of Interconnect Model
4. JEITA IBIS Model Portal site Plan

1. JEITA EDA-WG Activities

Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics

Cellular Phone, LCD /PDP TV,
Digital Camera/Video, DVD Recorder

(Digital , RF, and Analog circuits)

Auto Mobile Electronics ?

(Motor Drive, EMC)

< Applicability of IBIS V4.1 >

EMI, SI and PI
for Digital Consumer Electronics

<Background>

EMI **High-speed Clock Frequency**

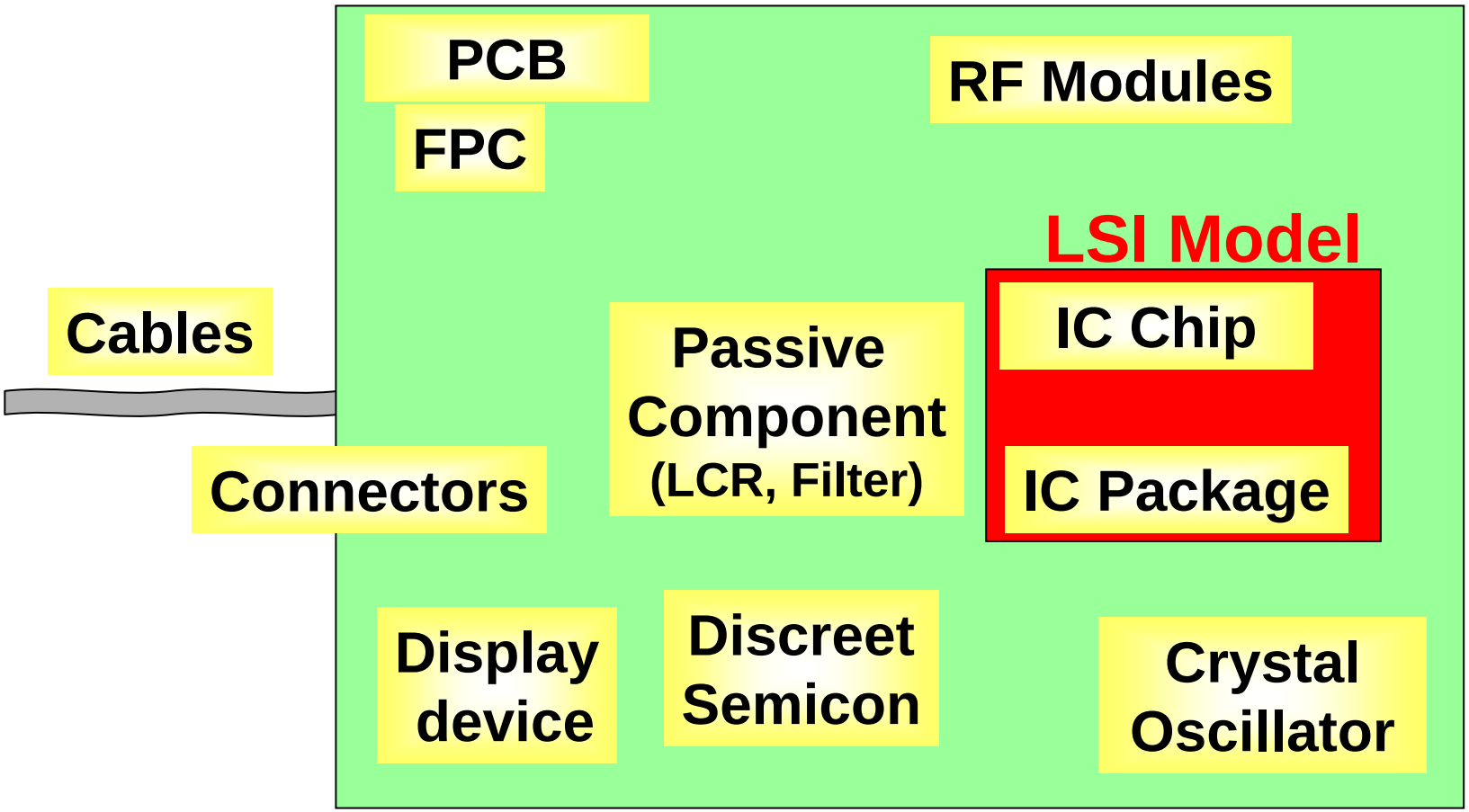
SI **DDR, PCI, PCI-Express**

PI **High density and Large scale IC**

SiP and Module, PCB level

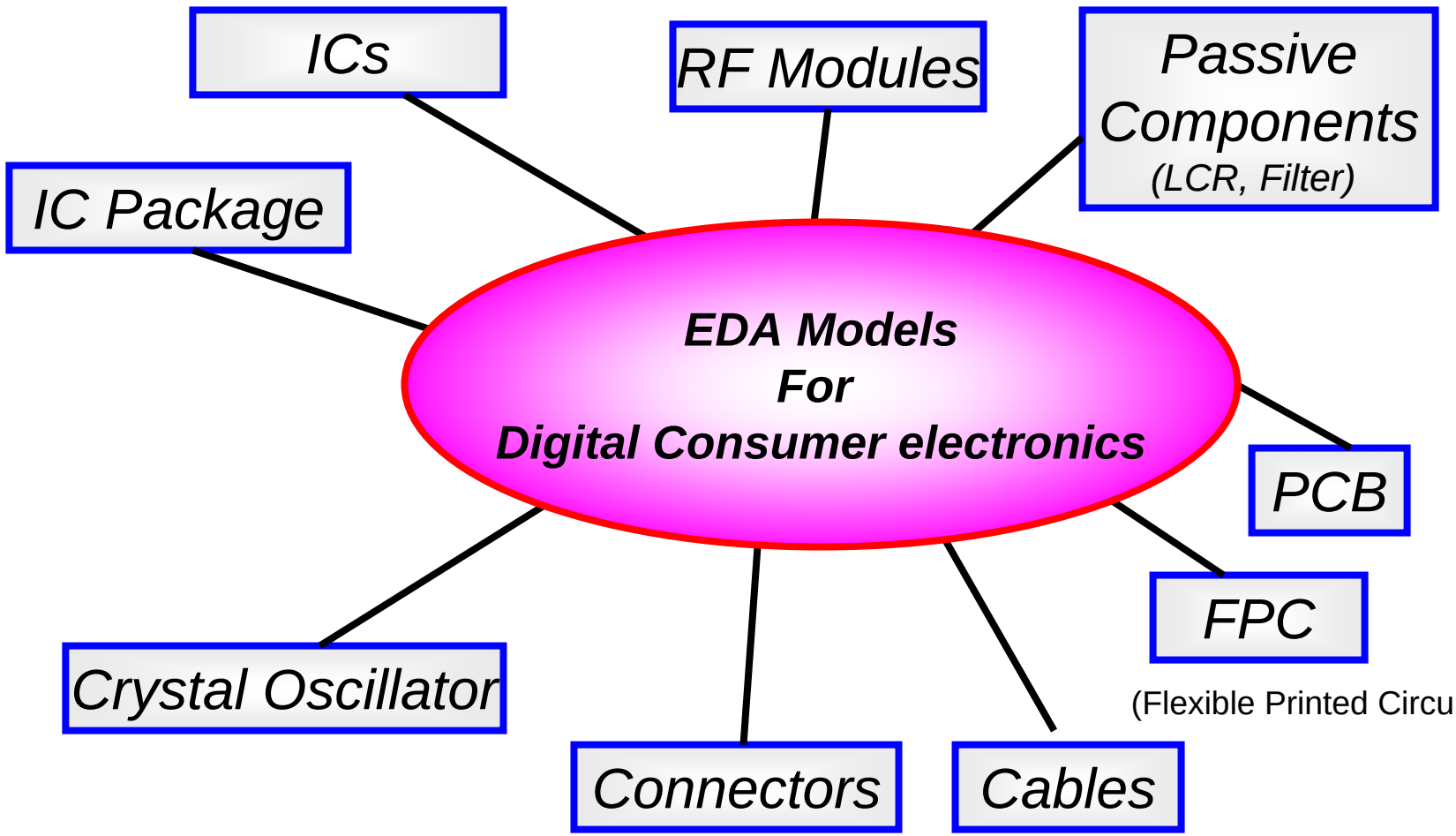
EMI, SI and PI Simulation Technology

EDA Model for EMI, SI and PI Simulation



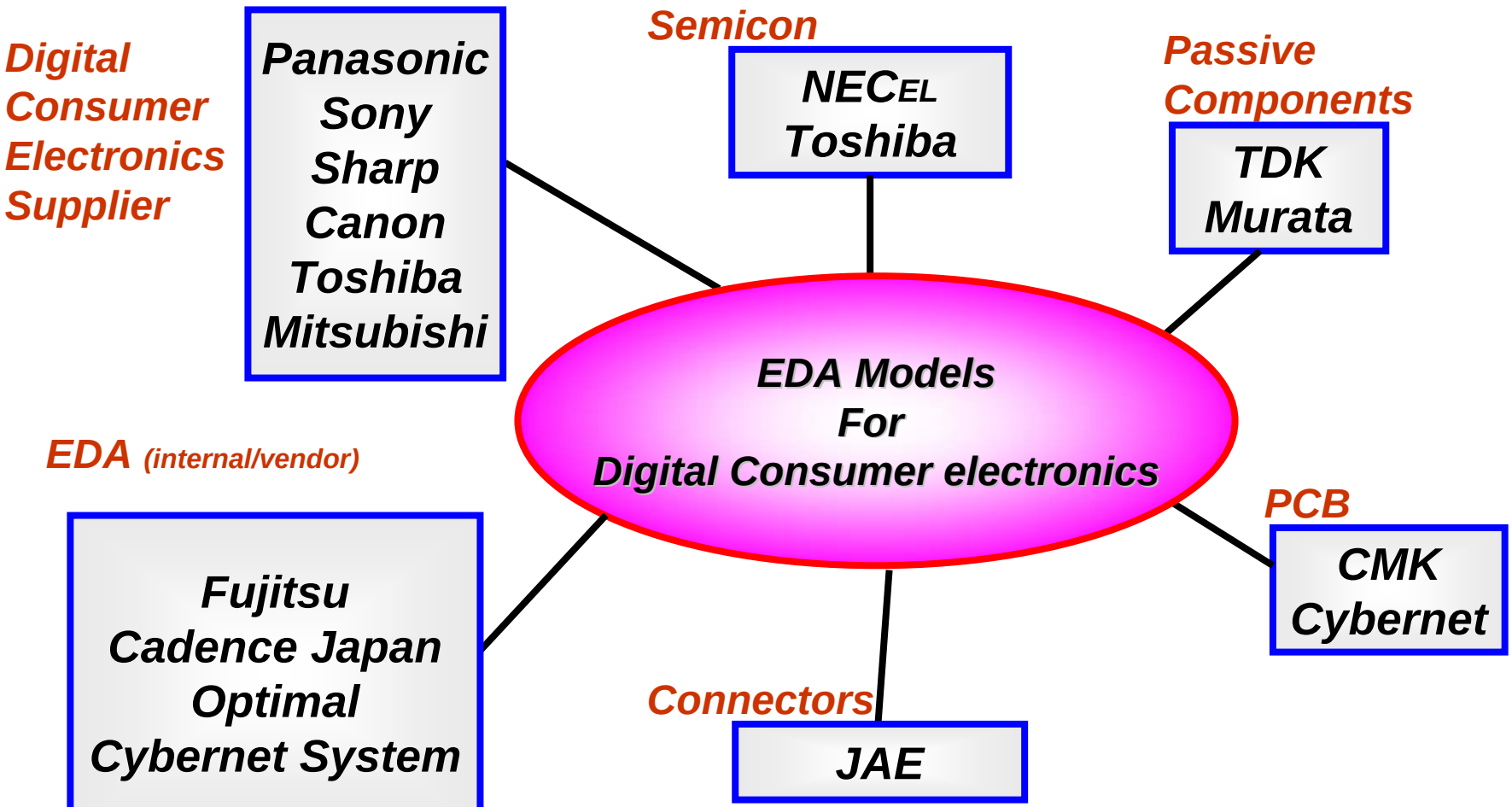
Focus of EDA Model for Simulation

9 components



JEITA EDA-WG Member

16 Major Companies



2. Short Term Direction of JEITA EDA WG

- **Study of Interconnect Model**
- **EDA Models of Passive Components and Connector and other Components**
- **JEITA IBIS Model WEB**
- **Discussion about Case study of Simulation for Digital Consumer Electronics and JEITA-IBIS Joint meeting periodically**

Study of Interconnect Model

JEITA IBIS Model Portal site Plan

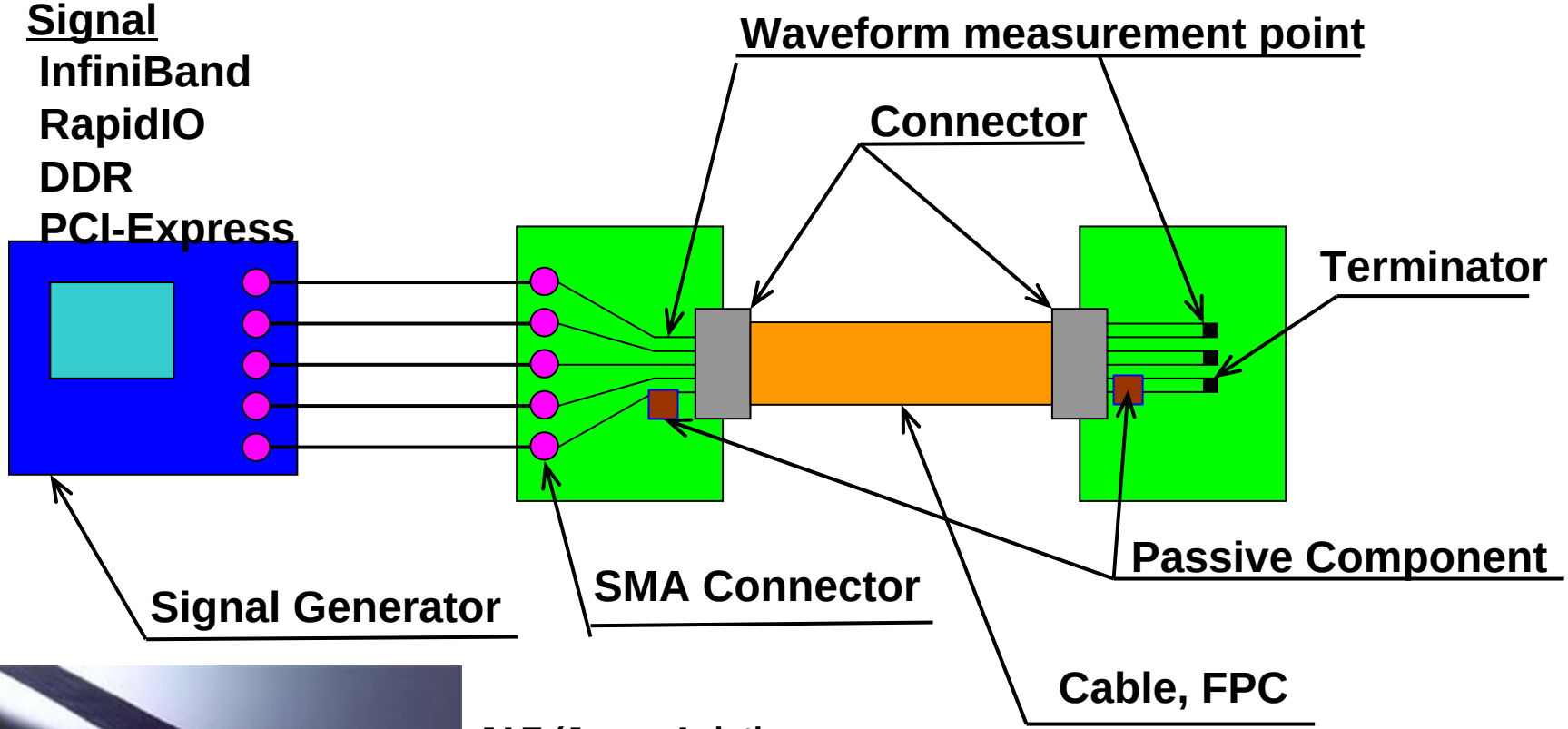
		EDA Model					EDA Tool (recommned)	Environment for the usage of EDA Model
		ICs	Passive Componets	Connectors	PCB board	Cable		
SI	＜1Gbps	◎	○	○	○	○	○	○
	＞1Gbps	○	○	○	○	○	○	○
EMI	<3GHz	○	○	○	○	○	○	○
PI	<3GHz	○	○		○		○	○

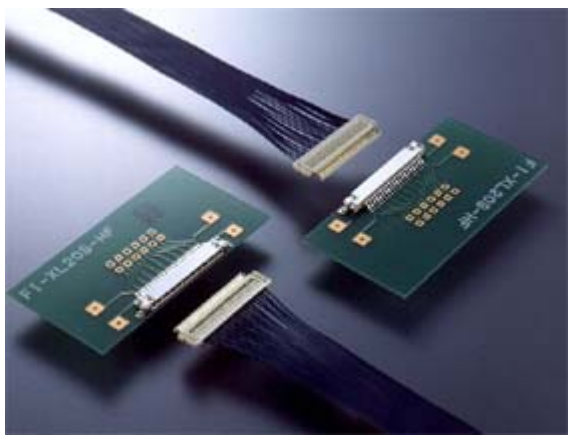
◎ foremost task

3. Study of Interconnect Model

SI Model (Connector, PCB, Cable)

Signal
InfiniBand
RapidIO
DDR
PCI-Express





JAE (Japan Aviation Electronics Industry)
FI-X Series

Study of Interconnect Model for Signal Integrity

- Target Application; DDR, PCI-Express etc.
- EDA Model; Connectors,

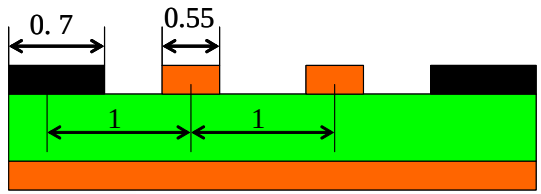
  Passive Components,

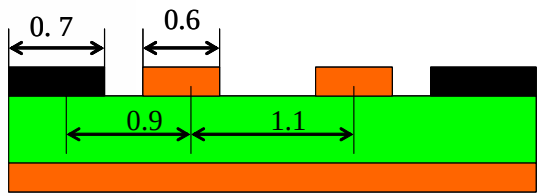
  PCB (Via, Pattern),

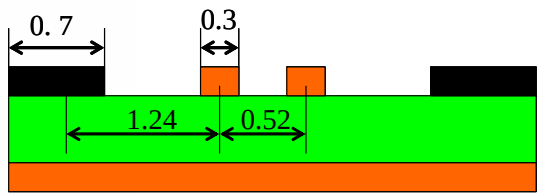
  LSI
- Simulation Tool; Cadence, etc.

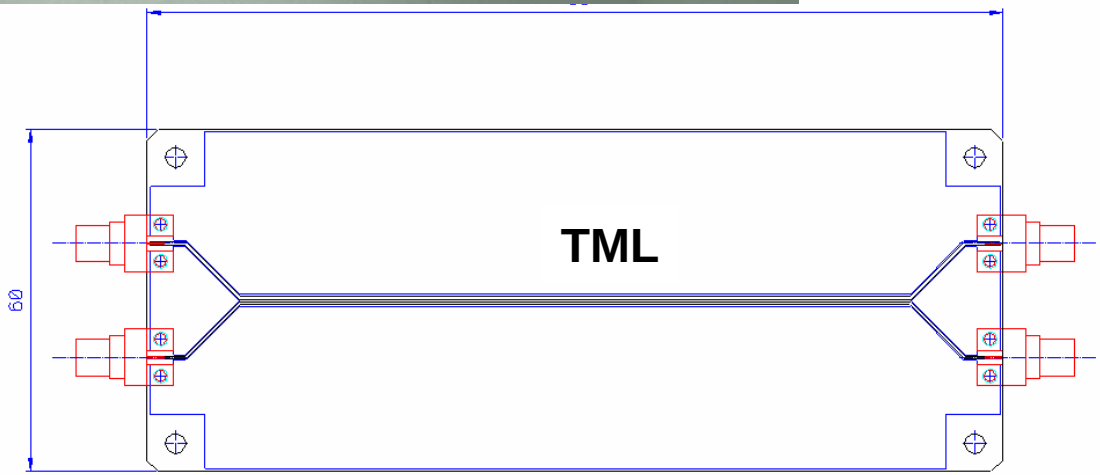
TML

layer structure





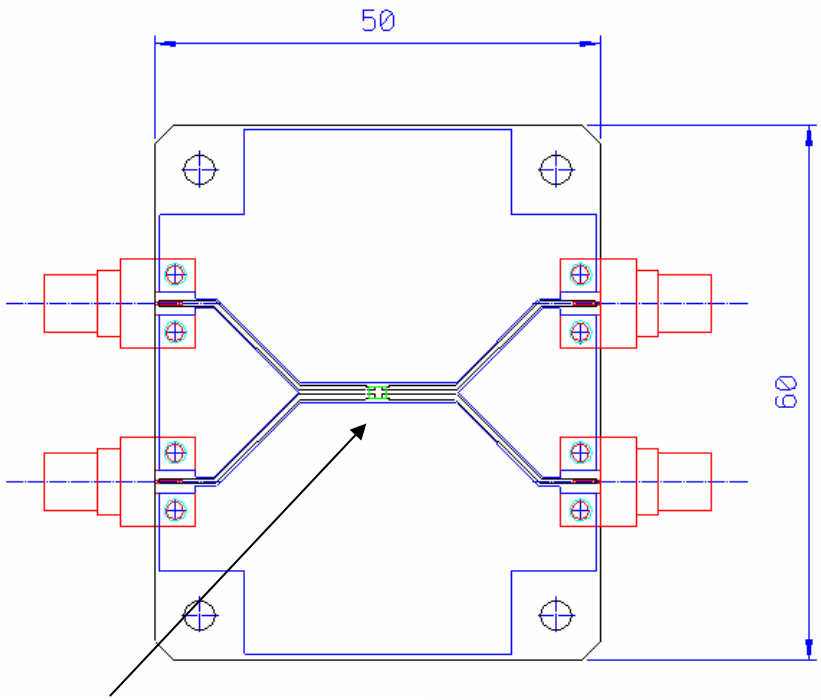


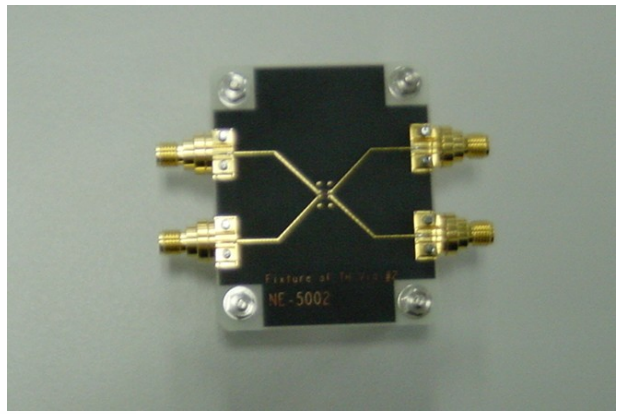


SMA Connector

Spacer

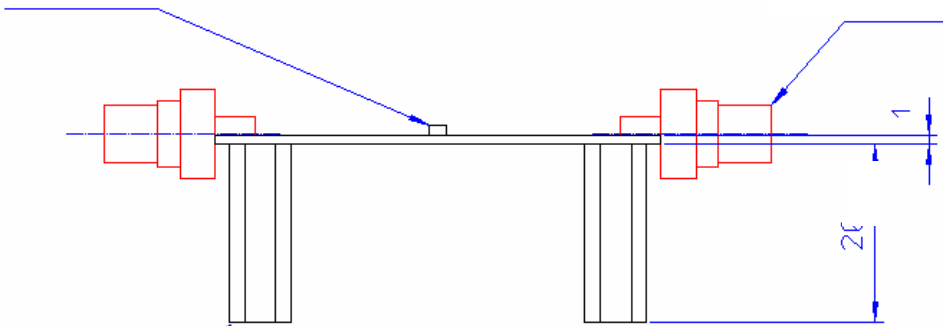
Passive Components





Passive Components

SMA Connector



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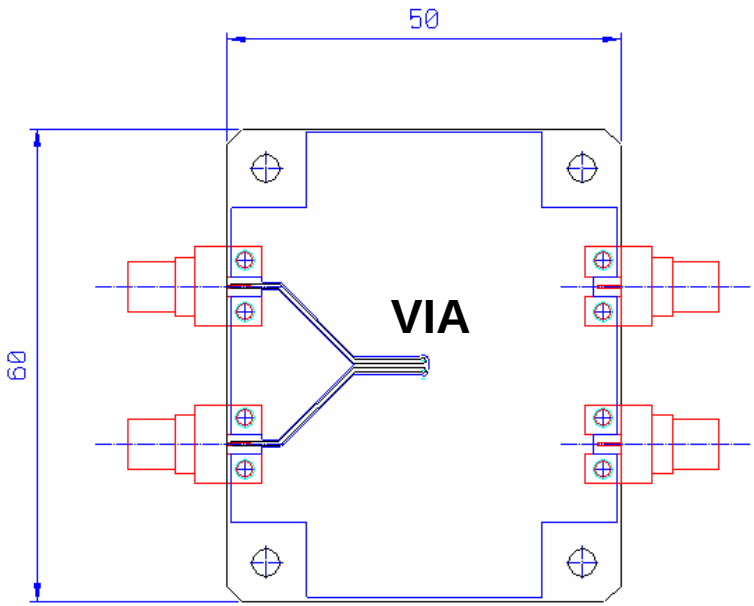
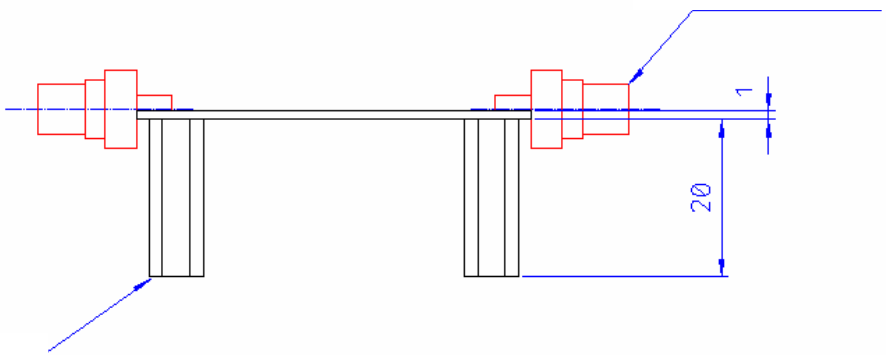
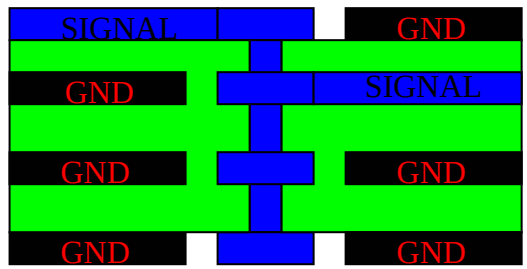
VIA

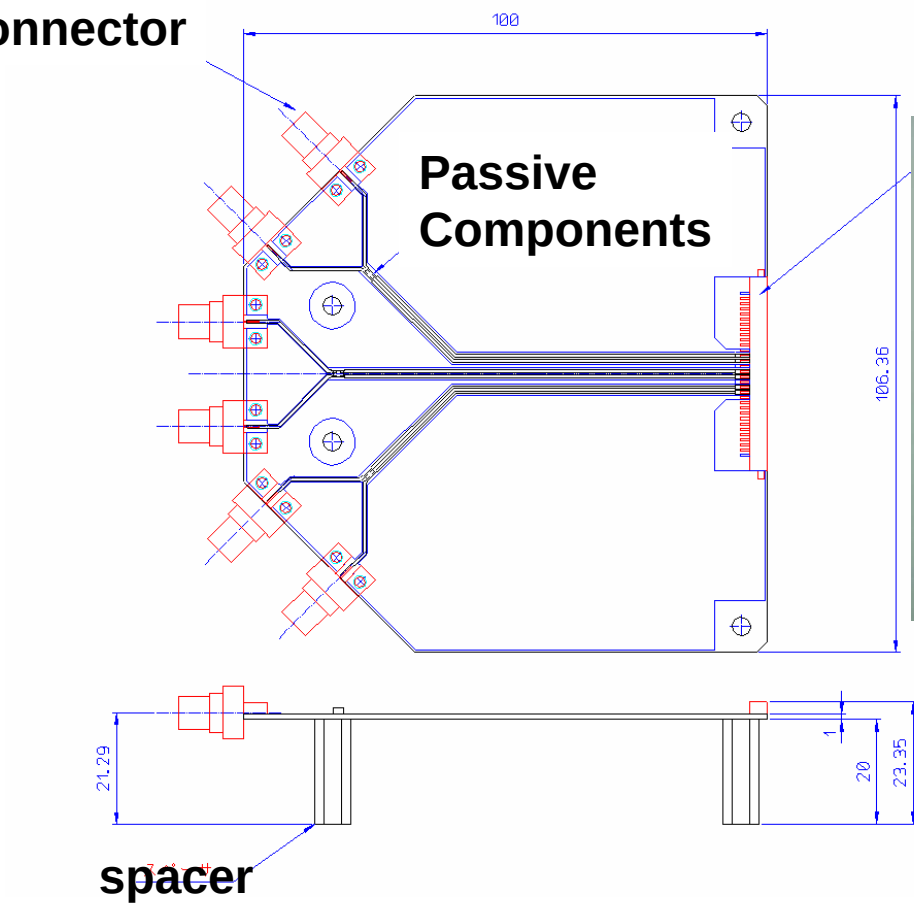


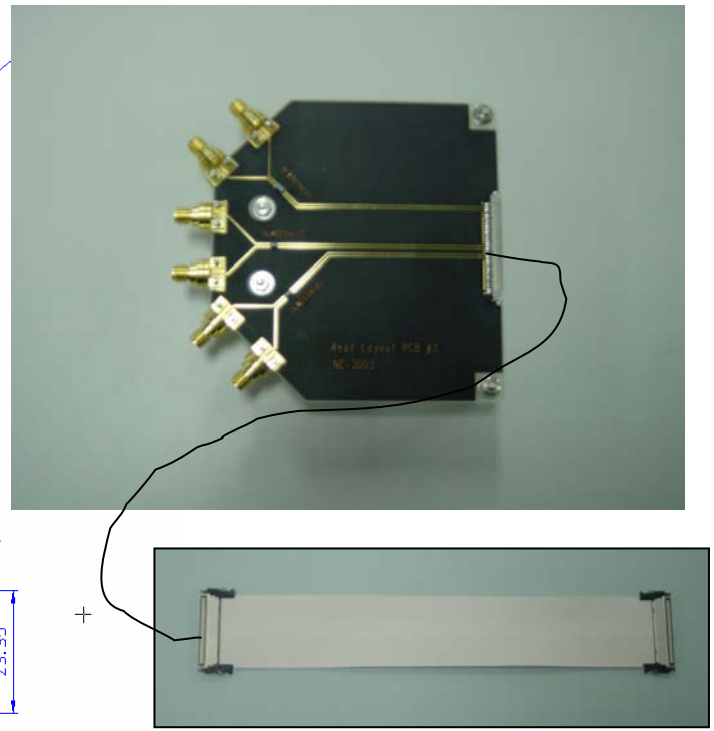




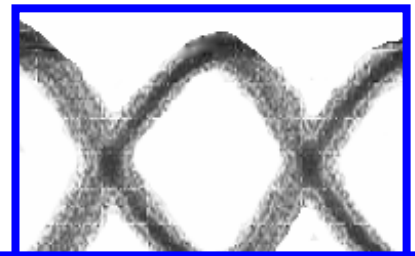
All Component
(TML, Passive Components, VIA, Connector)

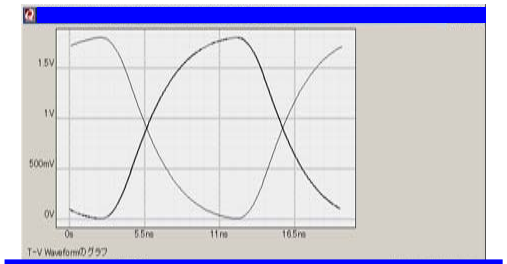
SMA Connector





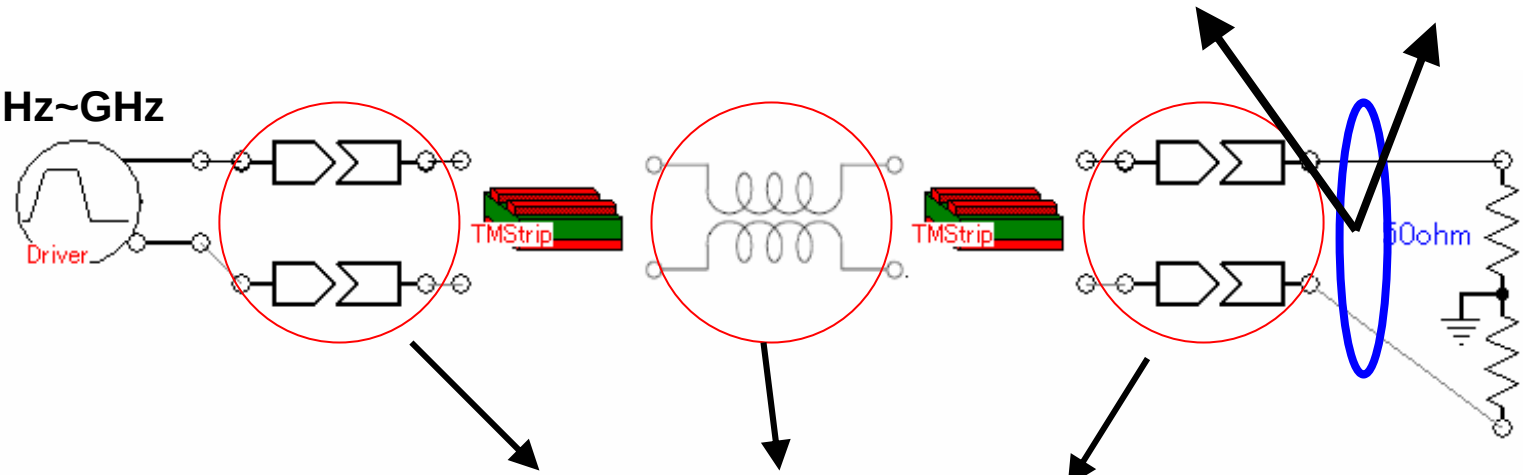
Compare Measurement with Simulation





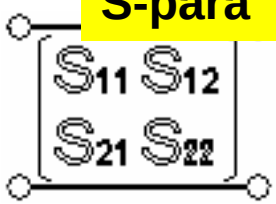
Measurement **Simulation**

MHz~GHz



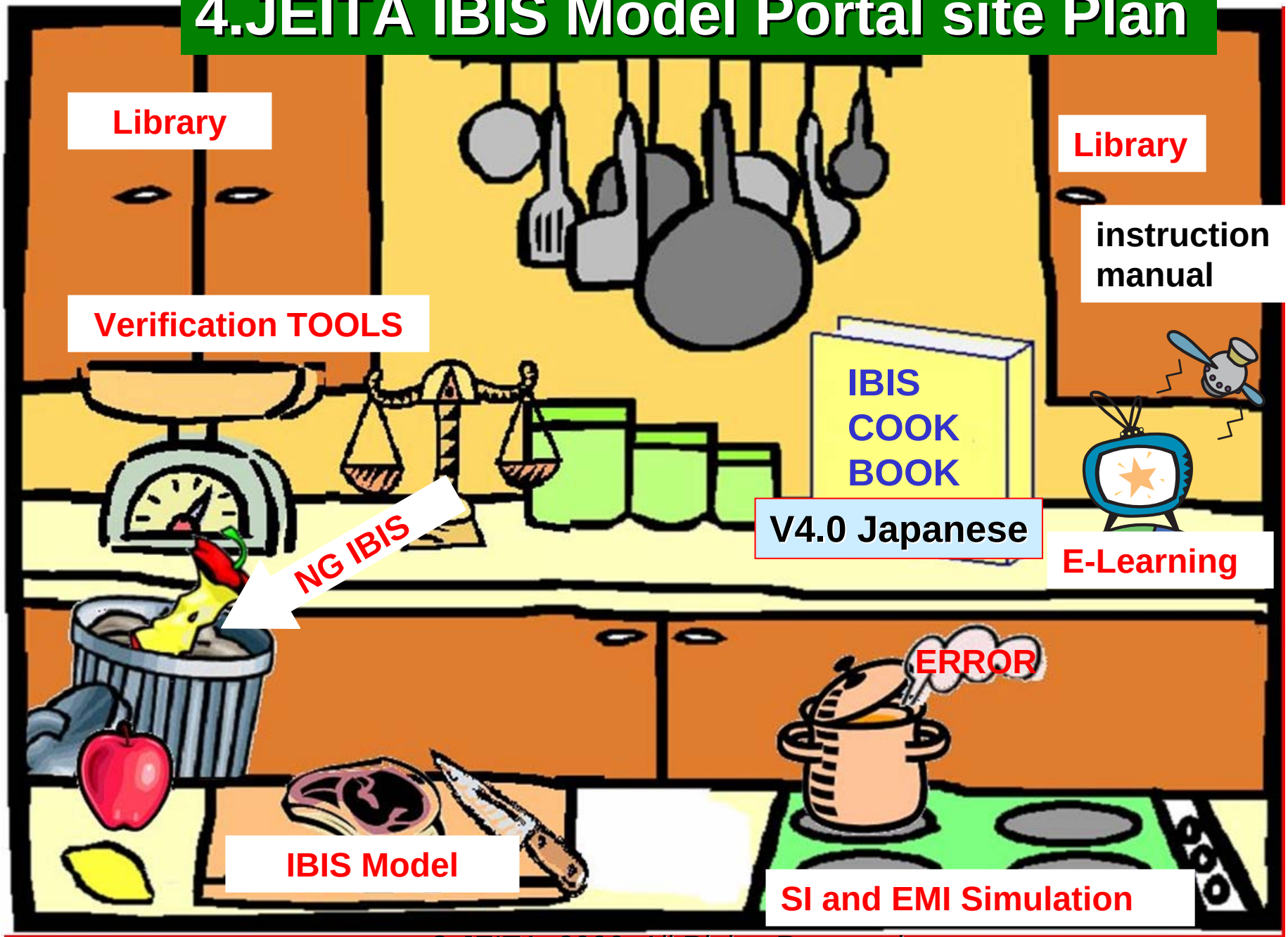
Model

S-para **Spice** **RLGC**



Ω/H/S/F

4.JEITA IBIS Model Portal site Plan



We hope to discuss case study of IBIS with you periodically

Thank you for all the help EIA/IBIS Committee!