# JEITA EDA -WG Activity and Study of Interconnect Model Part-3

**Oct 27, 2006**
**IBIS SUMMIT in China**

**JEITA EDA-WG**
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**Hiroaki Ikeda (Japan Aviation Electronics)**

*JEITA ; Japan Electronics and Information Technology Industries Association*

# Outlines

1. JEITA EDA-WG Activities
2. Short Term Direction of JEITA EDA WG
3. Study of  Interconnect Model
4. Progress Report

# 1. JEITA EDA-WG Activities

## Objectives of JEITA EDA

**EDA Model for**

**Digital Consumer Electronics**

**Cellular Phone, LCD /PDP TV,**
**Digital Camera/Video, DVD Recorder**

**(Digital , RF, and Analog circuits)**

**Auto Mobile Electronics ?**

**(Motor Drive, EMC)**

**< Applicability of IBIS V4.1 >**

# EMI, SI and PI
# for Digital Consumer Electronics

**<Background>**

**EMI** **High-speed Clock Frequency**

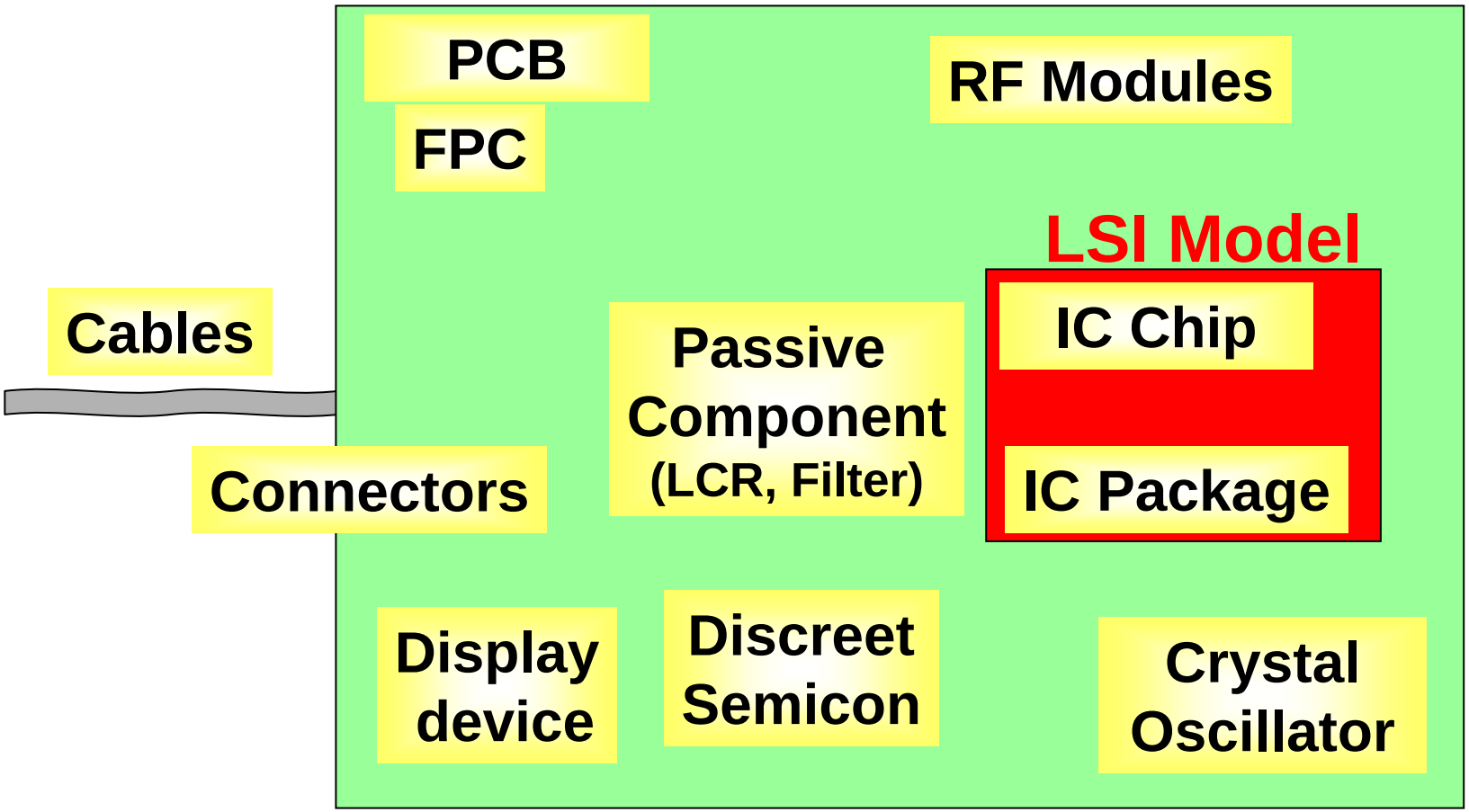
**SI** **DDR, PCI, PCI-Express**

**PI** **High density and Large scale IC**

**SiP and Module, PCB level**

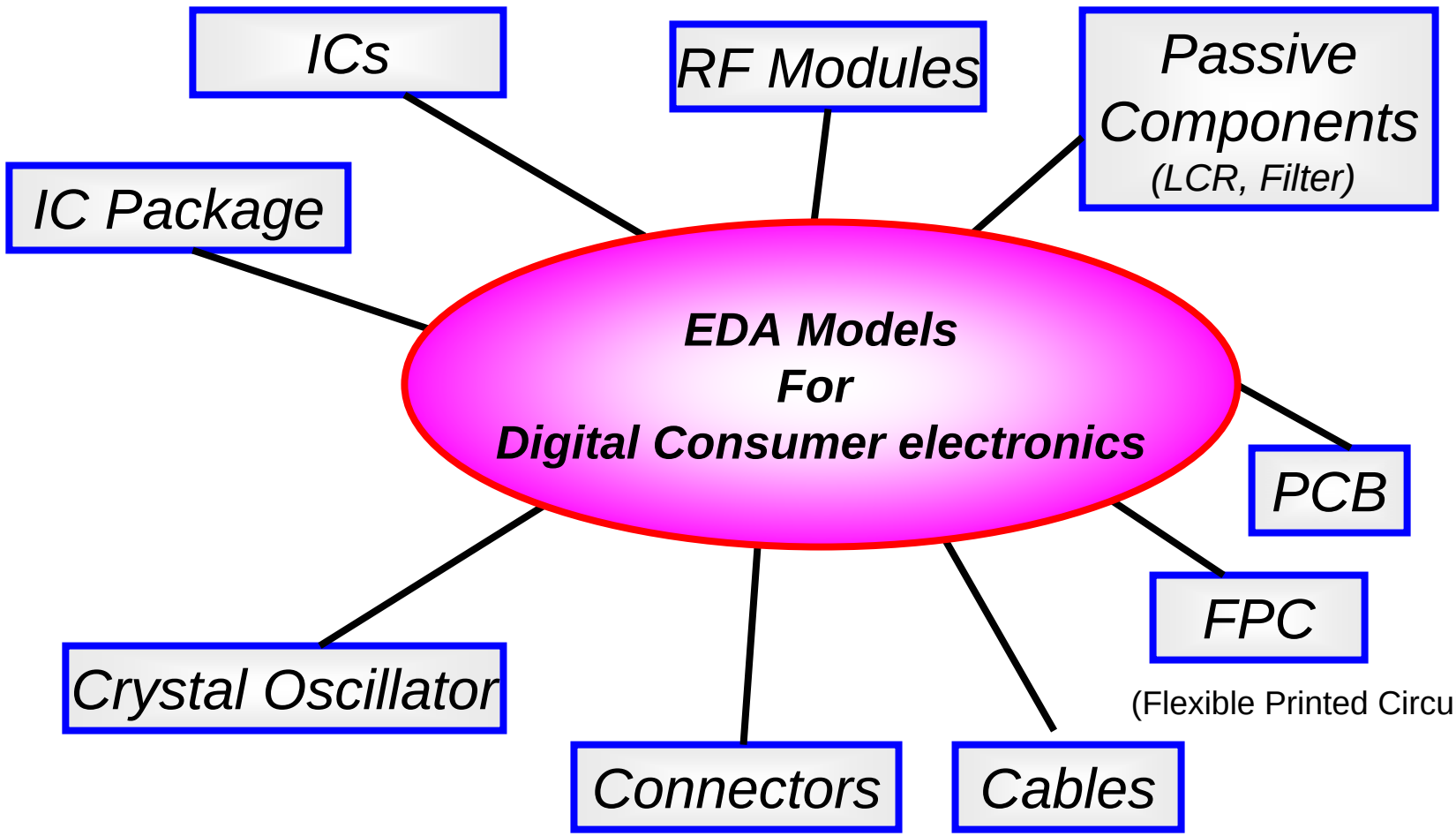
**EMI, SI and PI Simulation Technology**

# EDA Model for EMI, SI and PI Simulation



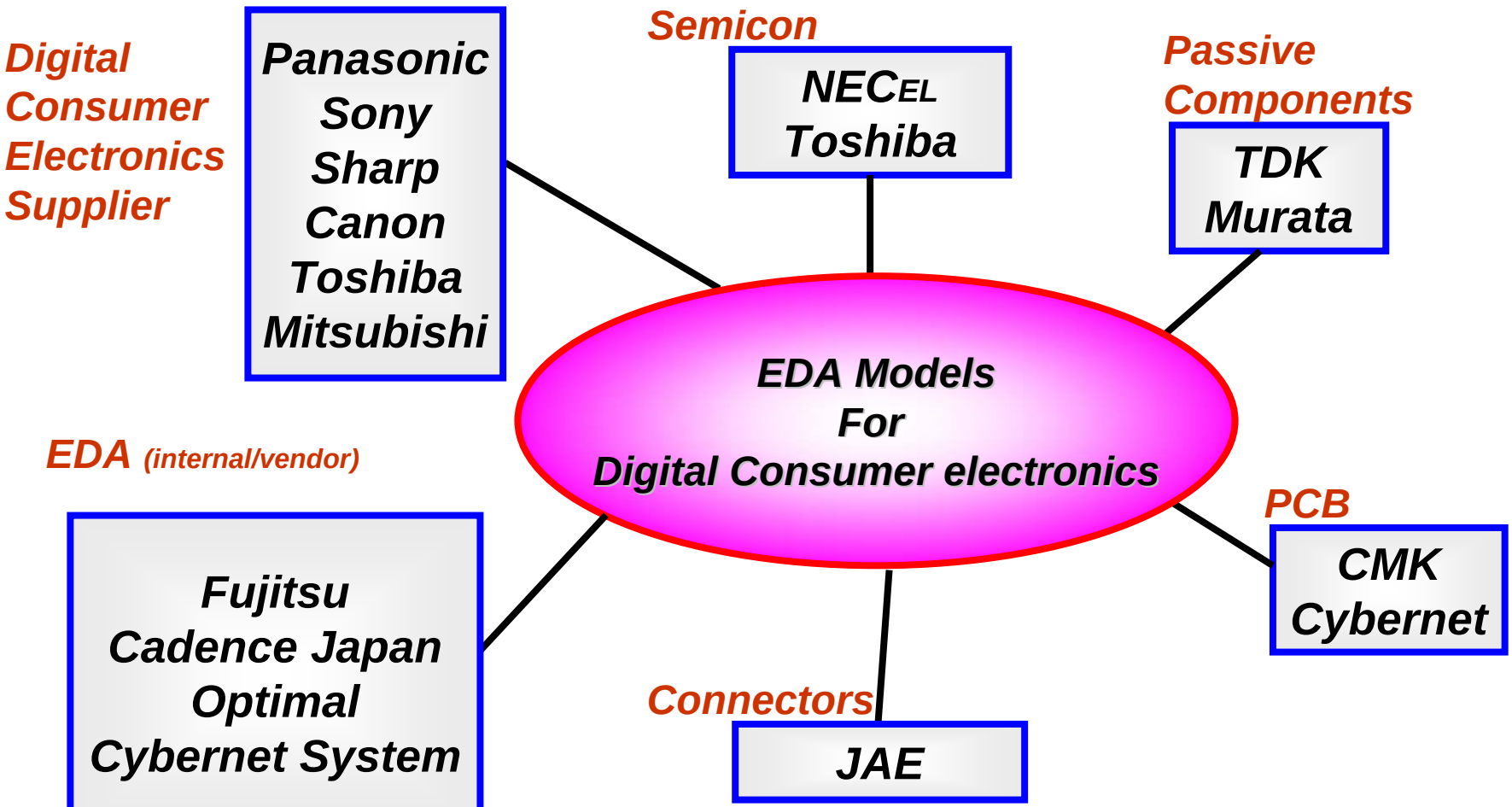
# Focus of EDA Model for Simulation

## 9 components



# JEITA EDA-WG Member

## 16 Major Companies

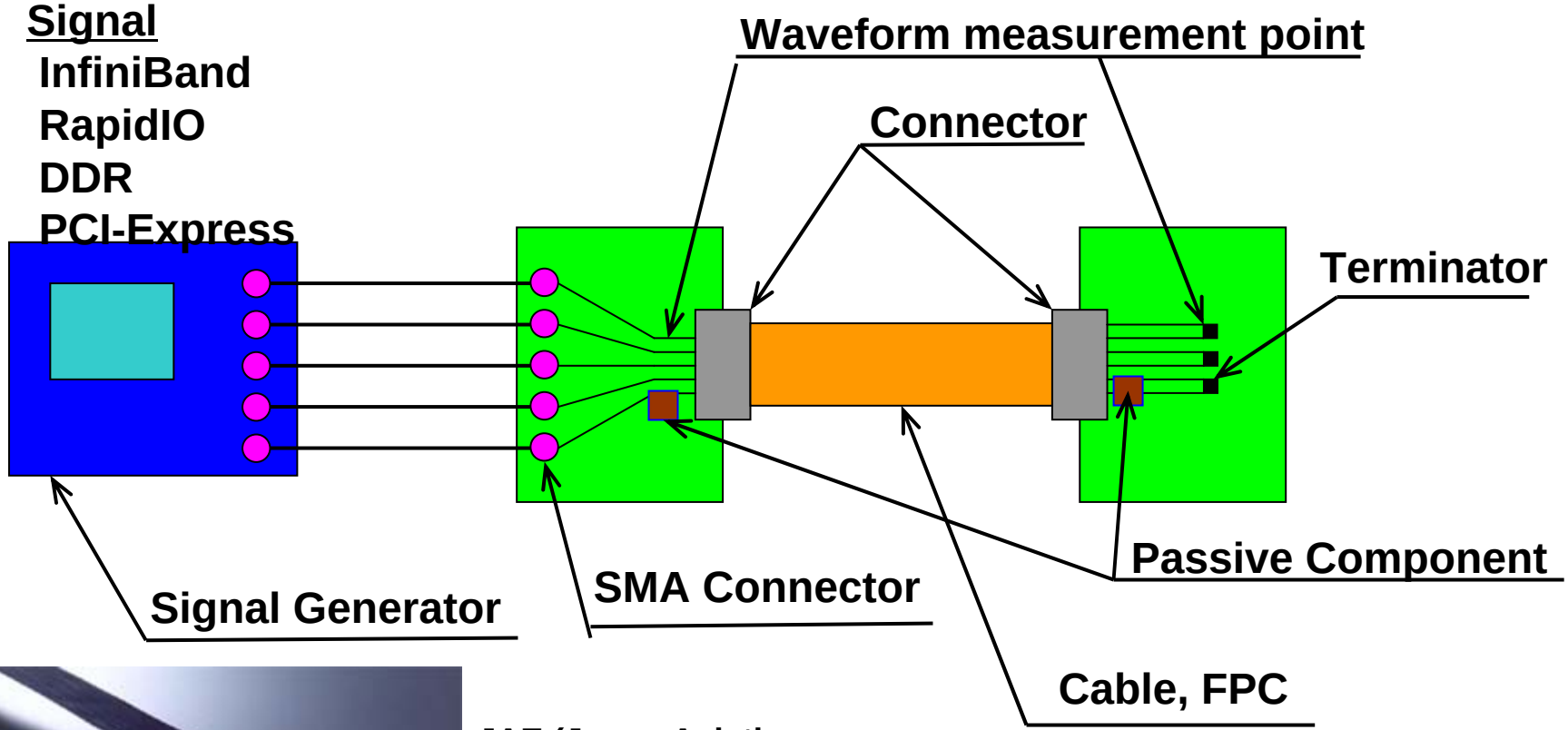


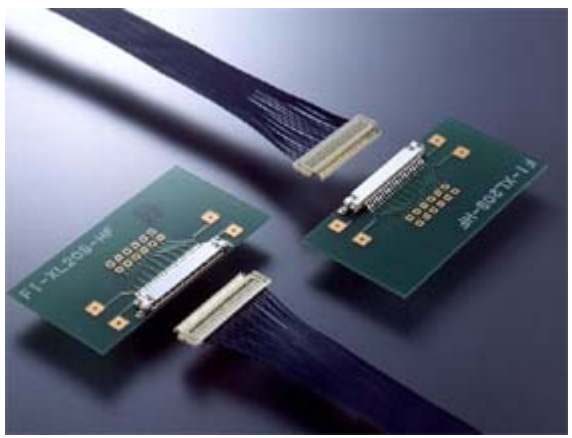
# 2. Short Term Direction of JEITA EDA WG

- **Study of Interconnect Model**
- **EDA Models of Passive Components and Connector and other Components**
- **JEITA IBIS Model WEB**
- **Discussion about Case study of Simulation for Digital Consumer Electronics and JEITA-IBIS Joint meeting periodically**

# 3. Study of Interconnect Model

## SI Model (Connector, PCB, Cable)



JAE (Japan Aviation Electronics Industry)
FI-X Series

# Study of Interconnect Model for Signal Integrity

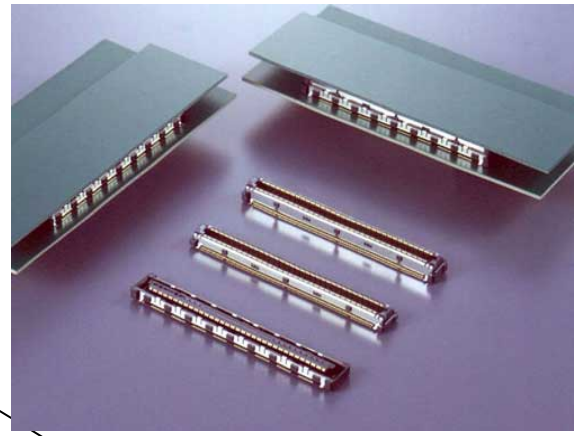
- Target Application; DDR, PCI-Express etc.
- EDA Model; Connectors,

  Passive Components,

  PCB (Via, Pattern),

  LSI
- Simulation Tool; Cadence, etc.

# SI Model (Connector- Type B; stacked module, PCB, Cable)

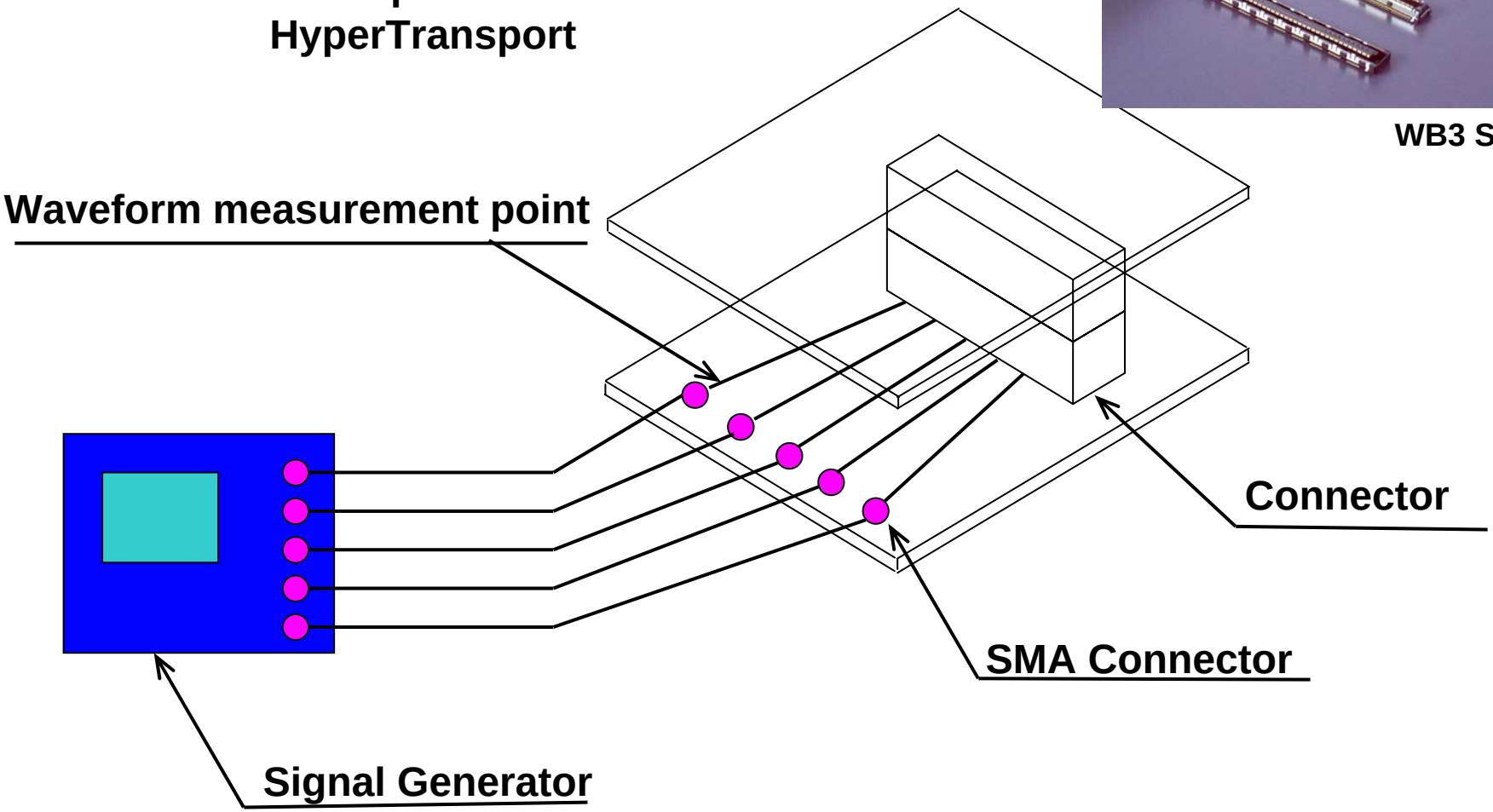


WB3 Series

**Signal**

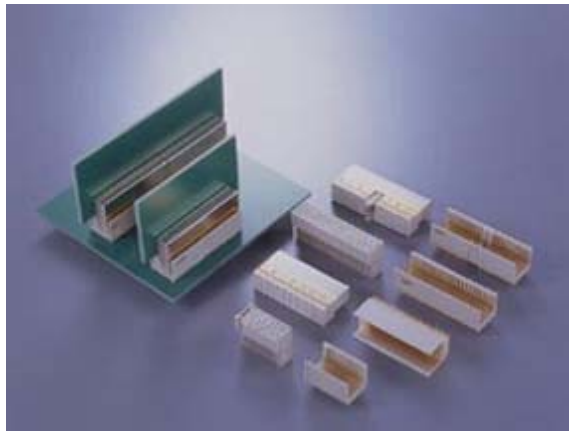
**PCI-Express**

**HyperTransport**



# SI Model (Connector- Type C, PCB, Cable)

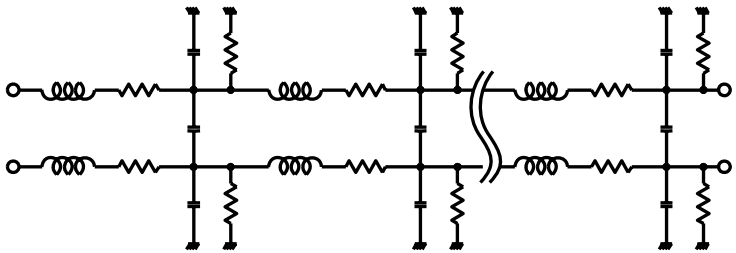
Signal
PCI-Express
HyperTransport



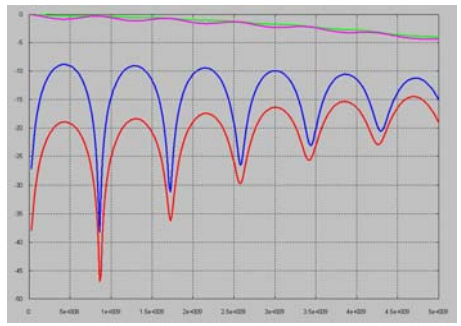
MJ04 Series

# Simulation Model

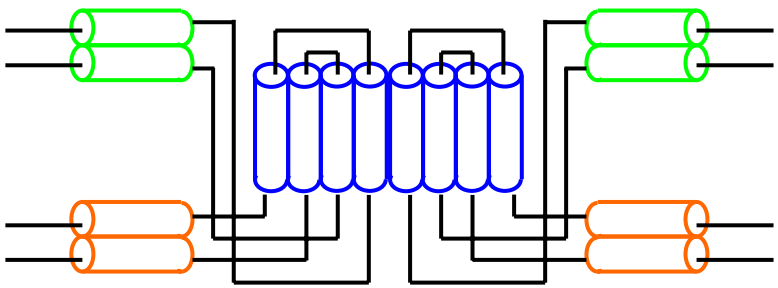
Equivalent circuit



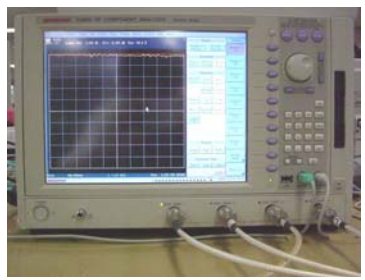
Simulation



TML

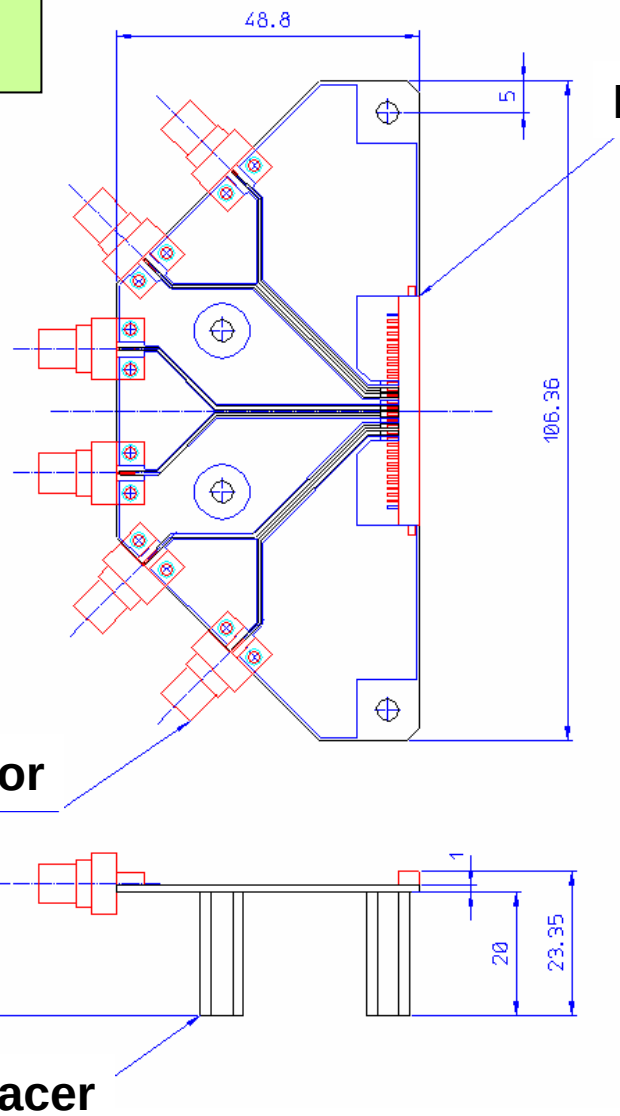


Measurement



# Evaluation Board

## Connector



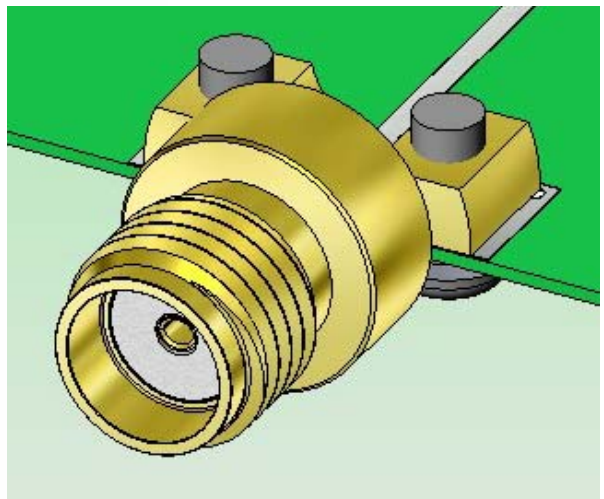

Fi-X Connector

SMA Connector

spacer

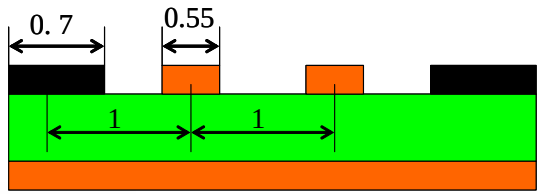
SMA Connector

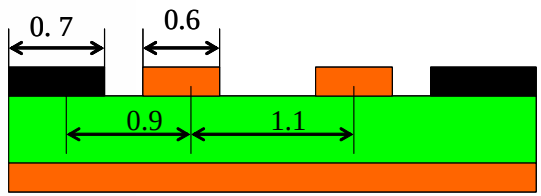
***SMAR006D00***

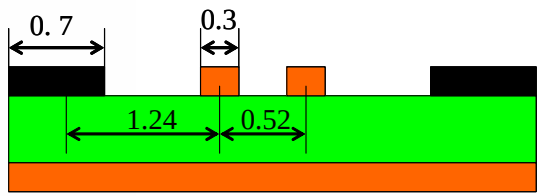


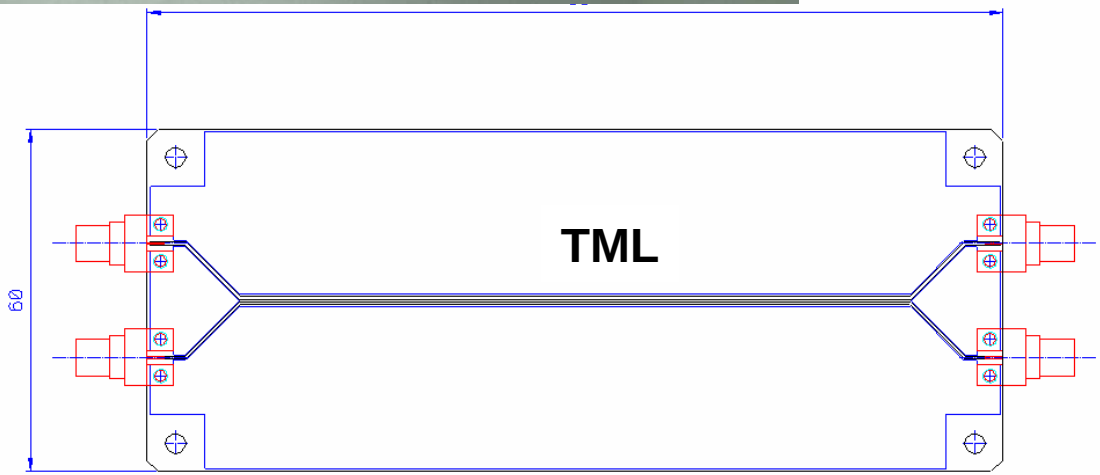
# TML


layer structure



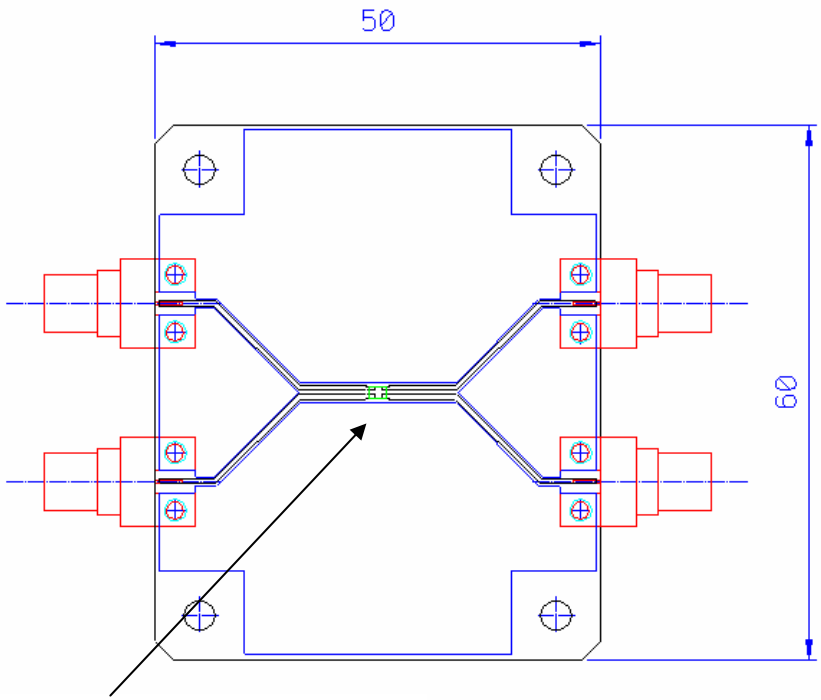



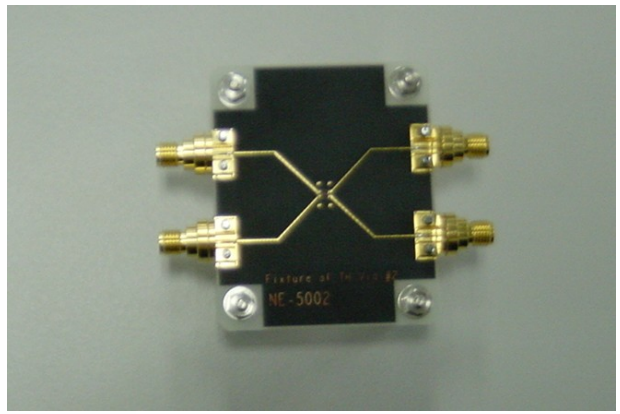




**SMA Connector**


**Spacer**

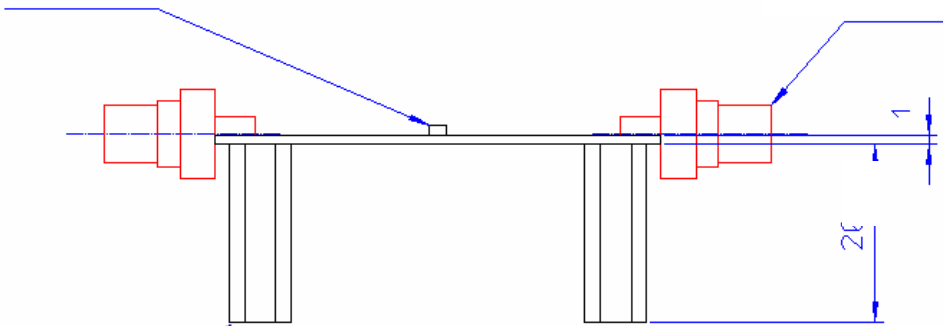
# Passive Components



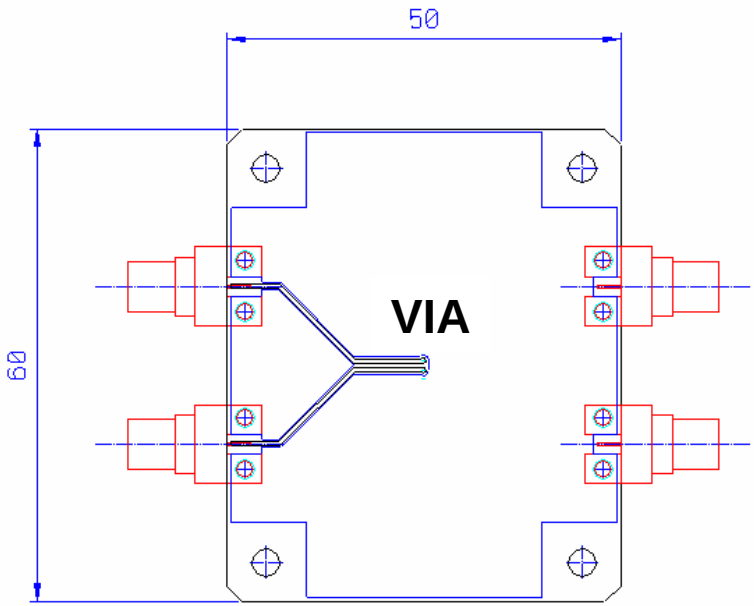
Passive Components

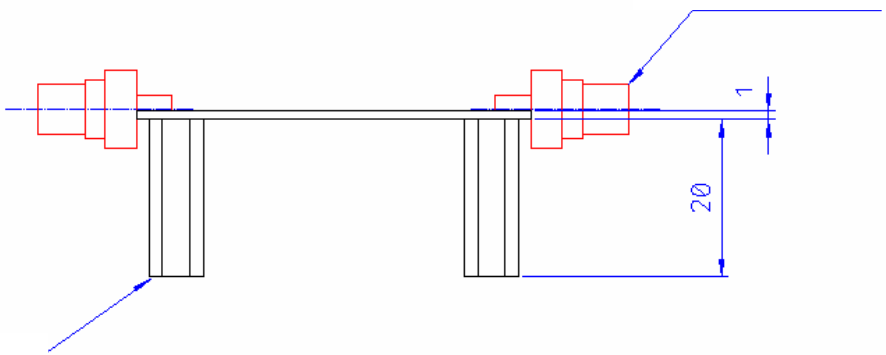
SMA Connector

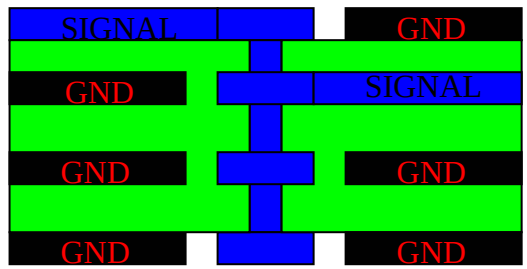



Spacer

# VIA



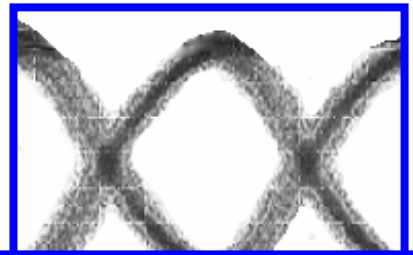



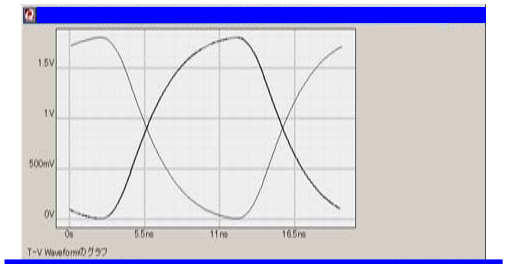
# 4. JEITA EDA-WG Progress Report

- **Study of Interconnect Model**

~ October of 2006

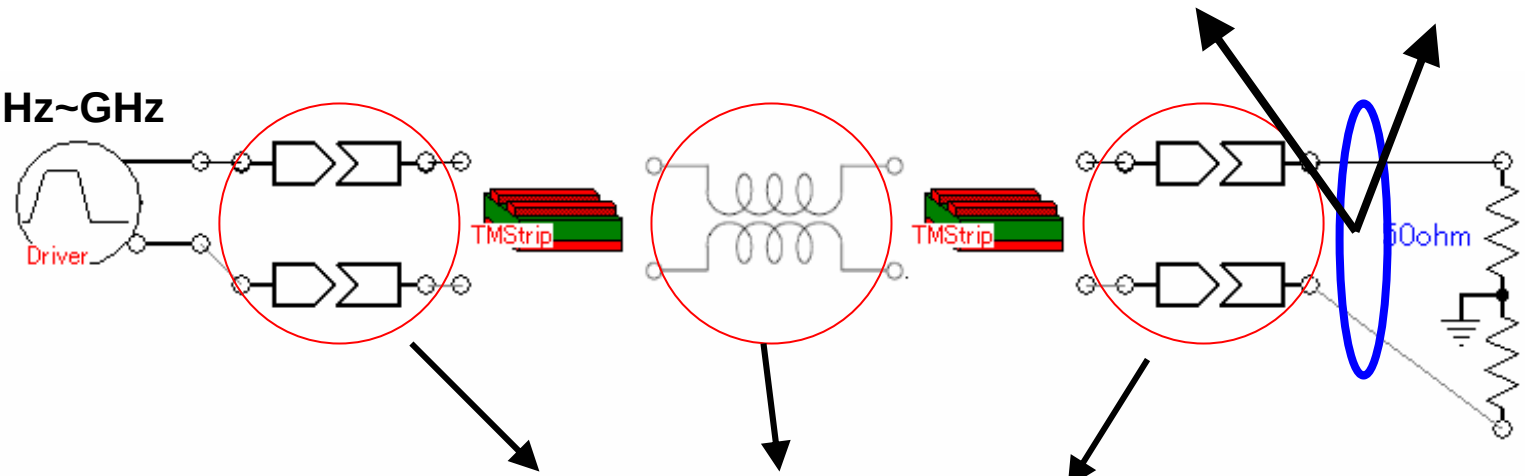
# Compare Measurement with Simulation





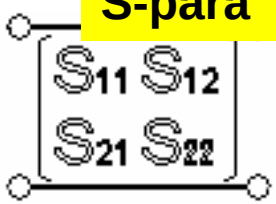
**Measurement** **Simulation**

MHz~GHz




**Model**

**S-para** **Spice** **RLGC**




Ω/H/S/F

# Study of Interconnect Model

Contents

# 0.1. Measurement equipment and simulation tools

## 0.1.1 Equipment of Measurement

Time Domain Reflectmetory (TDR)
86100C +54754A(TDR module)

Vector Network Analyzer (VNA)
N5230A PNA-L

Signal Generator (SG) with Real Time Osillscope (OSC)
81134A ,DSO81204B

## 0.1.2 Simulation tools and Venders

4 company's tool

# 1.1. Detail of Measurement

## 1.1.1 Measurement of Eye-diagram

Signal generator (SG) and real time oscilloscope (OSC) were used to compare measurement with simulation of Eye-Diagram.

SG was used to inject differential signal which were pseudo random bit sequence. (PRBS) PRBS pattern were 256bits.

OSC was used to record transient waveform.

DUT of three types were provided, which simulate PCBs of digital consumer electronics. One of them contains only filter and connector, the others contain filter, connector and also through hole via and slit.

Signal Generator
PRBS 2e8-1
Tr,Tf=96ps
Differential Signal
0.45-0.8v

Device Under Test (DUT)

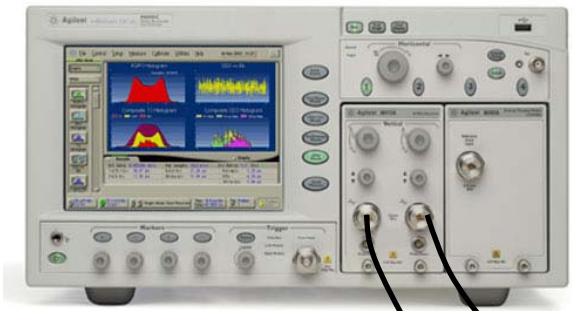
Oscillscope
BW 12GHz
40G sampling/s

# 1.1. Detail of Measurement

## 1.1.2 Measurement of TDR

To verify characteristic Impedance of PCB, TDR was used.
The TDR injected differential step pulse and measured reflection waveform, then characteristic Impedance was calculated by the reflection waveform.

One side of DUT were left open in order to measure DUT of electric length which is propagation time to the end ports.



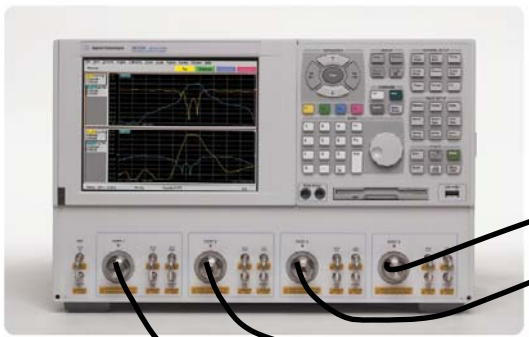
TDR OSC
TDR module
BW 18GHz
Tr 35psec

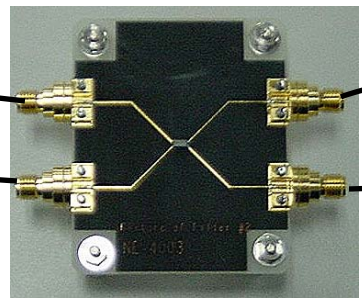
DUT


Open End
Not Terminated

## 1.1.3 Measurement of S-parameters

To verify simulation models ,VNA were used to measure S-parameters. The VNA has 4 ports, therefore it measures mixed mode S-parameters which are important parameter to investigate differential transmission line.





DUT

4 ports VNA
BW 10M-20GHz
IFBW 100k
Measured points 2000
Averaging 10 times

# 1.2. Detail of simulation
## EDA models

1. EDA models were provided by component manufacturer.

2. PCB models were extracted from CAD data by simulation tools.
   PCB manufacturer does not provide EDA model.
   They provide only layer structure, wire width, space between wires and dielectric constant.

3. EDA models were S-parameters or Equivalent Circuits.

# 1.2. Detail of simulation
## Simulation Items

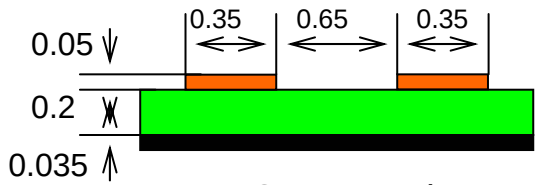
1. Eye-Diagram
   Only EDA model provided by the manufacturer.
   To verify Whether the measurement agrees with the simulation
   Measured S-parameters
   To verify whether each simulator accept S-parameters.

2. TDR Waveform
   Only wire of PCB
   To verify whether EDA model of PCB which is extracted by each simulator is correct.

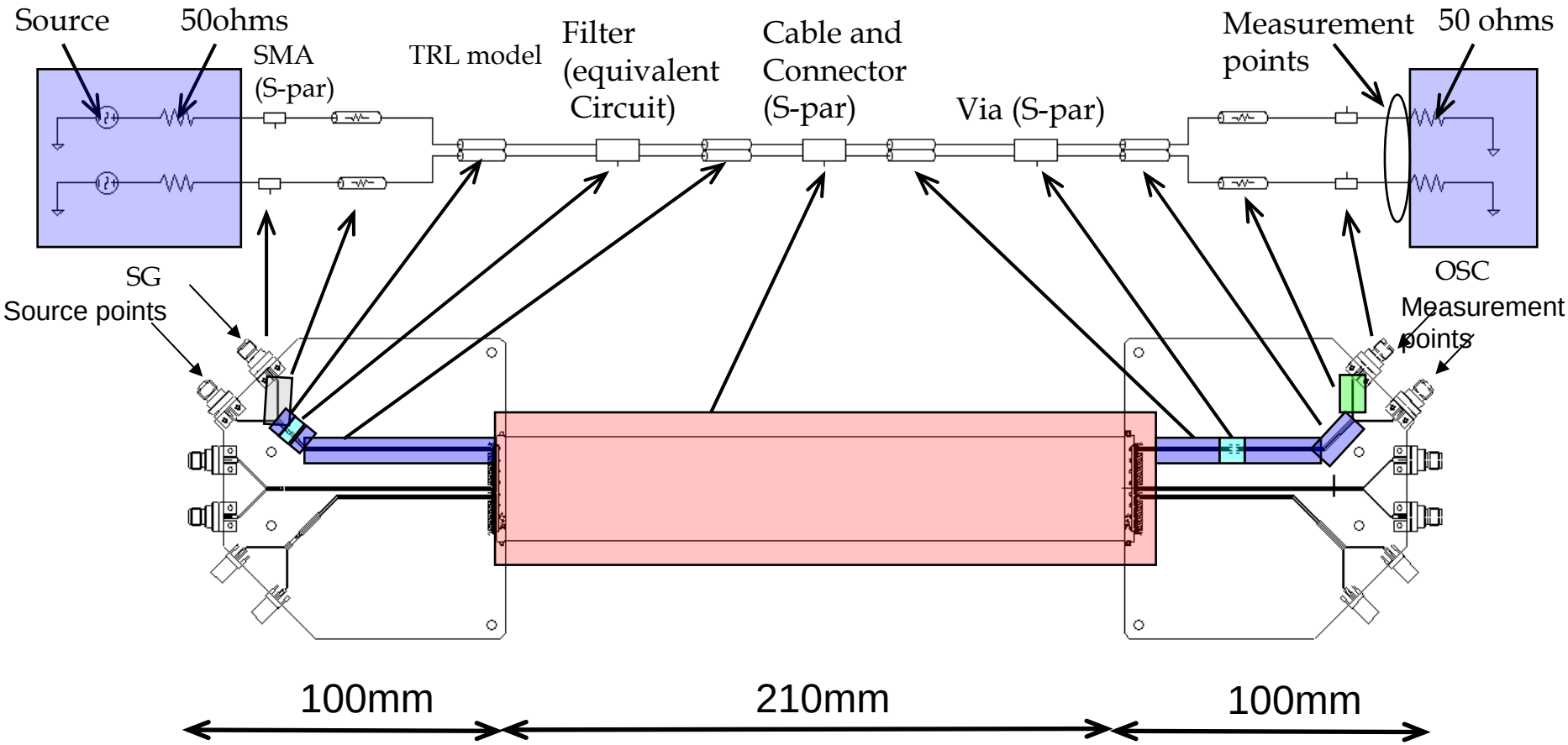
3. S-parameters
   Each EDA models
   To verify accuracy of each EDA models

# 1.2. Detail of simulation

## #68 DUT and Simulation model

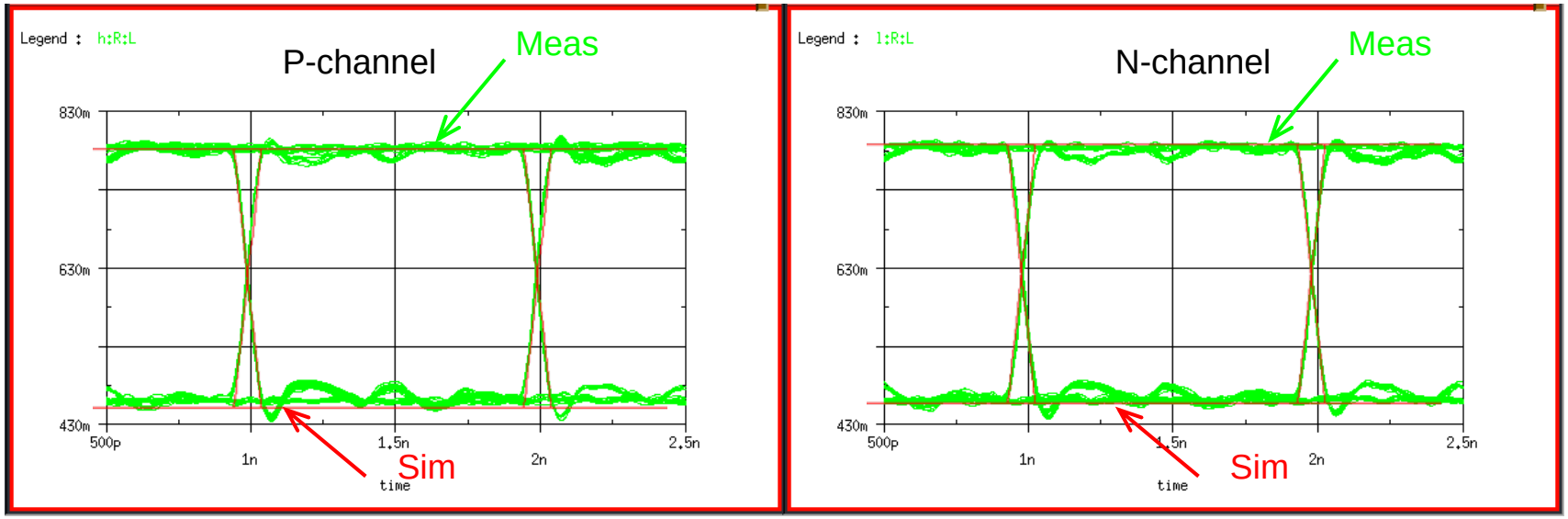



Cross section

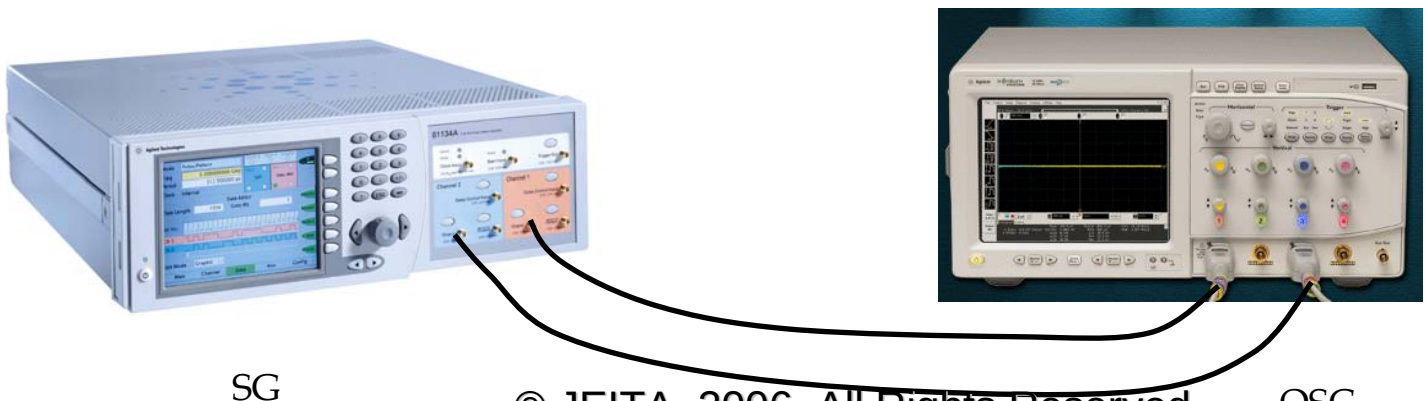


# 2.1 Comparison between Measurement and Simulation

## Eye diagram of Input conditions




To make source signal of simulation, OSC was directly connected with SG using short cable. Cable length was about 20cm.

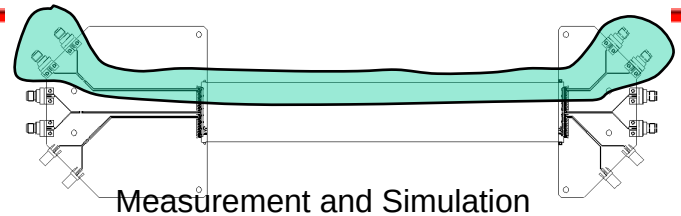


SG

OSC

# 2.2 Comparison between Measurement and Simulation

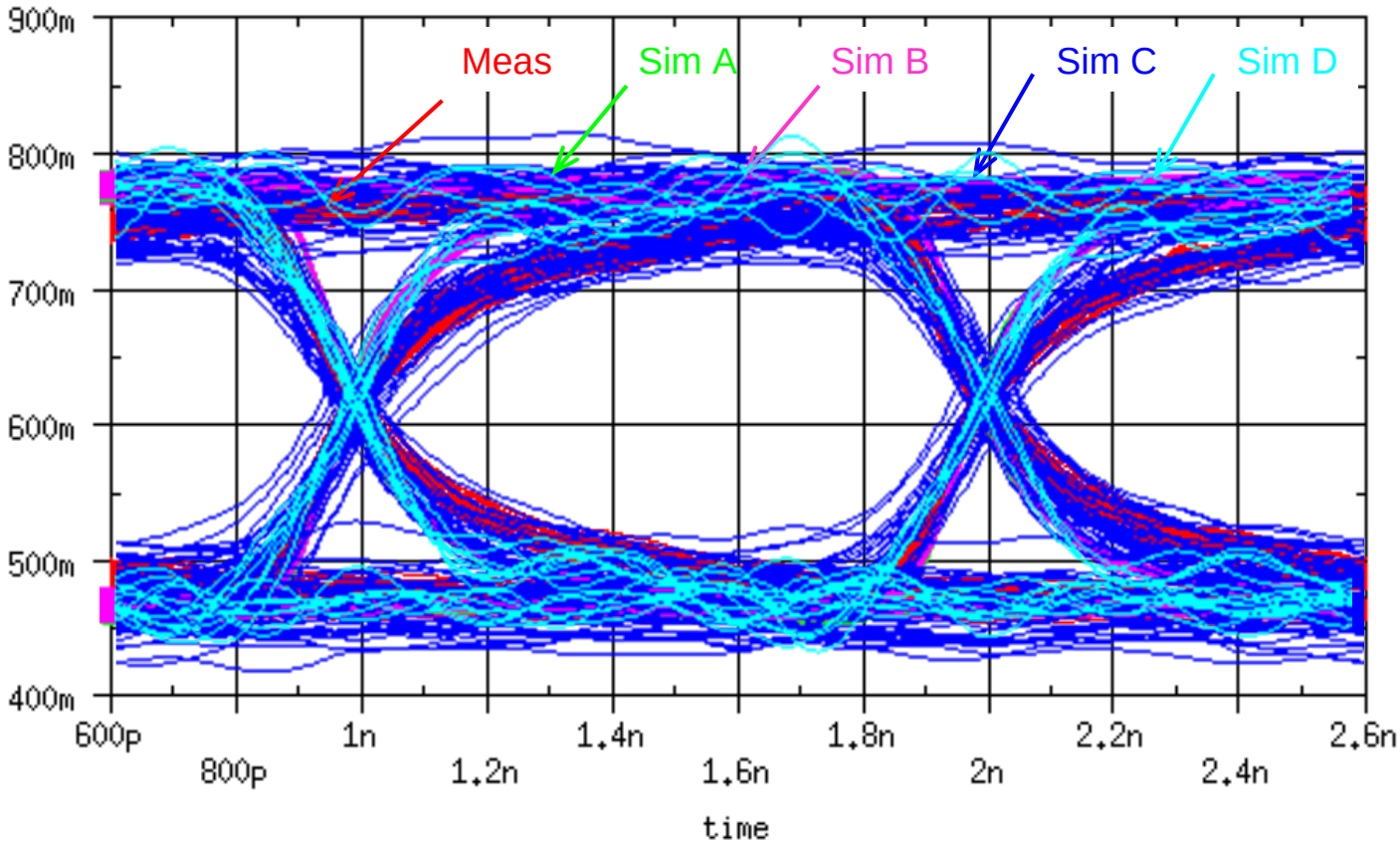
## #53 Eye Diagram of Measurement and Simulation



Measurement and Simulation

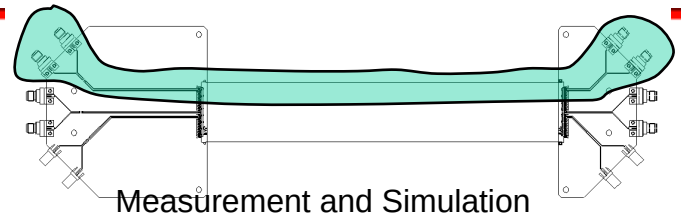
Legend : 53h:R:L

P-channel



# 2.3 Comparison between Measurement and Simulation

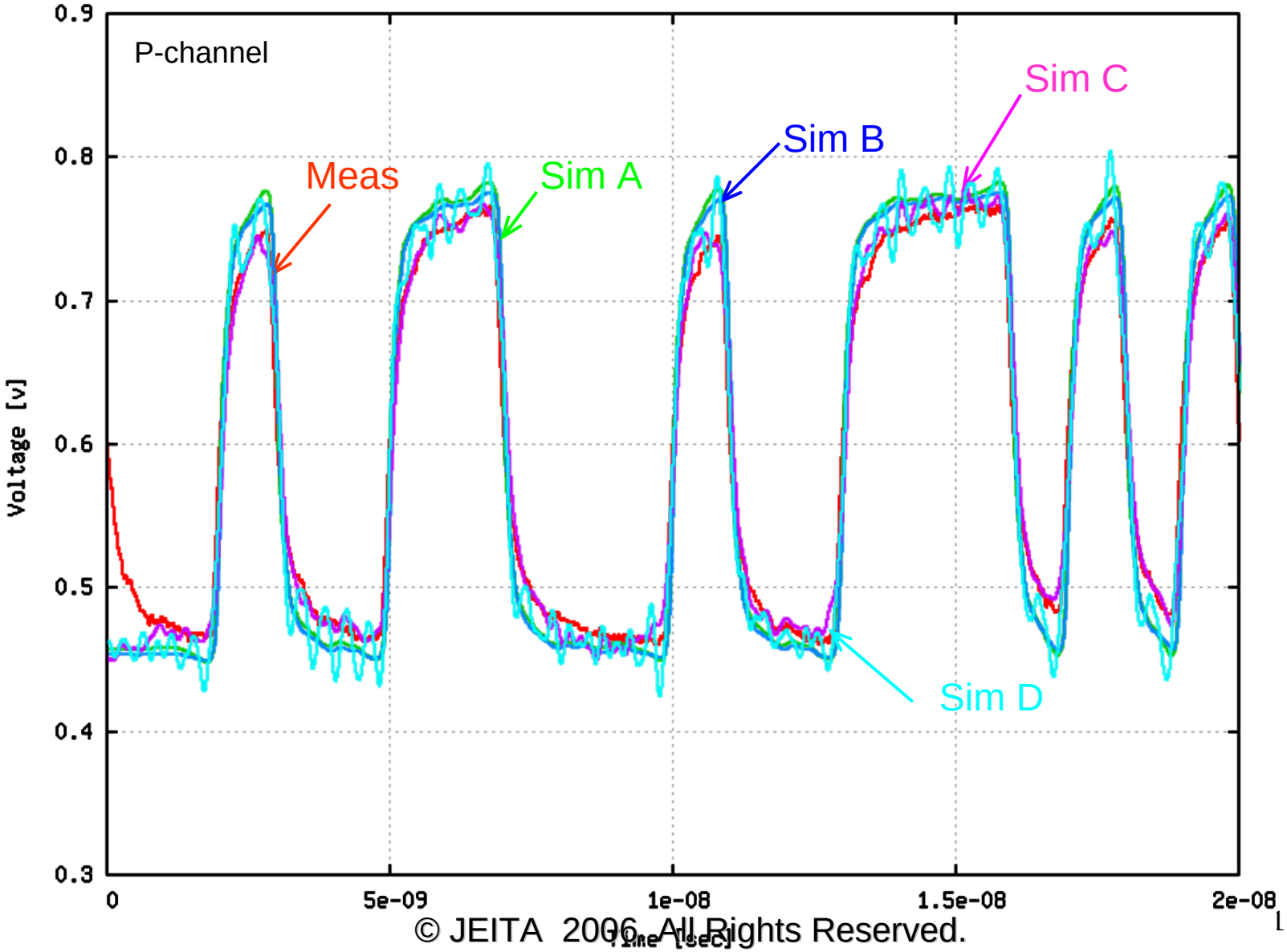
## #53 Eye Diagram of Measurement and Simulation



Measurement and Simulation

# 2.4 Comparison between Measurement and Simulation

## #53 Discrete Waveform of Measurement and Simulation

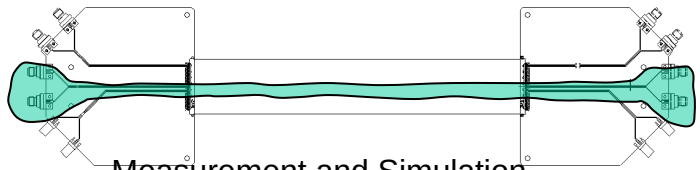


# 2.5 Comparison between Measurement and Simulation

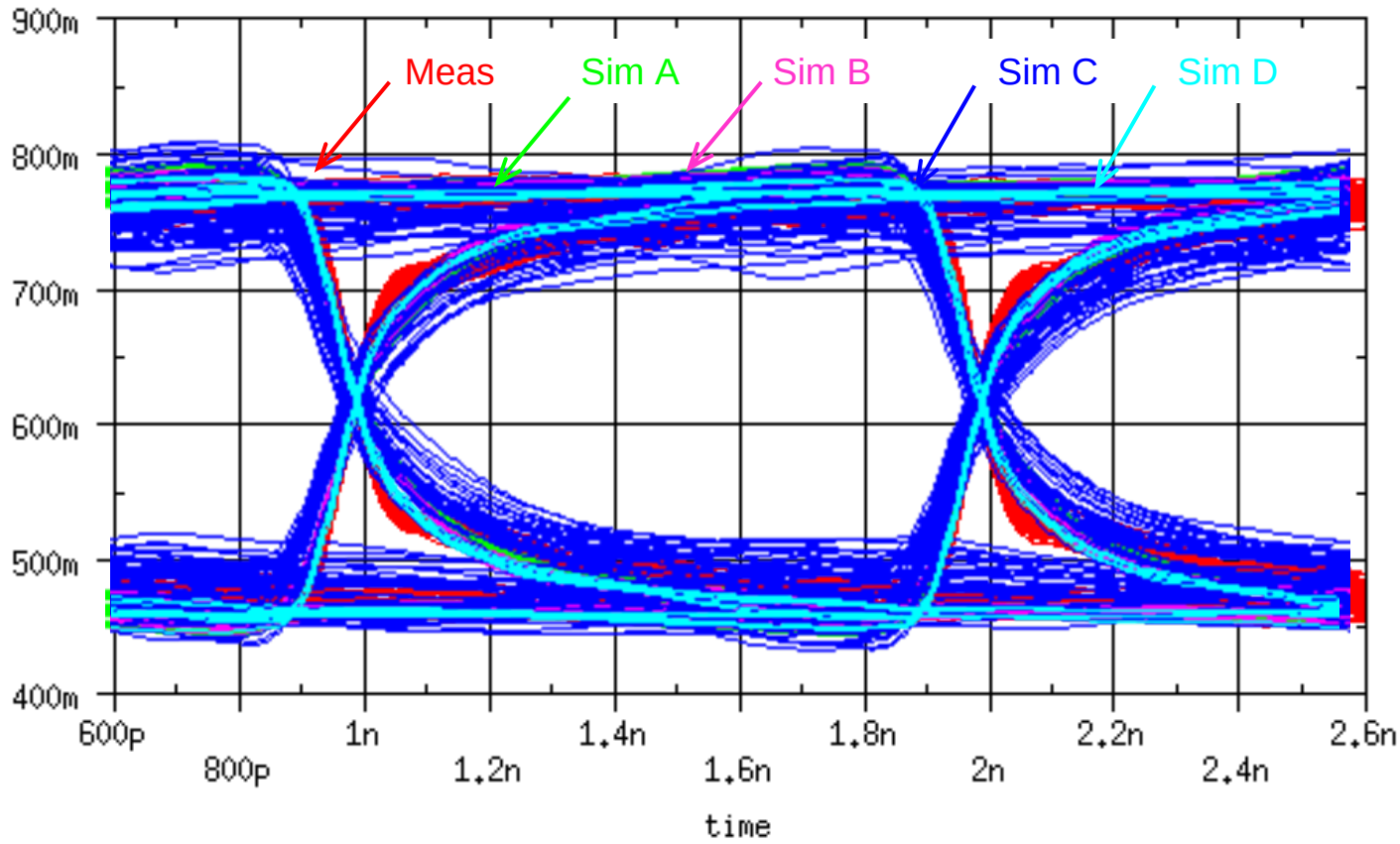
## #67 Eye Diagram of Measurement and Simulation

Legend : 67h:R:L

P-channel

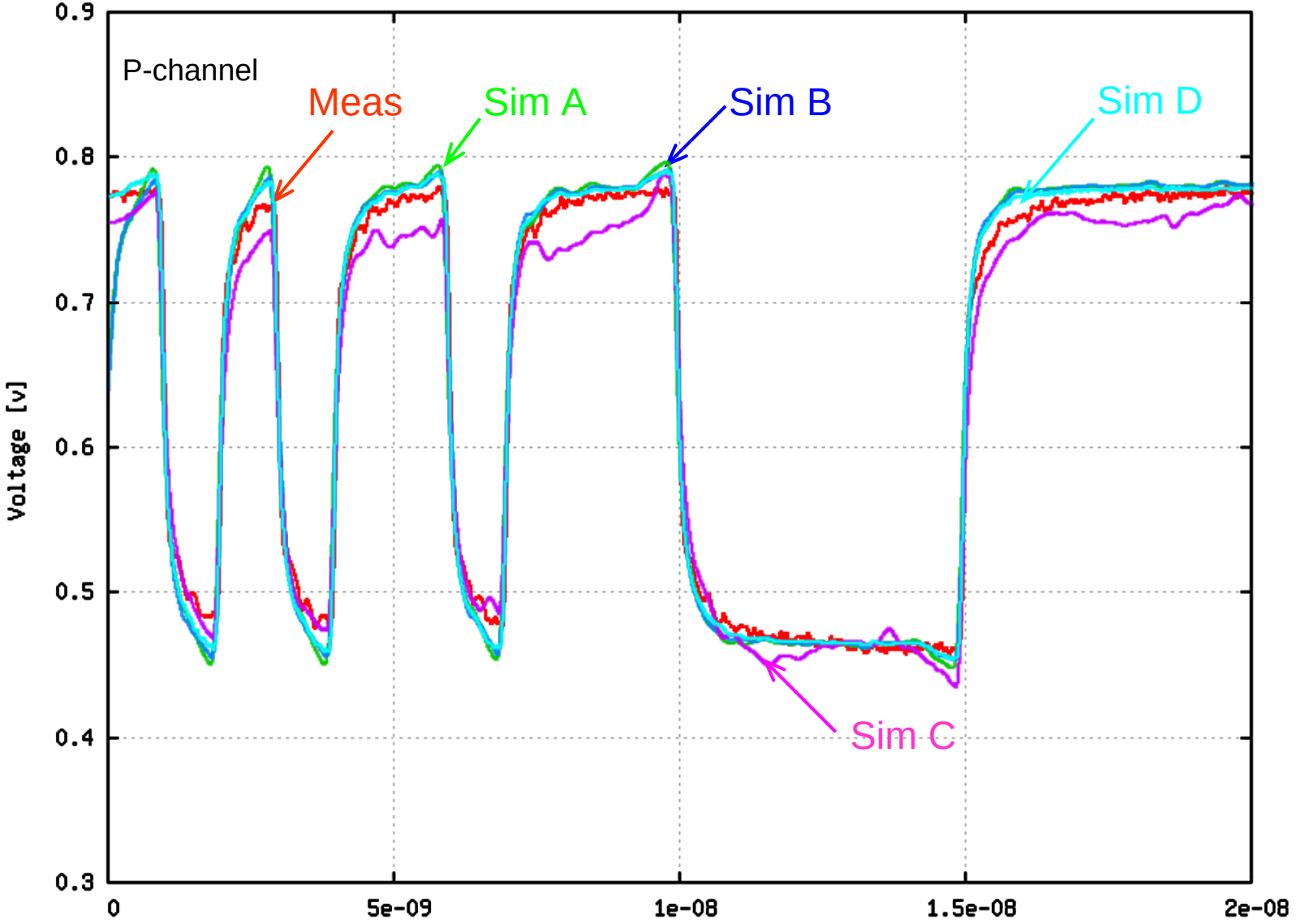


Measurement and Simulation



# 2.6 Comparison between Measurement and Simulation

## #67 Discrete Waveform of Measurement and Simulation

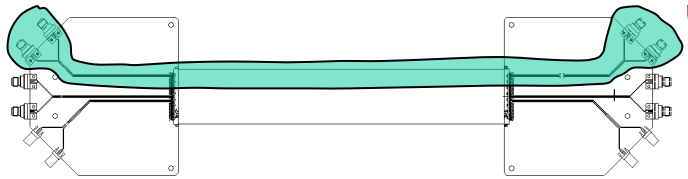


# 2.7 Comparison between Measurement and Simulation

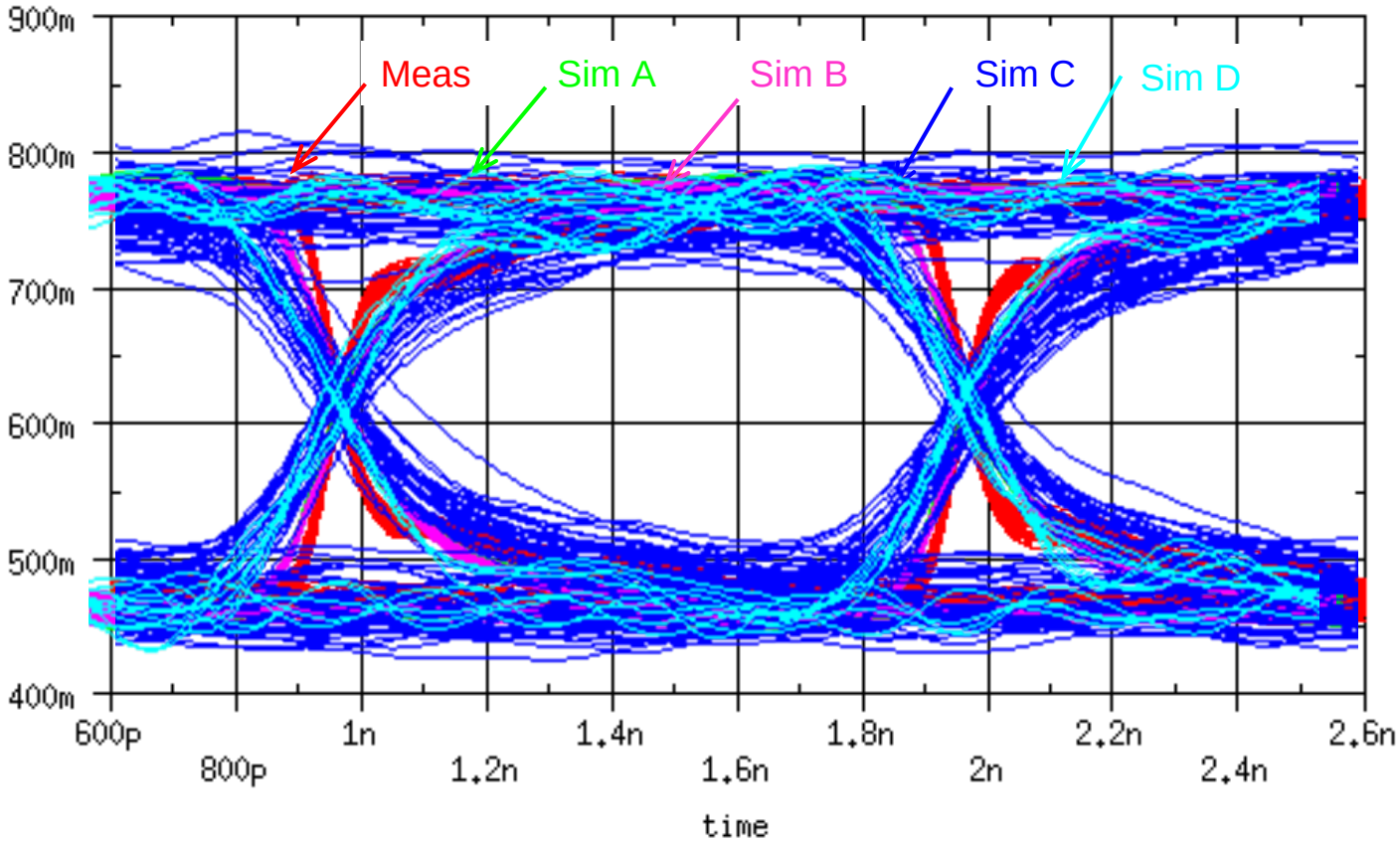
## #68 Eye Diagram of Measurement and Simulation

Legend : 68h:R:L

P-channel

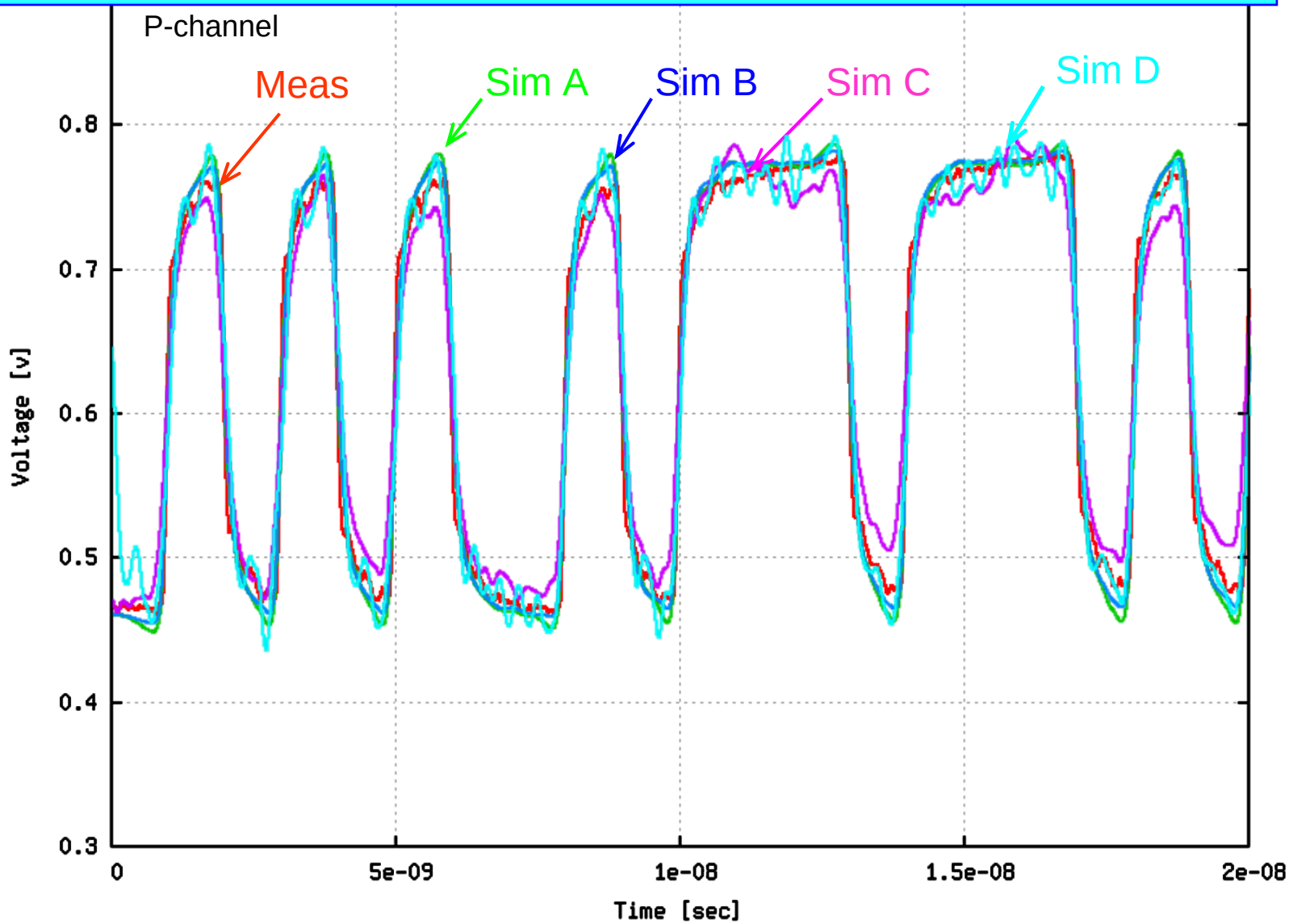


Measurement and Simulation



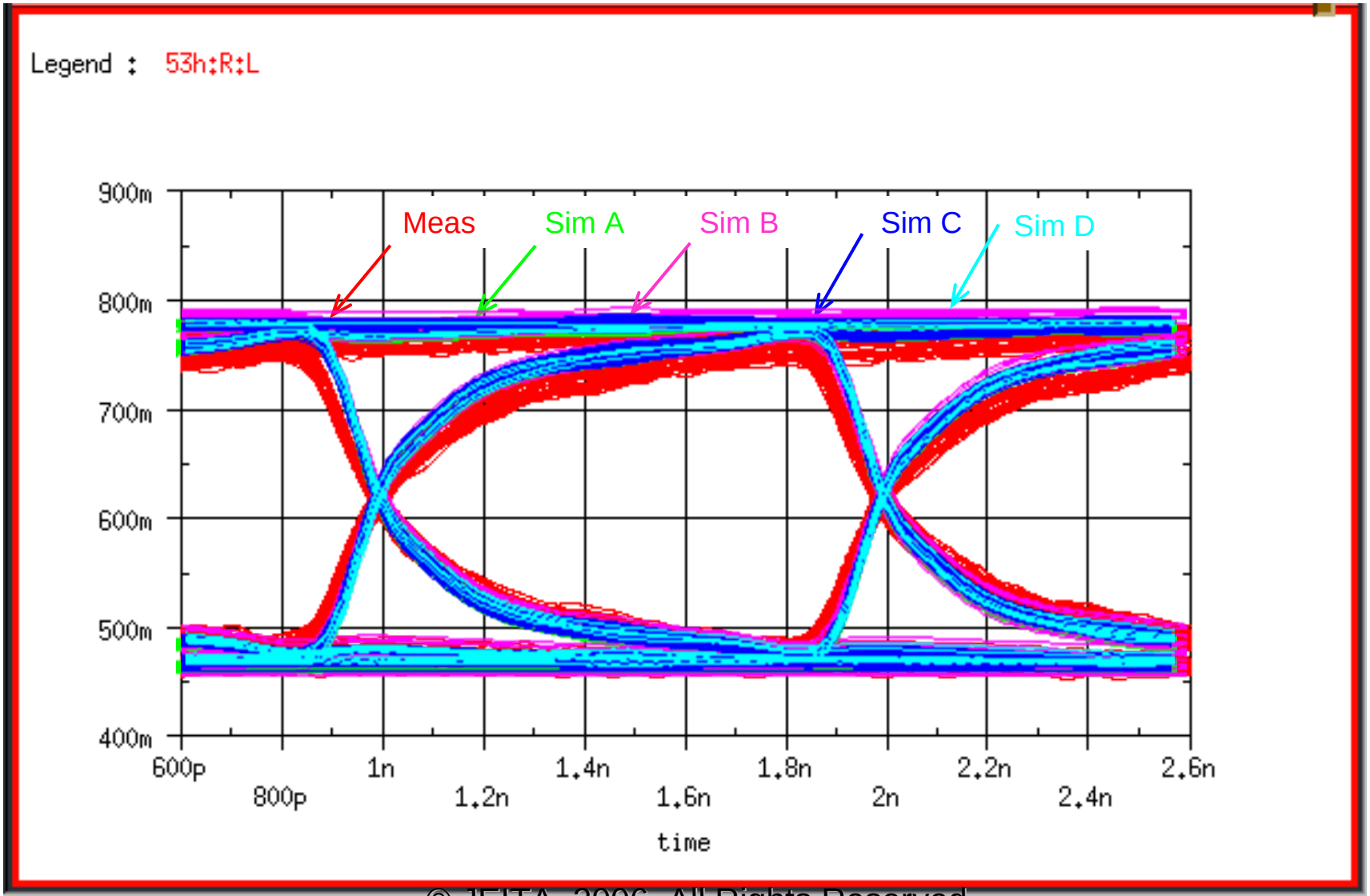
# 2.8 Comparison between Measurement and Simulation

## #68 Discrete Waveform of Measurement and Simulation



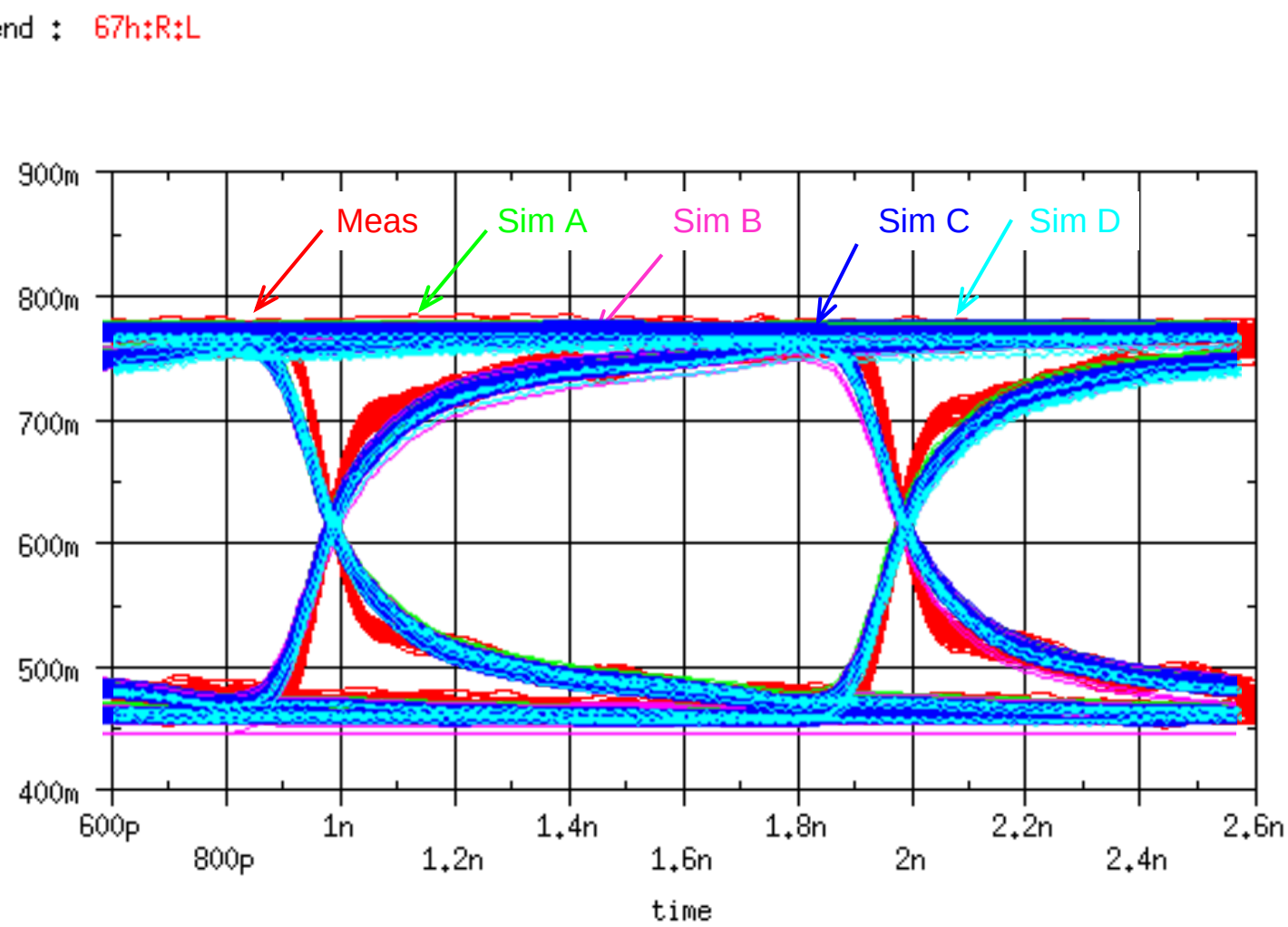
# 3.1 Simulation for Measured EDA models

## #53 Eye Diagram of Measurement and Simulation using measured S-parameters



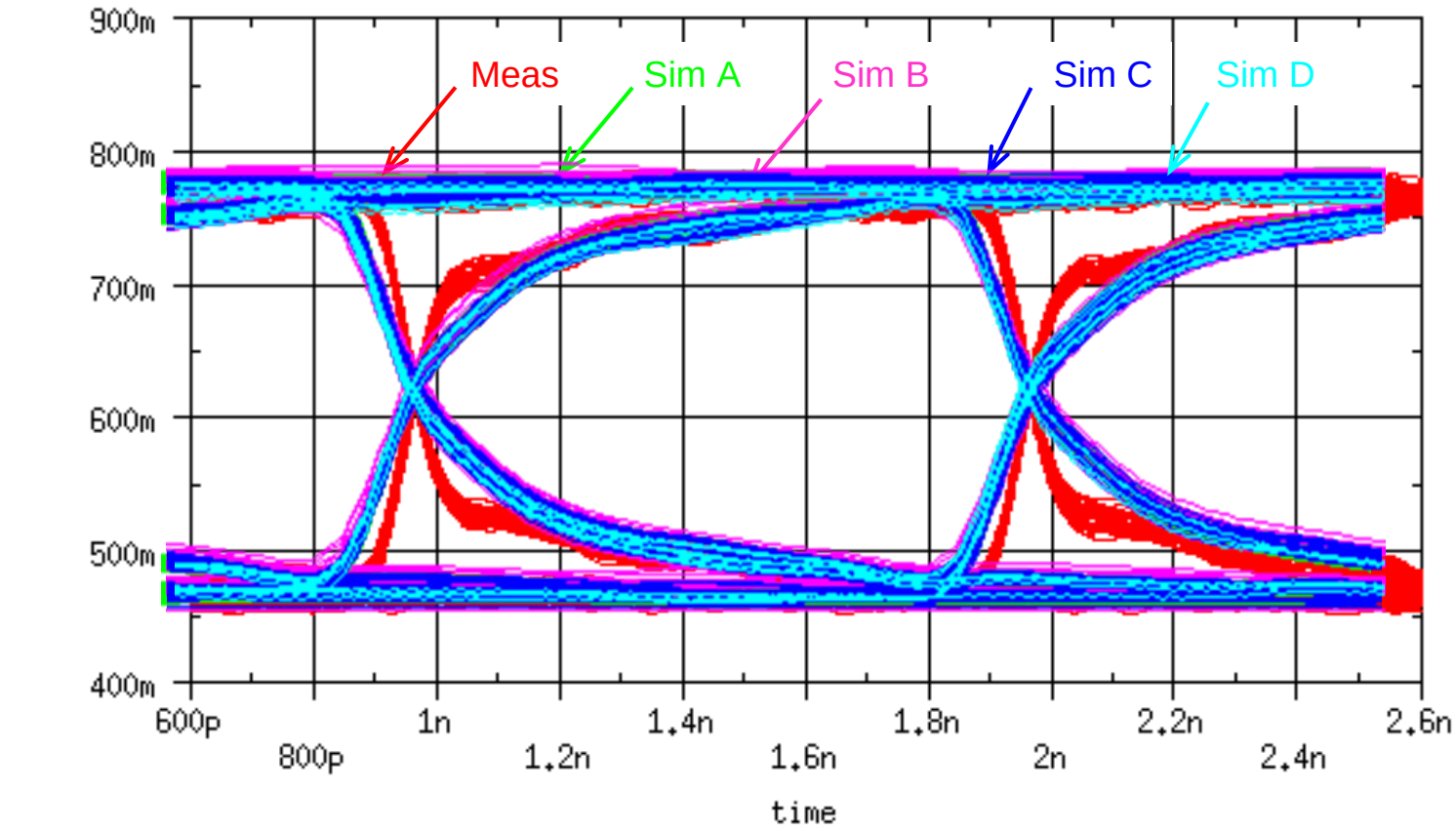
# 3.2 Simulations for Measured EDA models

## #67 Eye Diagram of Measurement and Simulation using measured S-parameters



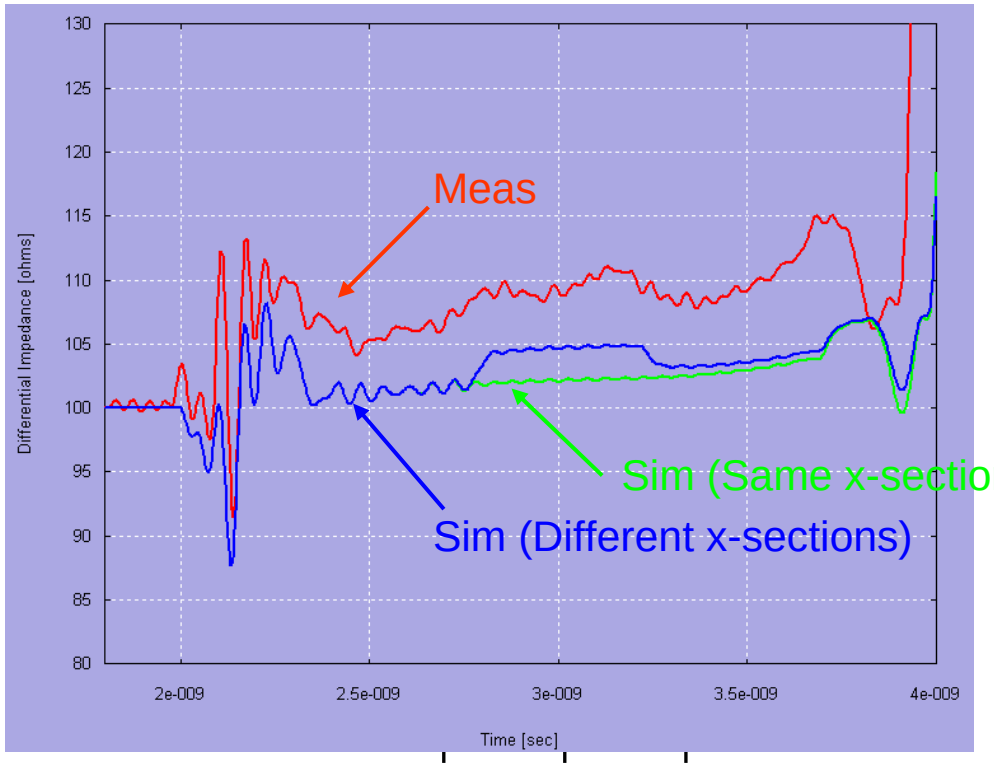
# 3.3 Simulations for Measured EDA models

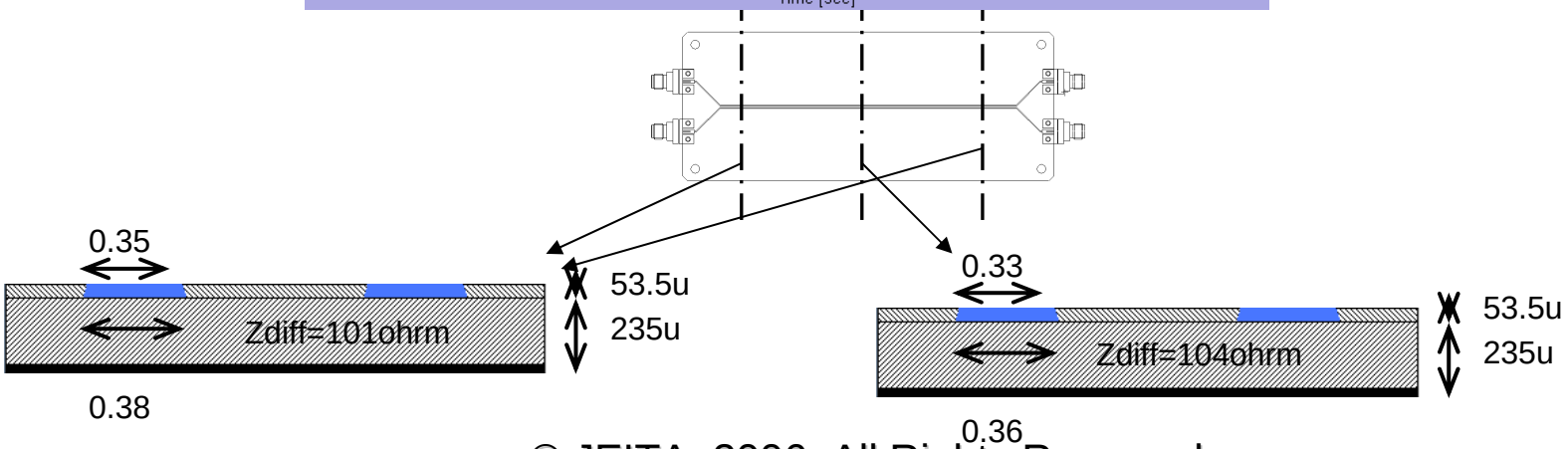
## #68 Eye Diagram of Measurement and Simulation using measured S-parameters



# 4. Accuracy of EDA models

## 4.1 Measured and Simulated TDR waveform

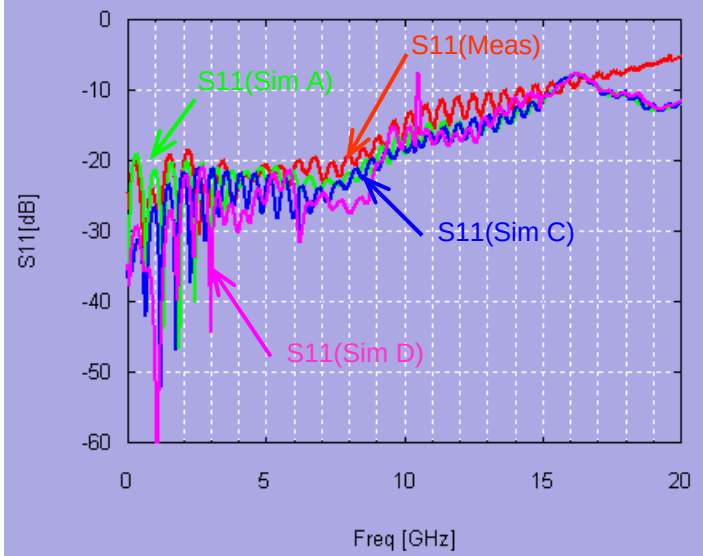


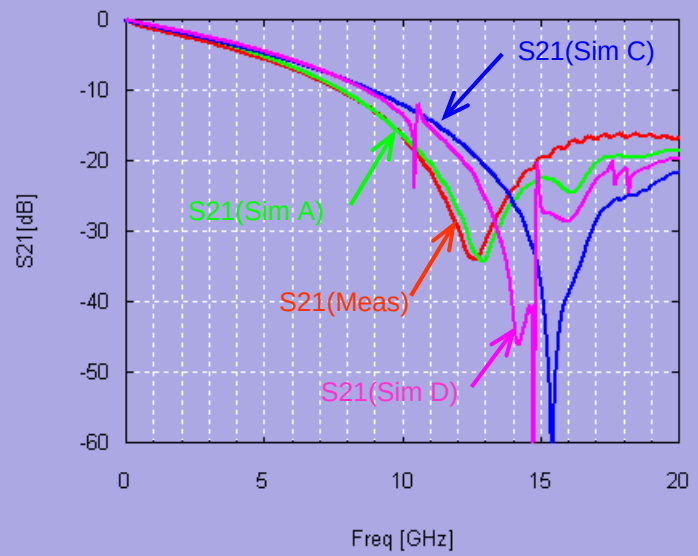



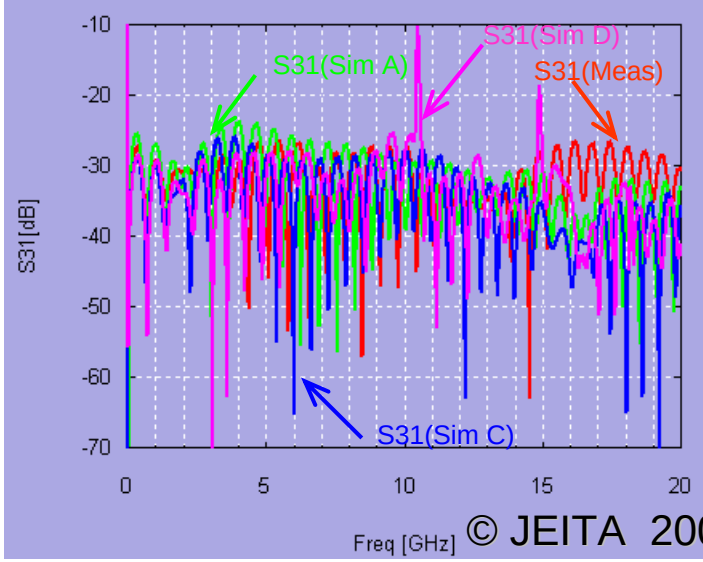
# 4. Accuracy of EDA models

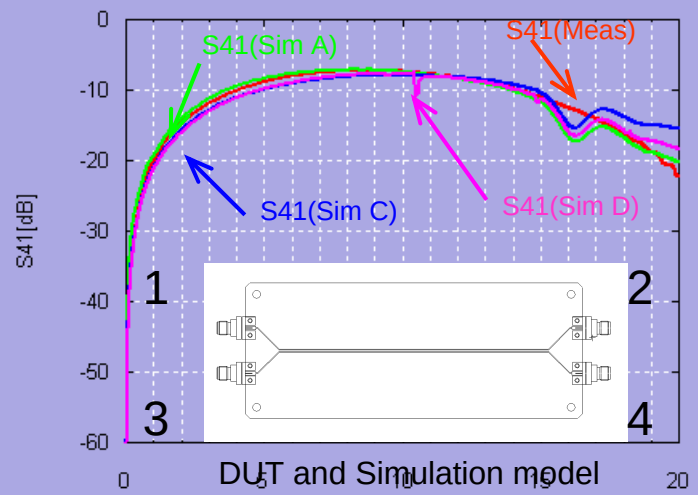
## 4.2.1 Measured and Simulated S-parameters

### Differential MSL with Solid GND Plane



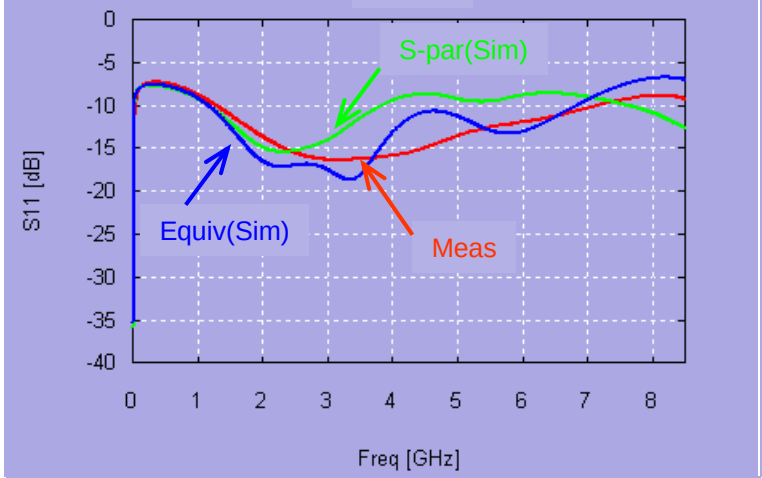



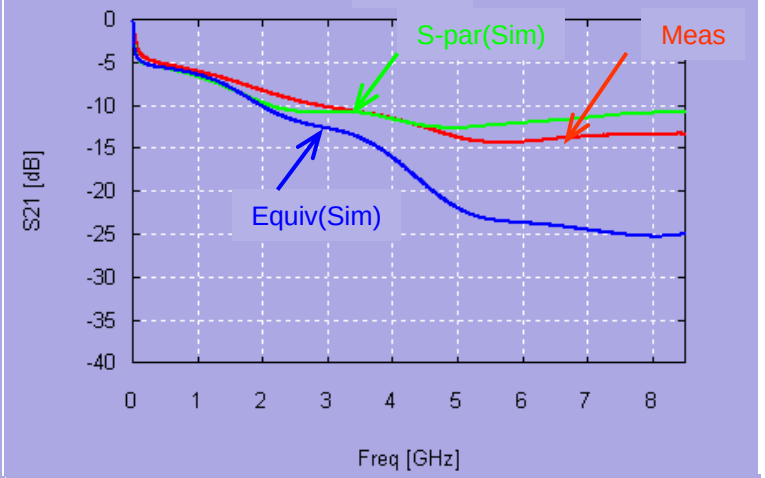

DUT and Simulation model

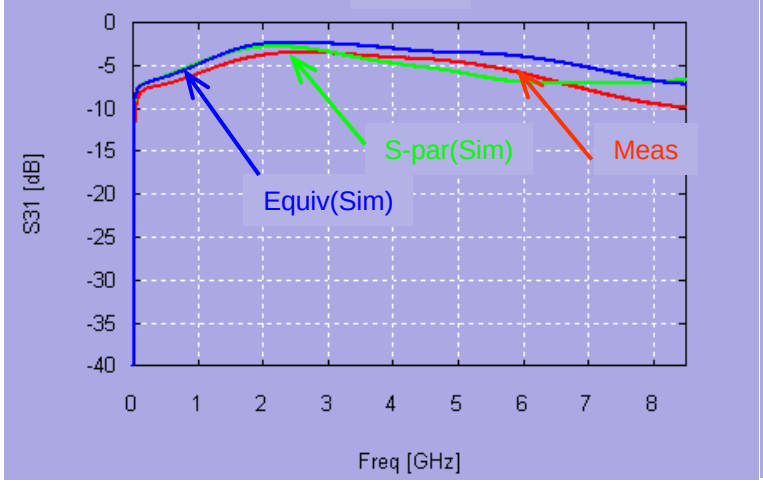
# 4. Accuracy of EDA models

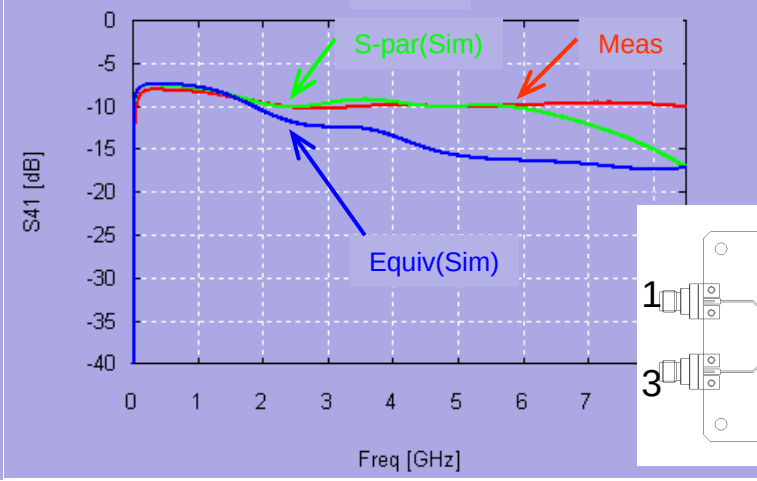
## 4.2.2 Measured and Simulated S-parameters

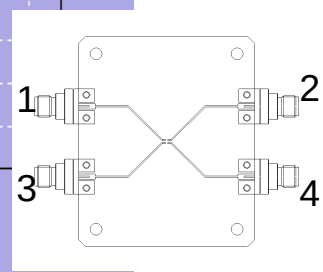
## Filter A



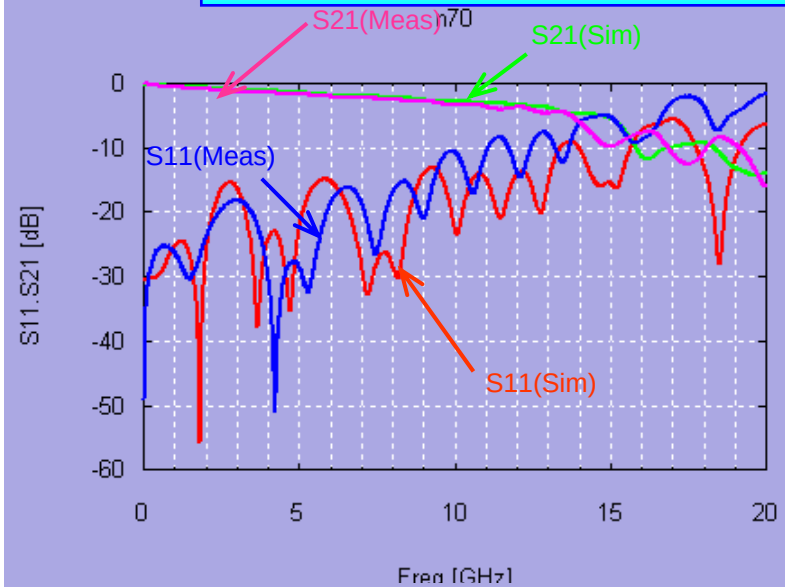



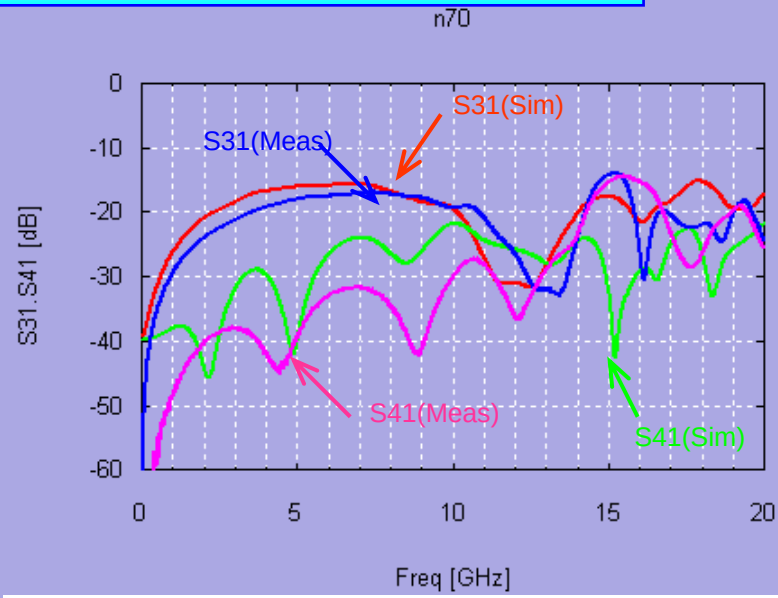



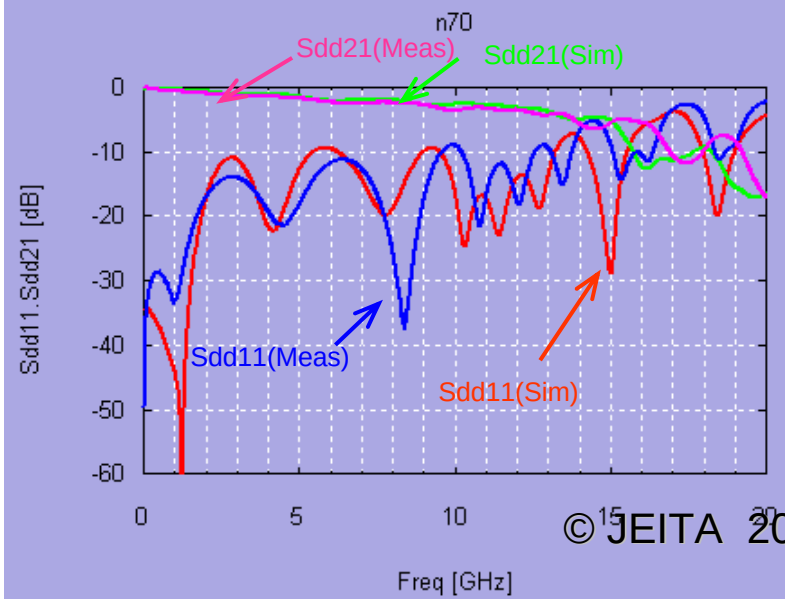
# 4. Accuracy of EDA models

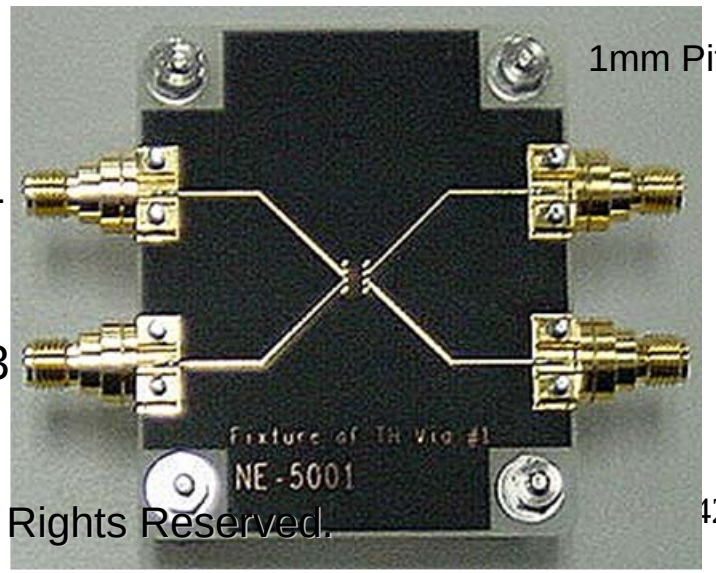
## 4.2.3 Measured and Simulated Mixed mode S-parameters

### Via 1mm pitch



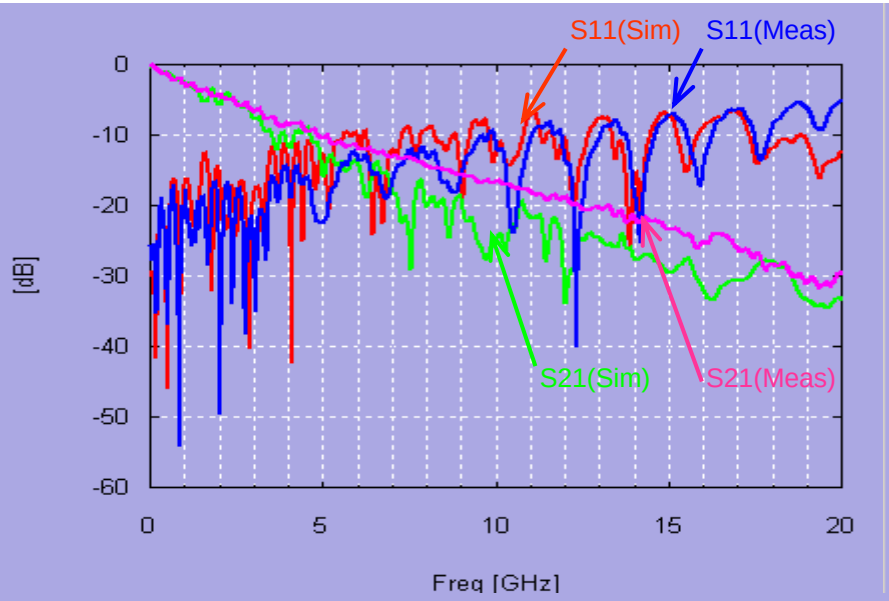



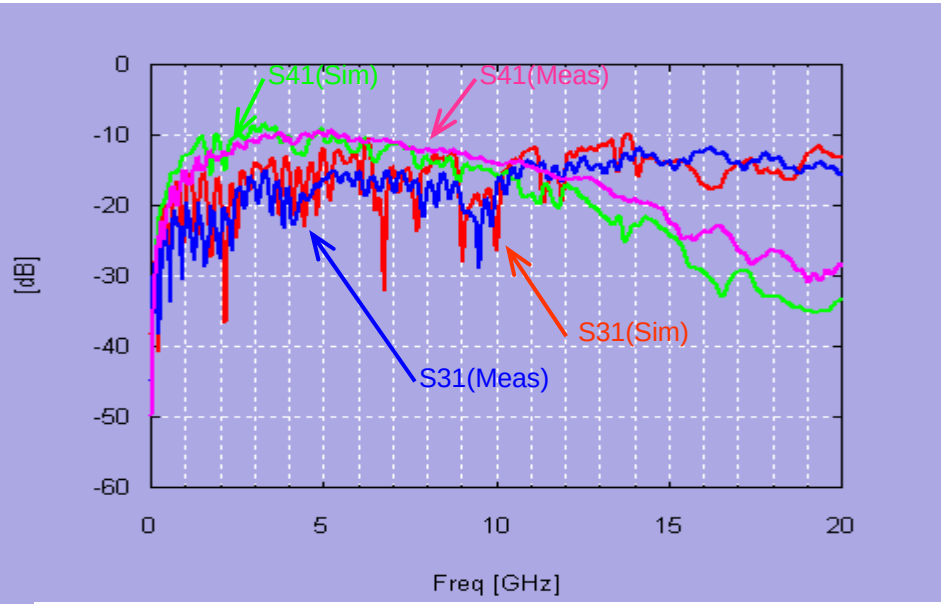



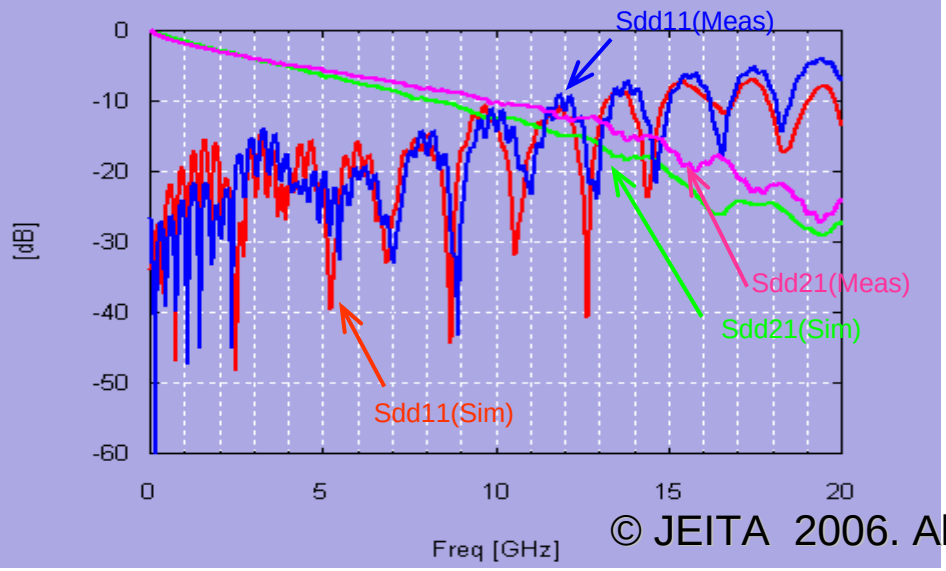



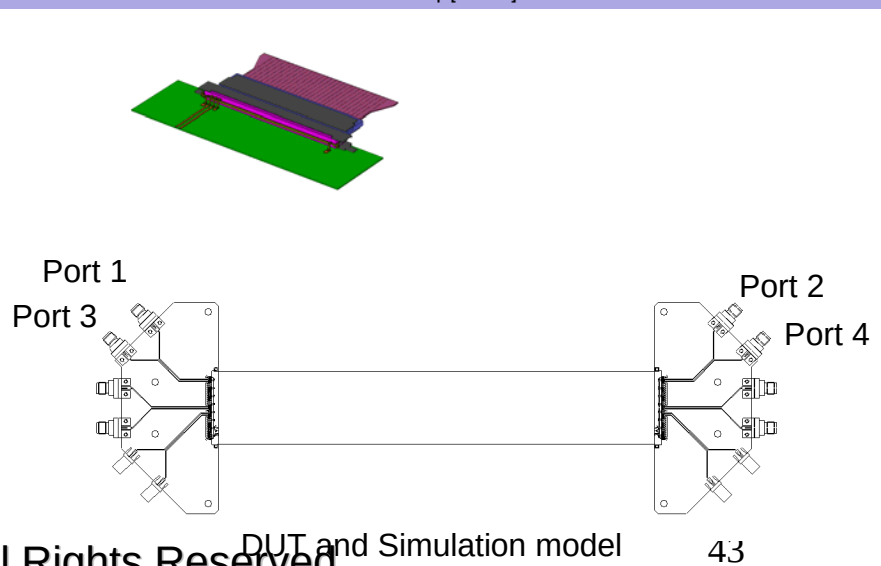
# 4. Accuracy of EDA models

## 4.2.4 Edge of Connector Cable




DUT and Simulation model

# 5. Conclusion

1. Measurement and simulation of Interconnect model were done.

2. Simulation used by EDA models whom component manufacturer provides and measurement are nearly agreed.

3.Each simulator accepts S-parameters and directly simulate them.

4.It is necessary to note that a design value and an actual value might be different when EDA model of PCB is made.

## Gratitude to cooperation in measurement and simulation

| | |
|---|---|
| Mr. Takeshi Watanabe | NEC Electronics |
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| Mr. Shigeharu Shimada | CMK |
| Mr. Seiji Hayashi | CANON |
| Mr. Yogi Yamashita | Agilent Technologies |
| Mr. Yukio Masuko | Cadence Design Systems |
| Mr. Hirotsugu Ueno | Cadence Design Systems |
| Mr. Kazuhiko Kusunoki | CYBNET |
| Mr. Masatoshi Kobayashi | CYBNET |
| Mr. Nobuhiko Kawai | Murata Manufacturing |
| Mr. Jun-ichi Wakasa | TDK |
| Mr. Yasumasa Kondo | Toshiba |
| Mr. Testuo Iwaki | Sharpe |

**We hope to discuss case study of IBIS with you periodically**

**Thank you for all the help EIA/IBIS Committee!**

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