System-Level Timing Closure Using IBIS Models

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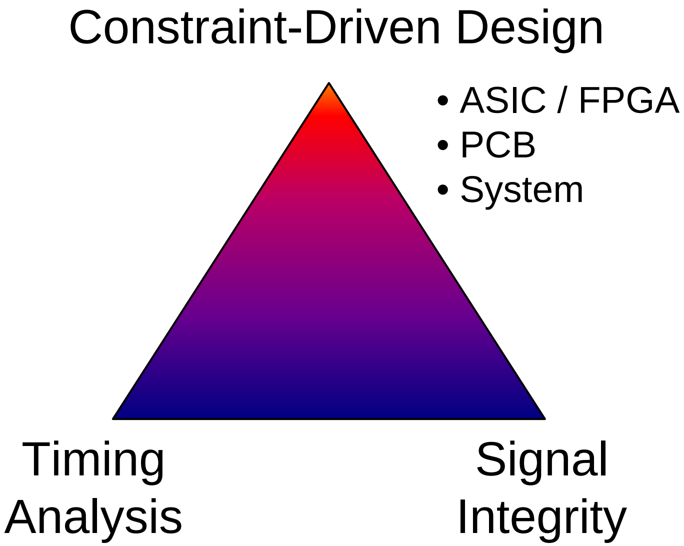
Asian IBIS Summit

Agenda

- High Speed System Design
- Establishing timing model
  - Derivation of timing equations
  - Idealized timing analysis
  - The role of signal integrity
  - Reconciling signal integrity with timing
- Pre-route exploration
- Driving physical design
- Post-route validation
- Design analysis reuse
- Case study: DDR2 memory

High Speed System Design … Not Just "Signal Integrity"



Constraint-Driven Design

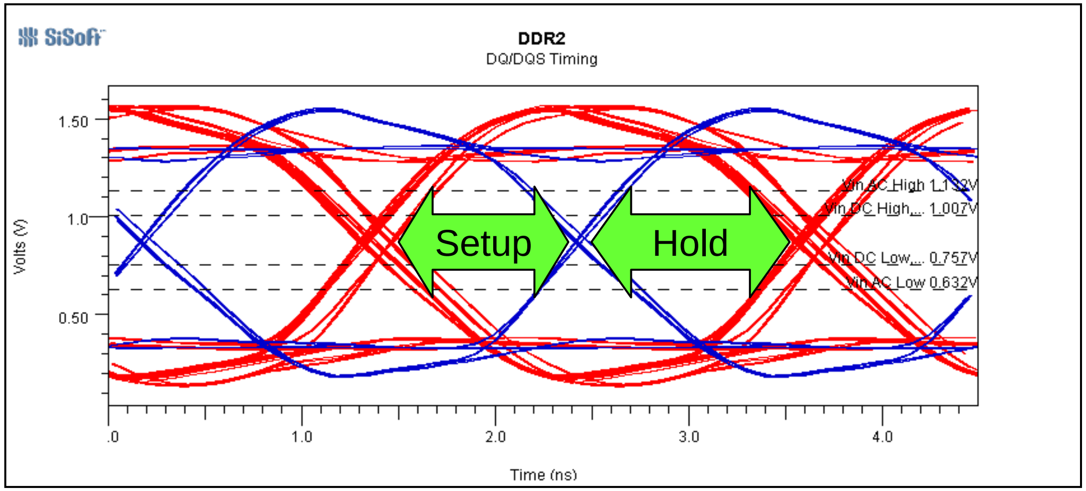
- ASIC / FPGA
- PCB
- System

Timing Analysis

Signal Integrity

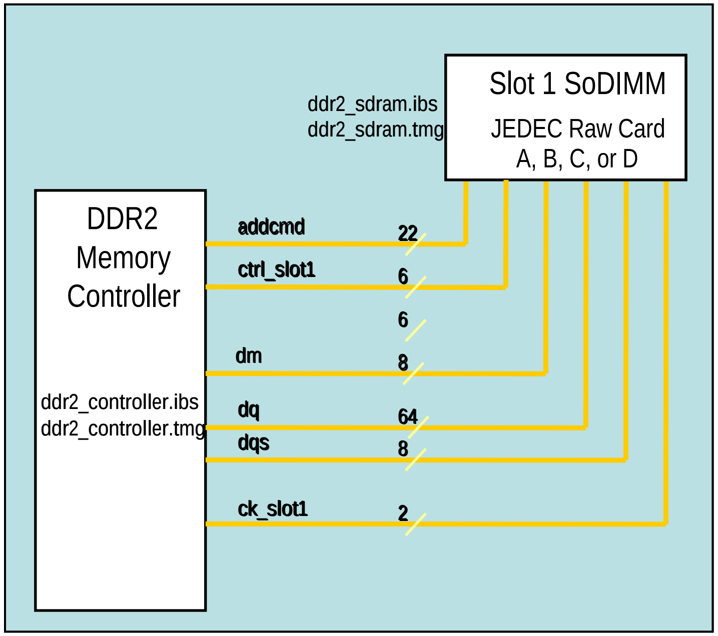
- High Speed Design involves multiple disciplines
- Changes in any area drive changes in others
- Mastery of modeling details & process flow is essential for success

System Level Timing Closure



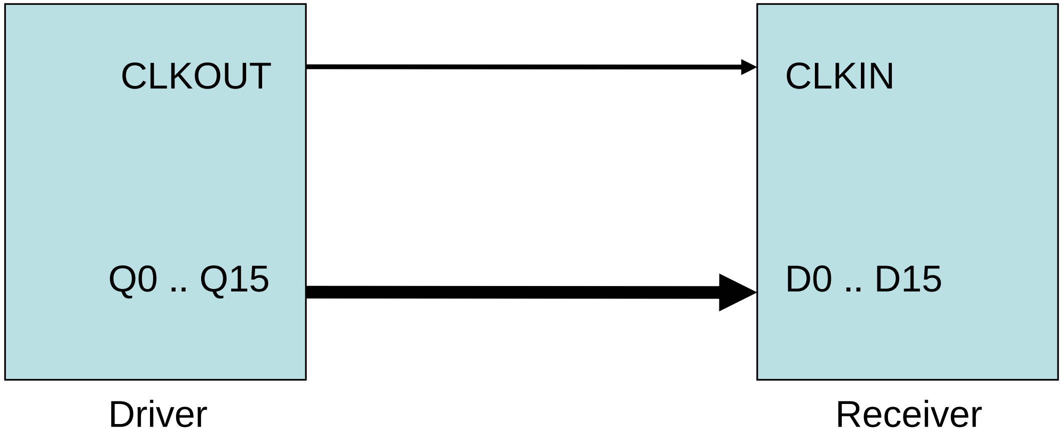
- Successful high speed design requires a rigorous methodology for ensuring positive design margin across all combinations of:
  - Component timing (process)
  - Voltage & temperature
  - Package & PCB routing lengths
  - PCB manufacturing variations (Z_0, loss)

Establishing Timing Budgets



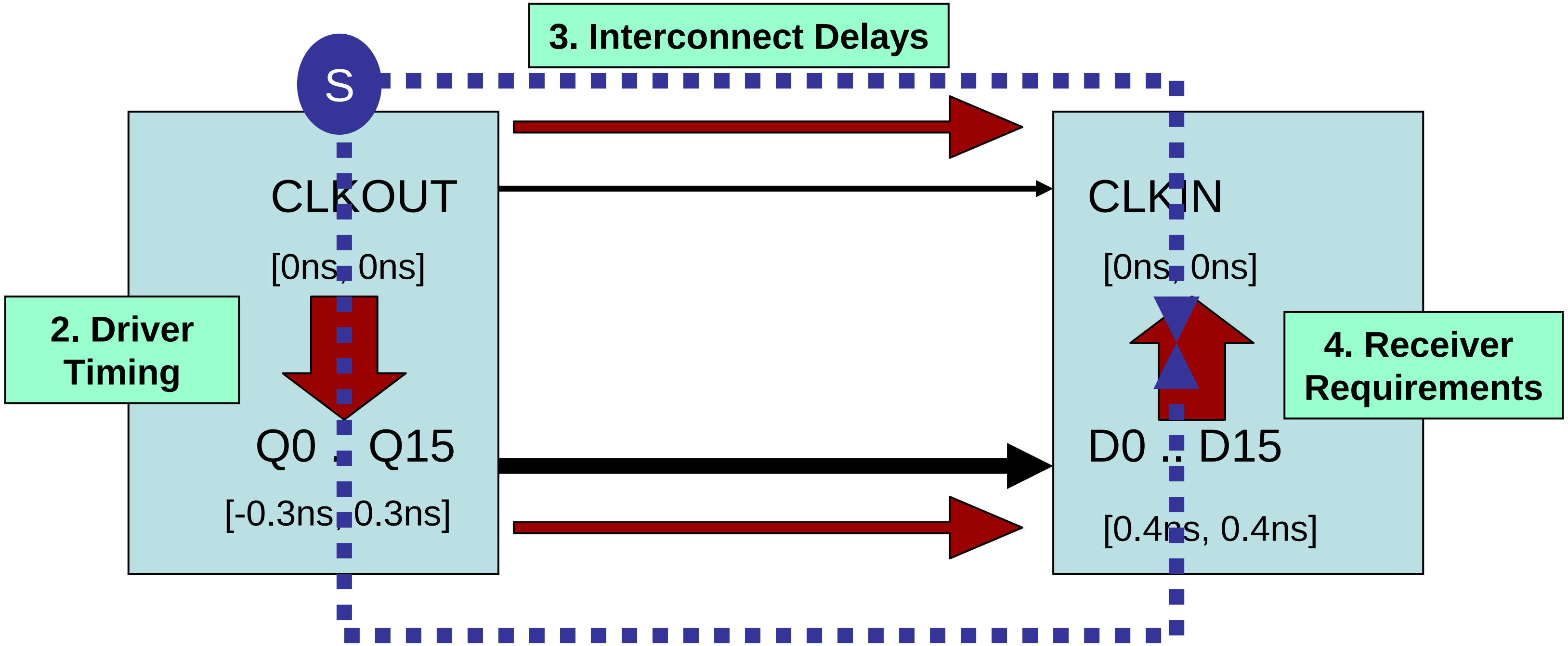
- High speed interfaces have one or more “transactions” that require timing closure
- Memory example:
  - Address/control
  - Data read
  - Data write
  - Strobe to Clock
- Timing relationships must be identified and closed for each different transaction

Source-Sync Transaction Example



- Establish component timing & transfer protocol
- Derive timing equations
- Idealized timing analysis
- Signal integrity analysis and Timing Closure

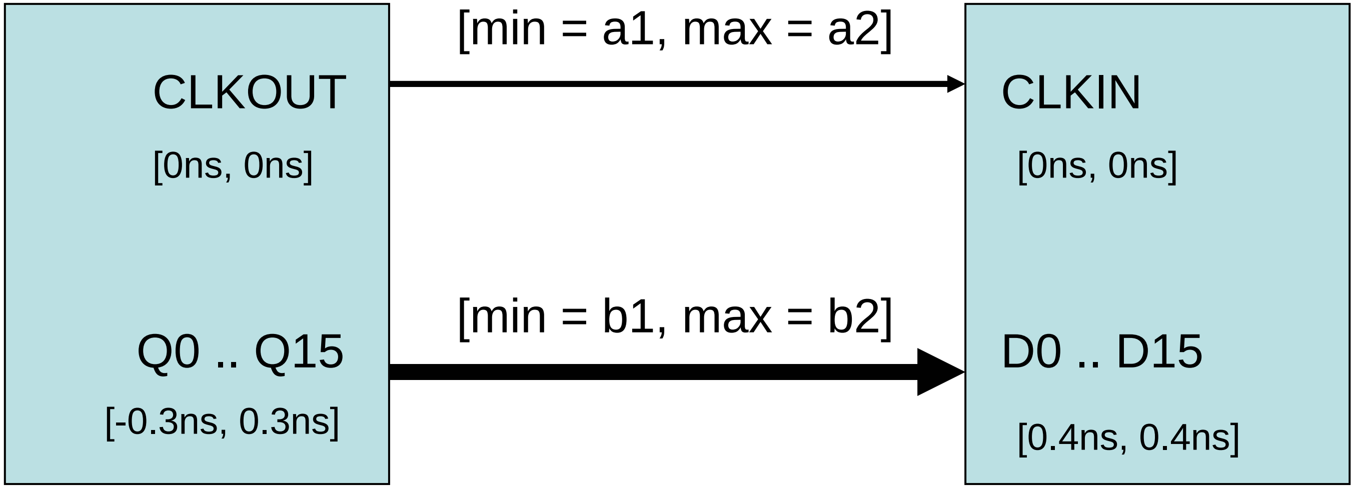
Component Timing, Transfer Protocol



1. Design Goals

Clock = 250 MHz
Source Sync, DDR transfer
Data Unit Interval = 2ns
90^{o} clock shift on PCB

Derive Timing Equations



Setup margin = [early clock] – [late data] – [setup requirement]
= [0ns + a1] – [0.3ns + b2] - [0.4ns]
= a1 – b2 – 0.7ns

Hold margin = [Data UI] + [early data] – [late clock] - [hold requirement]
= [2ns] + [-0.3ns + b1] – [0ns + a2] - [0.4ns]
= 1.3ns + b1 – a2

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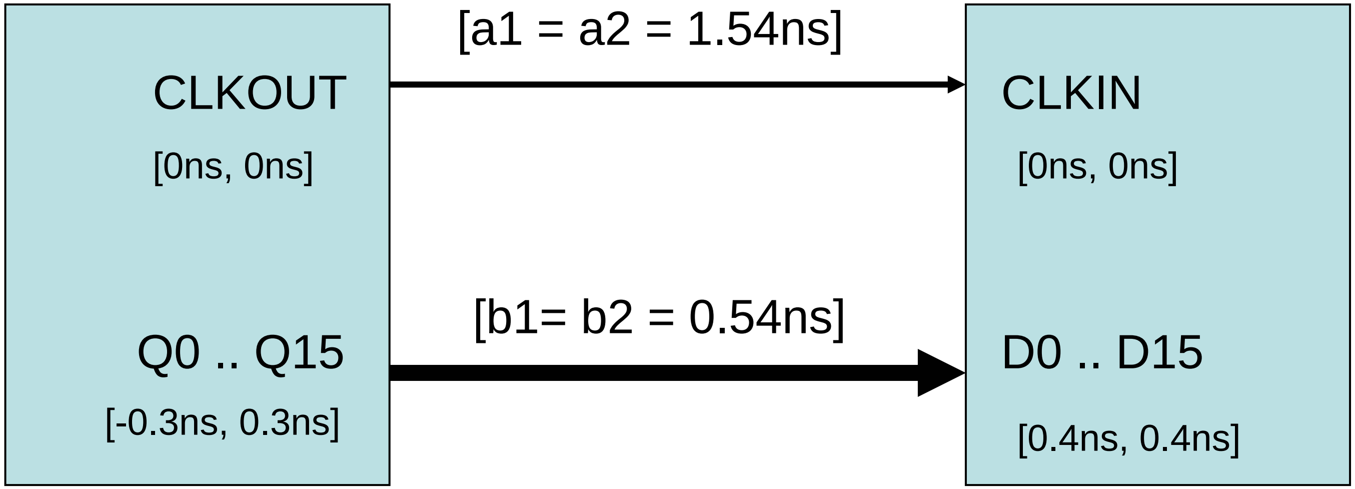
Idealized Timing Analysis

Minimum data length = 3”, at 180ps/in = 0.54ns



[a1 = a2 = 1.54ns]

CLKOUT

[0ns, 0ns]

CLKIN

[0ns, 0ns]

[b1= b2 = 0.54ns]

Q0 .. Q15

[-0.3ns, 0.3ns]

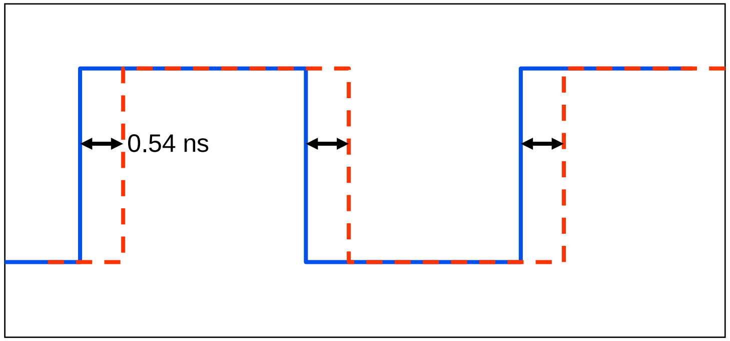
D0 .. D15

[0.4ns, 0.4ns]

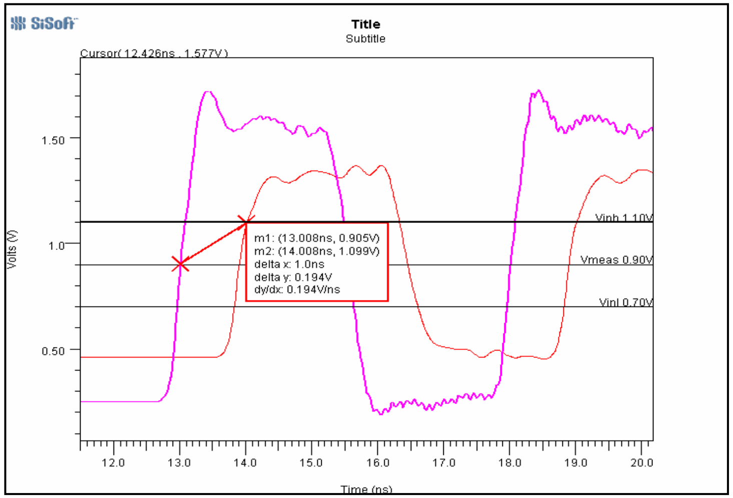
Setup margin = a1 – b2 – 0.7ns
= 1.54ns – 0.54ns – 0.7ns
= 0.3 ns

Hold margin = 1.3ns + b1 – a2
= 1.3ns + 0.54ns – 1.54ns
= 0.3ns

The Role of Signal Integrity



Idealized Delays

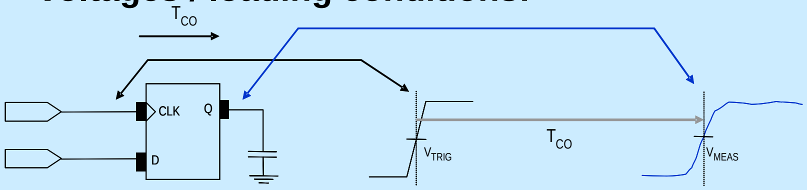


Real-World Delays

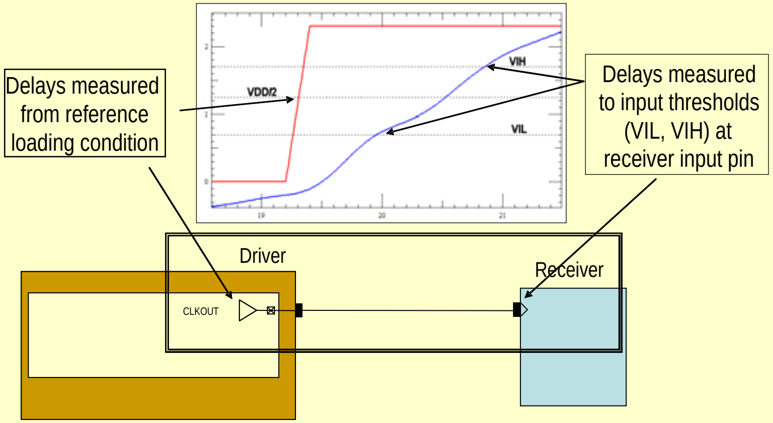
- Detailed analysis of digital switching behavior
- IBIS or HSpice models define I/O buffer behavior
- Accounts for
  - Actual circuit loading
  - Reflections / ringing
  - Circuit topology
  - Inter-symbol interference
  - Switching thresholds

Reconciling SI with Timing

- **Device delays are measured using specific voltages / loading conditions:**



- **SI flight times must be measured based on those same conditions:**

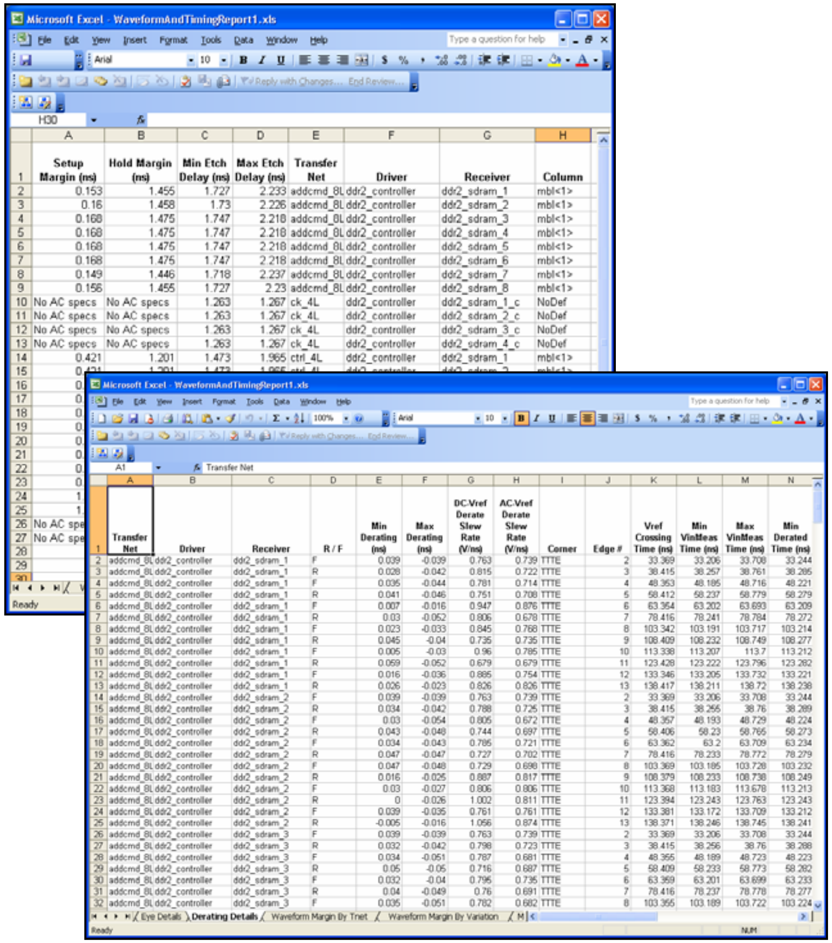


Delays measured from reference loading condition

Delays measured to input thresholds (VIL, VIH) at receiver input pin

- Static timing and signal integrity measurements *must* be compatible
- SI measurements are “normalized” to conditions under which loading is specified
  - IBIS Vref, Cref, Rref, Vmeas
- Timing Closure occurs when integrated timing/SI results show acceptable setup/hold margins

Building an Executable Timing Model



Microsoft Excel - WaveformAndTimingReport1.xls

	A	B	C	D	E	F	G	H
1	Setup Margin (ns)	Hold Margin (ns)	Min Etch Delay (ns)	Max Etch Delay (ns)	Transfer Net	Driver	Receiver	Column
2	0.153	1.455	1.727	2.233	addcmd_8L	ddr2_controller	ddr2_sdram_1	mbl<1>
3	0.16	1.458	1.73	2.226	addcmd_8L	ddr2_controller	ddr2_sdram_2	mbl<1>
4	0.168	1.475	1.747	2.218	addcmd_8L	ddr2_controller	ddr2_sdram_3	mbl<1>
5	0.168	1.475	1.747	2.218	addcmd_8L	ddr2_controller	ddr2_sdram_4	mbl<1>
6	0.168	1.475	1.747	2.218	addcmd_8L	ddr2_controller	ddr2_sdram_5	mbl<1>
7	0.168	1.475	1.747	2.218	addcmd_8L	ddr2_controller	ddr2_sdram_6	mbl<1>
8	0.149	1.446	1.718	2.237	addcmd_8L	ddr2_controller	ddr2_sdram_7	mbl<1>
9	0.156	1.455	1.727	2.23	addcmd_8L	ddr2_controller	ddr2_sdram_8	mbl<1>
10	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_1_c	NoDef
11	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_2_c	NoDef
12	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_3_c	NoDef
13	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_4_c	NoDef
14	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_1	mbl<1>
15	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_2	mbl<1>

Microsoft Excel - WaveformAndTimingReport1.xls

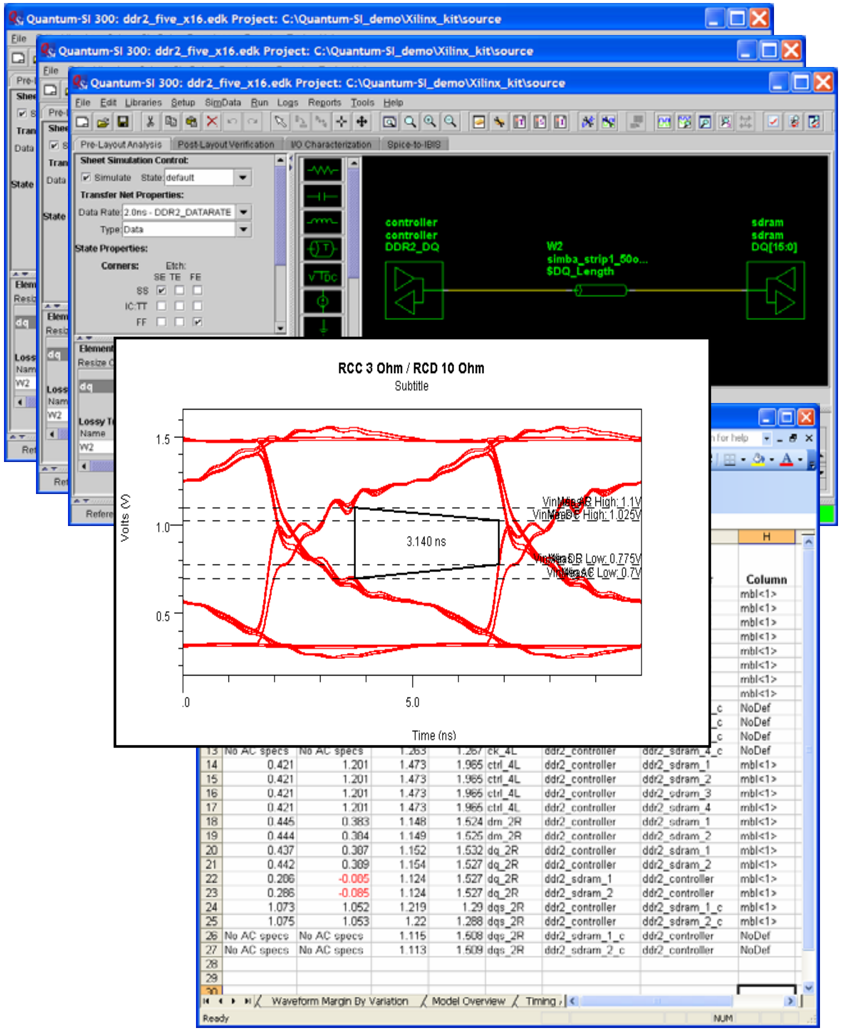
A1 Transfer Net

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1	Transfer Net	Driver	Receiver	R / F	Min Derating (ns)	Max Derating (ns)	DC-Vref Derate Slew Rate (V/ns)	AC-Vref Derate Slew Rate (V/ns)	Corner	Edge #	Vref Crossing Time (ns)	Min VinMeas Time (ns)	Max VinMeas Time (ns)	Min Derated Time (ns)
2	addcmd_8L	ddr2_controller	ddr2_sdram_1	F	0.039	-0.039	0.763	0.739	TTTE	2	33.369	33.206	33.708	33.244
3	addcmd_8L	ddr2_controller	ddr2_sdram_1	R	0.028	-0.042	0.815	0.722	TTTE	3	38.415	38.257	38.761	38.285
4	addcmd_8L	ddr2_controller	ddr2_sdram_1	F	0.035	-0.044	0.781	0.714	TTTE	4	48.363	48.185	48.716	48.221
5	addcmd_8L	ddr2_controller	ddr2_sdram_1	R	0.041	-0.046	0.751	0.708	TTTE	5	58.412	58.237	58.779	58.279
6	addcmd_8L	ddr2_controller	ddr2_sdram_1	F	0.007	-0.016	0.947	0.876	TTTE	6	63.354	63.202	63.693	63.209
7	addcmd_8L	ddr2_controller	ddr2_sdram_1	R	0.03	-0.052	0.806	0.678	TTTE	7	78.416	78.241	78.784	78.272
8	addcmd_8L	ddr2_controller	ddr2_sdram_1	F	0.023	-0.033	0.845	0.768	TTTE	8	103.342	103.191	103.717	103.214
9	addcmd_8L	ddr2_controller	ddr2_sdram_1	R	0.045	-0.04	0.735	0.735	TTTE	9	108.409	108.232	108.749	108.277
10	addcmd_8L	ddr2_controller	ddr2_sdram_1	F	0.005	-0.03	0.96	0.785	TTTE	10	113.338	113.207	113.7	113.212
11	addcmd_8L	ddr2_controller	ddr2_sdram_1	R	0.059	-0.052	0.679	0.679	TTTE	11	123.428	123.222	123.796	123.282
12	addcmd_8L	ddr2_controller	ddr2_sdram_1	F	0.016	-0.036	0.885	0.754	TTTE	12	133.346	133.205	133.732	133.221
13	addcmd_8L	ddr2_controller	ddr2_sdram_1	R	0.026	-0.023	0.826	0.826	TTTE	13	138.417	138.211	138.72	138.238
14	addcmd_8L	ddr2_controller	ddr2_sdram_2	F	0.039	-0.039	0.763	0.739	TTTE	2	33.369	33.206	33.708	33.244
15	addcmd_8L	ddr2_controller	ddr2_sdram_2	R	0.034	-0.042	0.788	0.725	TTTE	3	38.415	38.256	38.76	38.289
16	addcmd_8L	ddr2_controller	ddr2_sdram_2	F	0.03	-0.054	0.805	0.672	TTTE	4	48.357	48.193	48.729	48.224
17	addcmd_8L	ddr2_controller	ddr2_sdram_2	R	0.043	-0.048	0.744	0.697	TTTE	5	58.406	58.23	58.765	58.273
18	addcmd_8L	ddr2_controller	ddr2_sdram_2	F	0.034	-0.043	0.785	0.721	TTTE	6	63.362	63.2	63.709	63.234
19	addcmd_8L	ddr2_controller	ddr2_sdram_2	R	0.047	-0.047	0.727	0.702	TTTE	7	78.416	78.233	78.772	78.279
20	addcmd_8L	ddr2_controller	ddr2_sdram_2	F	0.047	-0.048	0.729	0.698	TTTE	8	103.369	103.185	103.728	103.232
21	addcmd_8L	ddr2_controller	ddr2_sdram_2	R	0.016	-0.025	0.887	0.817	TTTE	9	108.379	108.233	108.738	108.249
22	addcmd_8L	ddr2_controller	ddr2_sdram_2	F	0.03	-0.027	0.806	0.806	TTTE	10	113.368	113.183	113.678	113.213
23	addcmd_8L	ddr2_controller	ddr2_sdram_2	R	0	-0.026	1.002	0.811	TTTE	11	123.394	123.243	123.763	123.243
24	addcmd_8L	ddr2_controller	ddr2_sdram_2	F	0.039	-0.035	0.761	0.761	TTTE	12	133.381	133.172	133.709	133.212
25	addcmd_8L	ddr2_controller	ddr2_sdram_2	R	-0.005	-0.016	1.056	0.874	TTTE	13	138.371	138.246	138.745	138.241
26	addcmd_8L	ddr2_controller	ddr2_sdram_3	F	0.039	-0.039	0.763	0.739	TTTE	2	33.369	33.206	33.708	33.244
27	addcmd_8L	ddr2_controller	ddr2_sdram_3	R	0.032	-0.042	0.798	0.723	TTTE	3	38.415	38.256	38.76	38.288
28	addcmd_8L	ddr2_controller	ddr2_sdram_3	F	0.034	-0.051	0.787	0.681	TTTE	4	48.355	48.189	48.723	48.223
29	addcmd_8L	ddr2_controller	ddr2_sdram_3	R	0.05	-0.05	0.716	0.687	TTTE	5	58.409	58.233	58.773	58.282
30	addcmd_8L	ddr2_controller	ddr2_sdram_3	F	0.032	-0.04	0.795	0.735	TTTE	6	63.369	63.201	63.699	63.233
31	addcmd_8L	ddr2_controller	ddr2_sdram_3	R	0.04	-0.049	0.76	0.691	TTTE	7	78.416	78.237	78.778	78.277
32	addcmd_8L	ddr2_controller	ddr2_sdram_3	F	0.035	-0.051	0.782	0.682	TTTE	8	103.355	103.189	103.722	103.224

- For each interface, all transactions must be validated for all cases:
  - Component timing (process)
  - Voltage, temperature
  - PCB variations
- Creating an executable timing model to perform automatic regression is ideal
- Possibilities
  - Excel
  - Custom scripting
  - EDA tools

$$t_{cycle} = t_{co} + t_{final\ settling} + t_{setup} + t_{skew} + t_{jitter} + t_{SSO} + t_{ISI}$$

Pre-Route SI Exploration



Sheet Simulation Control:
☑ Simulate State: default

Transfer Net Properties:
Data Rate: 2.0ns - DDR2_DATARATE
Type: Data

State Properties:
Corners: Etch:

	SE	TE	FE
SS	☑	□	□
IC:TT	□	□	□
FF	□	□	☑

								Column
13	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_4_c	NoDef
14	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_1	mbl<1>
15	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_2	mbl<1>
16	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_3	mbl<1>
17	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_4	mbl<1>
18	0.445	0.383	1.148	1.524	dm_2R	ddr2_controller	ddr2_sdram_1	mbl<1>
19	0.444	0.384	1.149	1.525	dm_2R	ddr2_controller	ddr2_sdram_2	mbl<1>
20	0.437	0.387	1.152	1.532	dq_2R	ddr2_controller	ddr2_sdram_1	mbl<1>
21	0.442	0.389	1.154	1.527	dq_2R	ddr2_controller	ddr2_sdram_2	mbl<1>
22	0.206	-0.005	1.124	1.527	dq_2R	ddr2_sdram_1	ddr2_controller	mbl<1>
23	0.286	-0.085	1.124	1.527	dq_2R	ddr2_sdram_2	ddr2_controller	mbl<1>
24	1.073	1.052	1.219	1.29	dqs_2R	ddr2_controller	ddr2_sdram_1_c	mbl<1>
25	1.075	1.053	1.22	1.288	dqs_2R	ddr2_controller	ddr2_sdram_2_c	mbl<1>
26	No AC specs	No AC specs	1.115	1.508	dqs_2R	ddr2_sdram_1_c	ddr2_controller	NoDef
27	No AC specs	No AC specs	1.113	1.509	dqs_2R	ddr2_sdram_2_c	ddr2_controller	NoDef
28								
29								
30								

- Pre-route simulations model planned
  - Drivers
  - Receivers
  - Routing topology & lengths
  - Termination
- Simulated interconnect delays are extracted and plugged back into the Executable Timing Model
- Setup and hold margins are calculated for temperature, process and voltage corners

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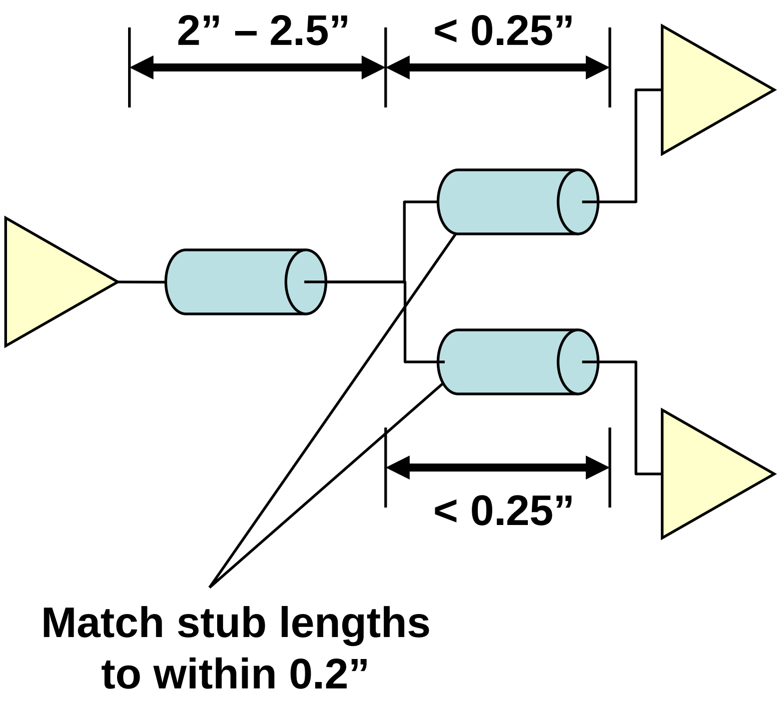
Driving Physical Design



- Pre-route SI/Timing analysis defines PCB routing rules
- Rules usually include pin ordering, length limits and stub matching
- Driving automated rules into PCB CAD is essential

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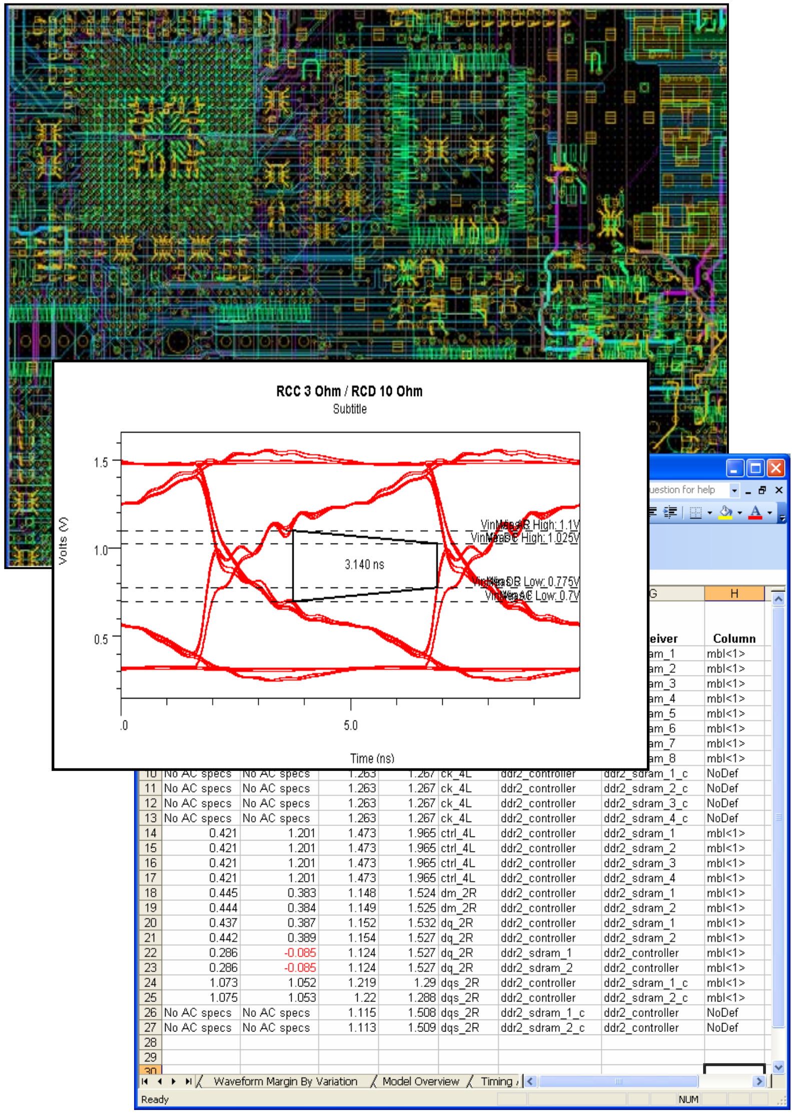
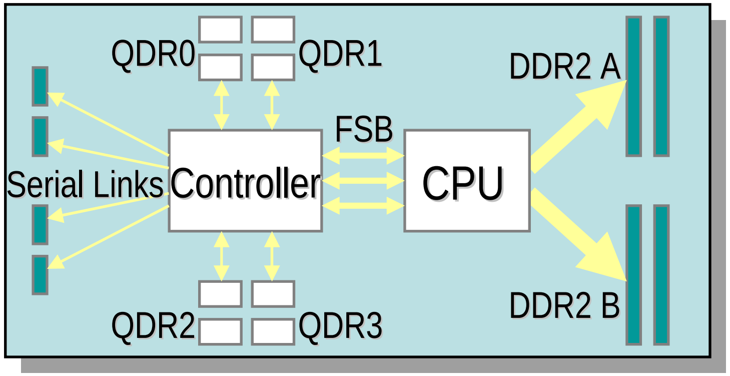
Post-Route Validation



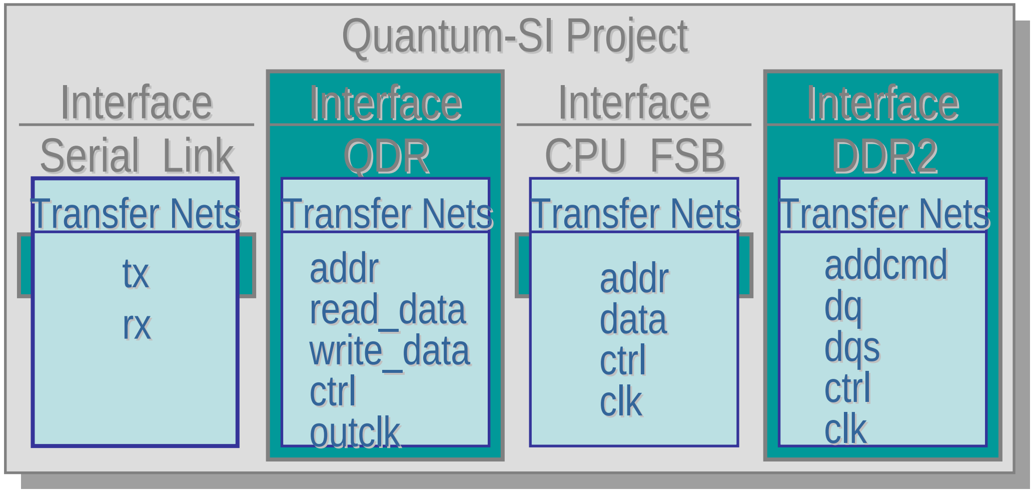
							G	H
							eiver	Column
							am_1	mbl<1>
							am_2	mbl<1>
							am_3	mbl<1>
							am_4	mbl<1>
							am_5	mbl<1>
							am_6	mbl<1>
							am_7	mbl<1>
							am_8	mbl<1>
10	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_1_c	NoDef
11	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_2_c	NoDef
12	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_3_c	NoDef
13	No AC specs	No AC specs	1.263	1.267	ck_4L	ddr2_controller	ddr2_sdram_4_c	NoDef
14	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_1	mbl<1>
15	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_2	mbl<1>
16	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_3	mbl<1>
17	0.421	1.201	1.473	1.965	ctrl_4L	ddr2_controller	ddr2_sdram_4	mbl<1>
18	0.445	0.383	1.148	1.524	dm_2R	ddr2_controller	ddr2_sdram_1	mbl<1>
19	0.444	0.384	1.149	1.525	dm_2R	ddr2_controller	ddr2_sdram_2	mbl<1>
20	0.437	0.387	1.152	1.532	dq_2R	ddr2_controller	ddr2_sdram_1	mbl<1>
21	0.442	0.389	1.154	1.527	dq_2R	ddr2_controller	ddr2_sdram_2	mbl<1>
22	0.286	-0.085	1.124	1.527	dq_2R	ddr2_sdram_1	ddr2_controller	mbl<1>
23	0.286	-0.085	1.124	1.527	dq_2R	ddr2_sdram_2	ddr2_controller	mbl<1>
24	1.073	1.052	1.219	1.29	dqs_2R	ddr2_controller	ddr2_sdram_1_c	mbl<1>
25	1.075	1.053	1.22	1.288	dqs_2R	ddr2_controller	ddr2_sdram_2_c	mbl<1>
26	No AC specs	No AC specs	1.115	1.508	dqs_2R	ddr2_sdram_1_c	ddr2_controller	NoDef
27	No AC specs	No AC specs	1.113	1.509	dqs_2R	ddr2_sdram_2_c	ddr2_controller	NoDef
28								
29								
30								

- Routed topologies are extracted from PCB database and simulated
- Simulated interconnect delays are extracted and plugged back into system timing model
- Setup and hold margins are calculated for temperature, process and voltage corners

Design Analysis Reuse

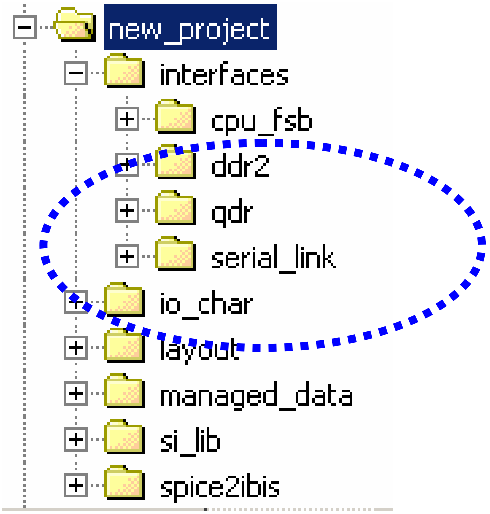


Once all the SI/timing data for an interface has been captured, it should be possible to directly reuse that information for multiple instances in a project or other projects



Quantum-SI Project

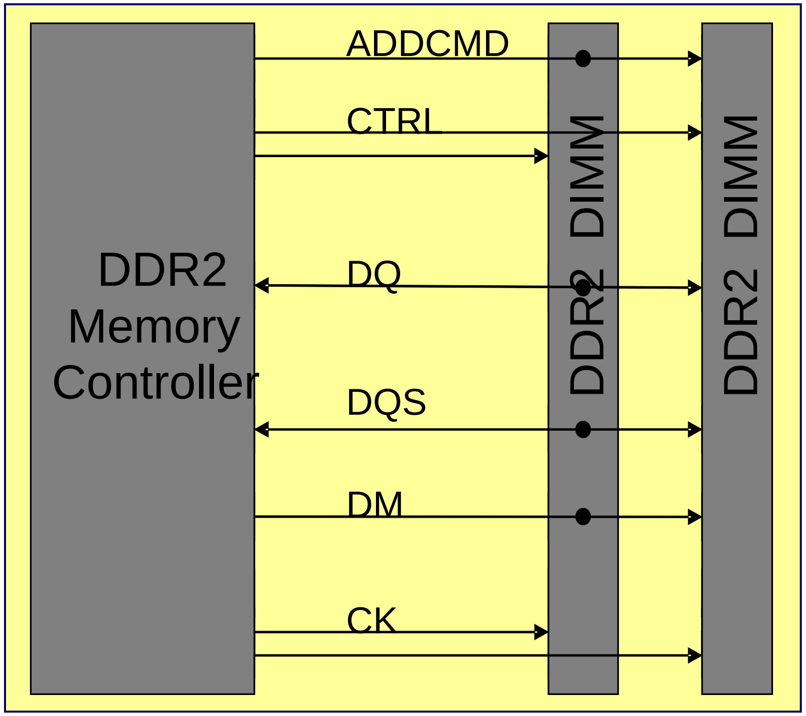
Interface Serial Link	Interface QDR	Interface CPU FSB	Interface DDR2
Transfer Nets	Transfer Nets	Transfer Nets	Transfer Nets
tx rx	addr read_data write_data ctrl outclk	addr data ctrl clk	addcmd dq dqs ctrl clk



```
new_project
  interfaces
    cpu_fsb
    ddr2
    qdr
    serial_link
  io_char
  layout
  managed_data
  si_lib
  spice2ibis
```

Each interface kit contains net class schematics, timing data & SI models

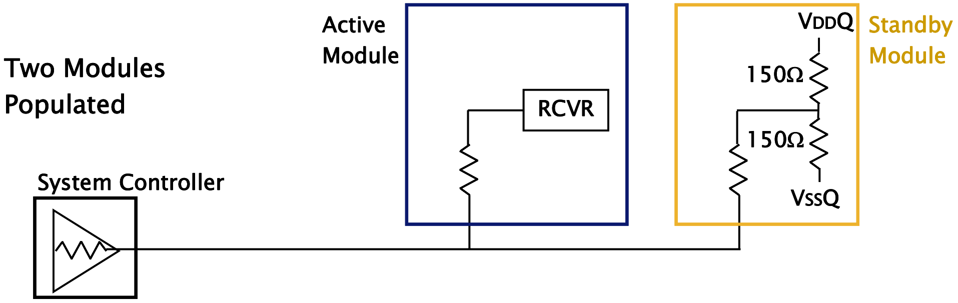
Case Study: DDR2 System Memory



- DDR2 supports one or two DIMM modules
- DIMM Modules
  - Registered and Unbuffered
  - 4 to 18 memory devices
- Two module, data write transaction is presented here
- Complete case study:

  "Features and Implementation of High-Performance 667Mbs and 800Mbs DDRII Memory Systems"
  - Presented by Micron & SiSoft
  - DesignCon West, 2005
- http://www.sisoft.com/papers.asp

DDR2 Data Write Configuration



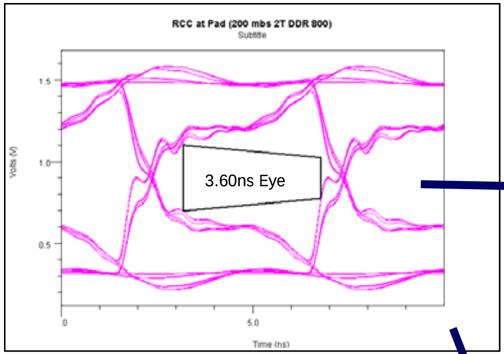
Write Configurations						
Configuration	Write to	DQ Active-Term Resistance				
		Controller	Dram at Slot 1		Dram at Slot 2	
			Front Side	Back Side	Front Side	Back Side
2R / 2R	Slot 1	No Term	No Term	No Term	50 or 75 ohm	No Term
	Slot 2	No Term	50 or 75 ohm	No Term	No Term	No Term
2R / 1R	Slot 1	No Term	No Term	No Term	50 or 75 ohm	Empty
	Slot 2	No Term	50 or 75 ohm	No Term	No Term	Empty
1R / 2R	Slot 1	No Term	No Term	Empty	50 or 75 ohm	No Term
	Slot 2	No Term	50 or 75 ohm	Empty	No Term	No Term
1R / 1R	Slot 1	No Term	No Term	Empty	50 or 75 ohm	Empty
	Slot 2	No Term	50 or 75 ohm	Empty	No Term	Empty
2R / Empty	Slot 1	No Term	150 ohm	No Term	Empty	Empty
Empty / 2R	Slot 2	No Term	Empty	Empty	150 ohm	No Term
1R / Empty	Slot 1	No Term	150 ohm	Empty	Empty	Empty
Empty / 1R	Slot 2	No Term	Empty	Empty	150 ohm	Empty

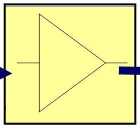
- Termination strategy is dynamic; depends on how many DIMMs are present and which device is receiving
- Simulation environment must switch receiver models based on which case is being analyzed

Slew Rate Derating – “Virtual Eye”

Eye at device pad

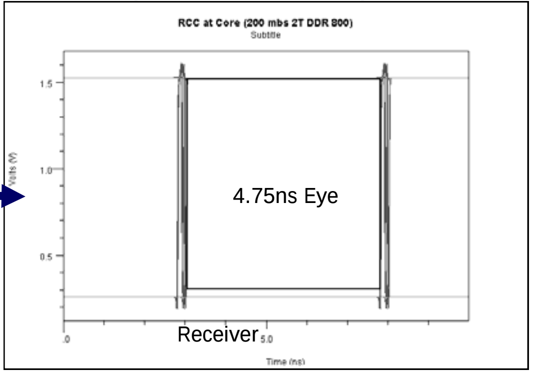
(simulated result)



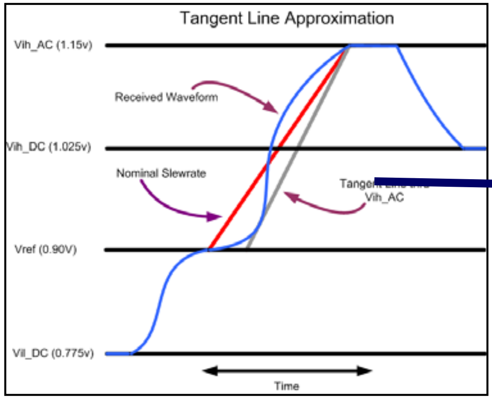


Eye at receiver output

(simulated result)



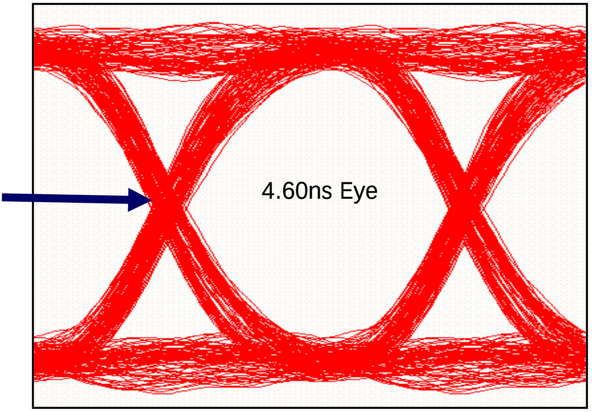
Waveform derating scheme



Waveform processing

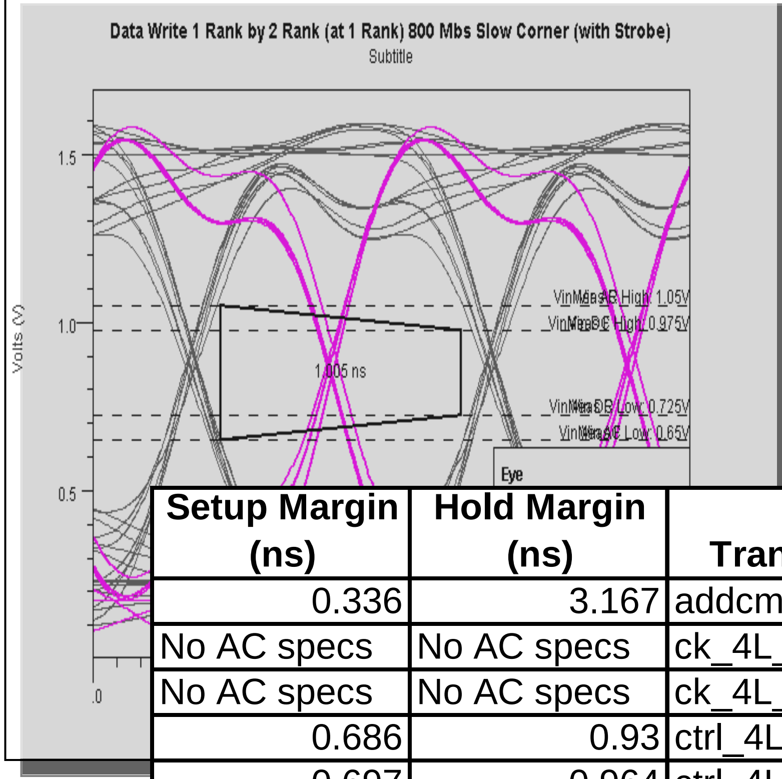
Virtual eye at receiver

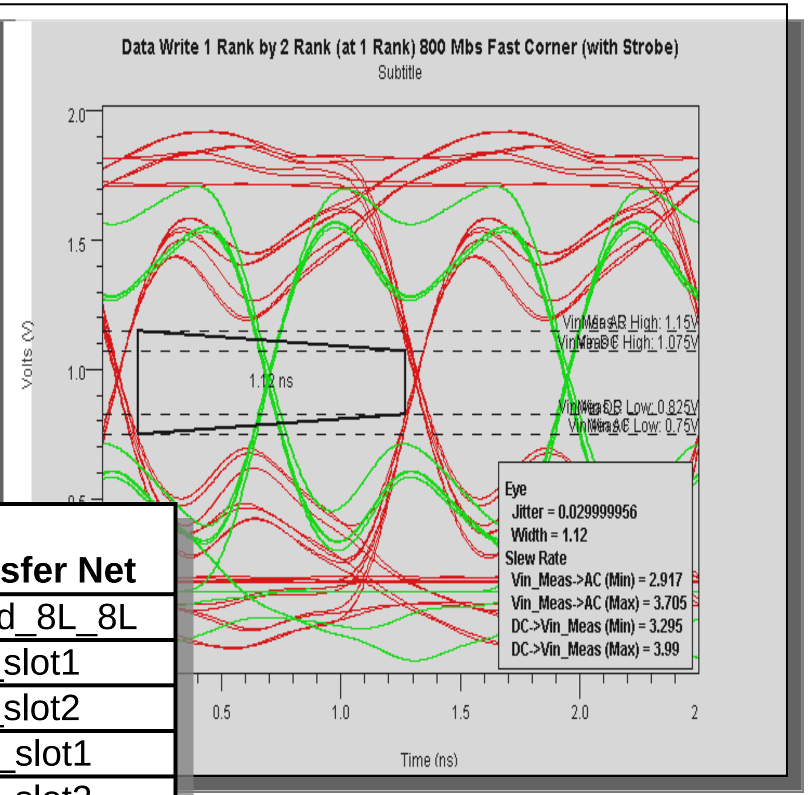
(computed result)



DDR2 Analysis Results

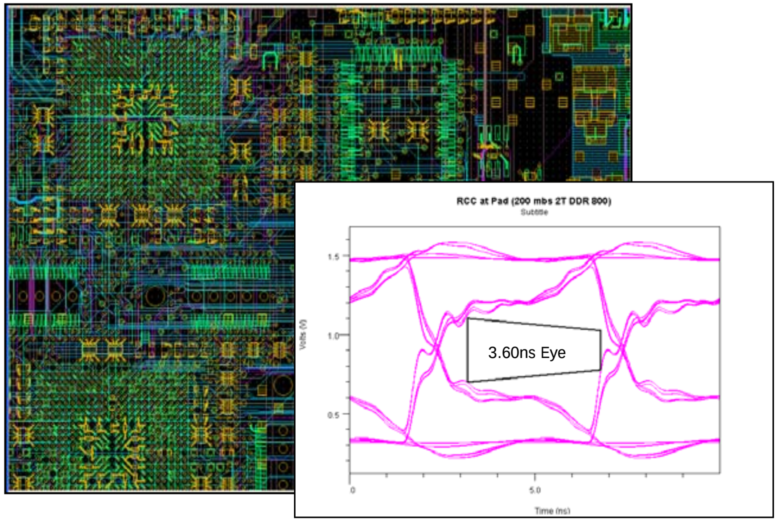
Data Write Slow / Fast Corners





Setup Margin (ns)	Hold Margin (ns)	Transfer Net
0.336	3.167	addcmd_8L_8L
No AC specs	No AC specs	ck_4L_slot1
No AC specs	No AC specs	ck_4L_slot2
0.686	0.93	ctrl_4L_slot1
0.697	0.964	ctrl_4L_slot2
0.468	0.205	dm_2R_2R
0.213	-0.148	dq_2R_2R
1.155	0.944	dqs_2R_2R

Summary



Setup Margin (ns)	Hold Margin (ns)	Transfer Net
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No AC specs	No AC specs	ck_4L_slot1
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- High-speed system design requires a rigorous, repeatable methodology for achieving Timing Closure
- Static Timing, Signal Integrity, and physical design rules are all interrelated
- An Executable Timing Model allows for a user to validate all transactions across all cases
- Signal Integrity analysis must be performed in accordance with the system timing model