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System-Level SSO Simulation Techniques with Various IBIS Package Models

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Presentation Outline

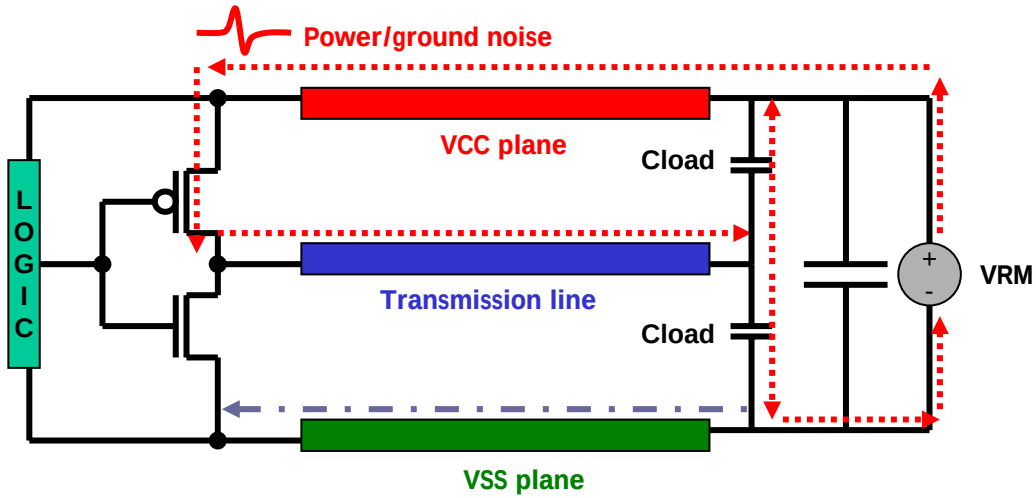
Simultaneous Switching Output Noise Analysis – a.k.a SSO/SSN

- Fundamentals of SSO Mechanisms
- Typical SSO Simulation Setup
- IBIS Package Modeling Choices
- Case study to compare the package models
- Summary

The SSO / SSN Problem

- SSO, SSN, Power/Ground Bounce, Delta-I Noise, …
  - Simultaneous Switching Output, Simultaneous Switching Noise, di/dt, power and ground voltage fluctuations, etc.
- Two types: I/O switching and Core logic switching
  - This presentation focuses on I/O SSO analysis

Fundamentals of I/O SSO Mechanisms



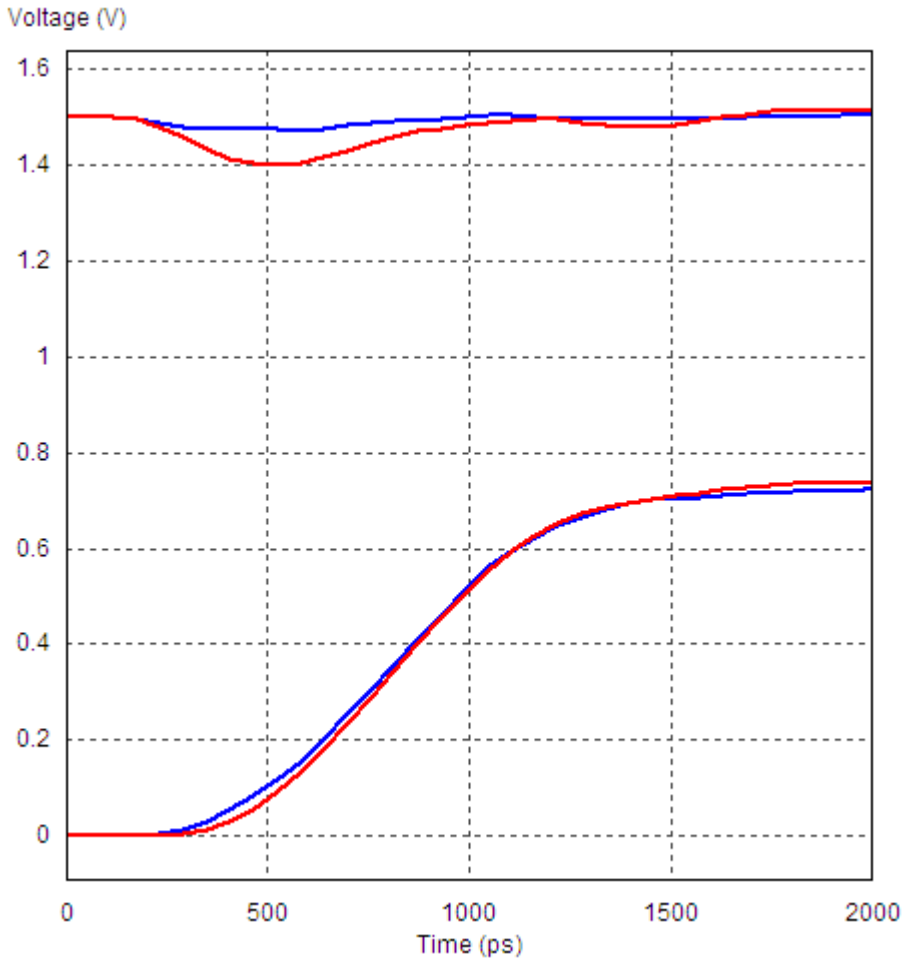
When the output is driven high, the transmission line is connected to the PWR net at the driver. When the output is driven low, the transmission line is connected to the GND net at the driver. This connection forms one end of the sig/gnd or sig/pwr loop.

The capacitive loads (for typical CMOS technologies) complete the sig/gnd and sig/pwr loops. Return current takes the path of least impedance, so PDS performance is key.

All three loops are important factors for optimizing signal quality and reducing PDS noise.

Fundamentals of I/O SSO Mechanisms

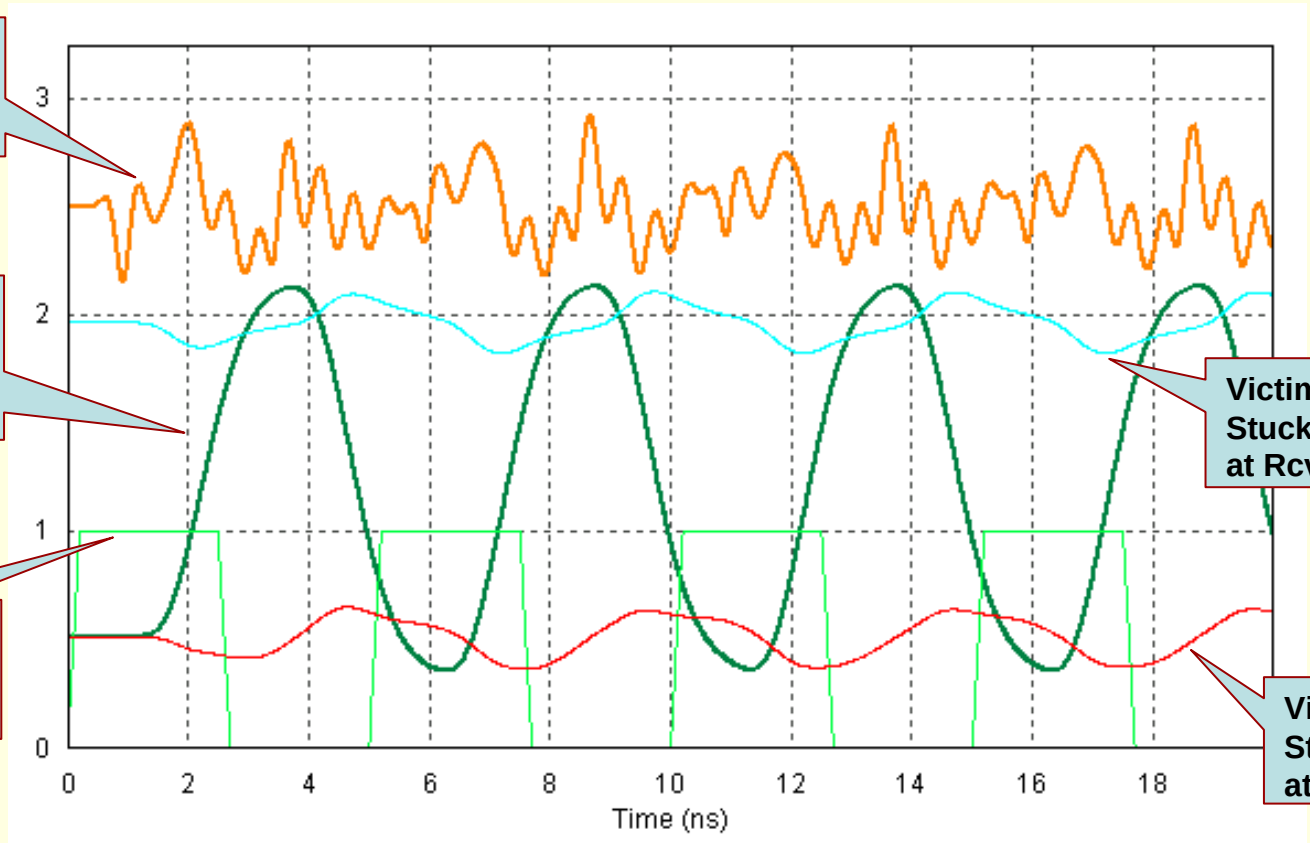
- SSO is a combination of signal and power integrity issues
- Affects signal edge rate, timing and voltage margins
- System-level issue involving both packages and PCBs
- Multiple signal net crosstalk mechanisms – trace / via / pin
- Two components of PDS noise
  - PDS current supplied to devices
  - Return currents from I/Os
- BGA inductance presents a fundamental limitation on the PCB's PDS freq. range; the package is responsible for decoupling above that freq. region
- PCB layout can only do so much – it cannot solve package design problems



Blue – Single I/O switching results

Red – Two I/Os switching results

Typical SSO Analysis Results

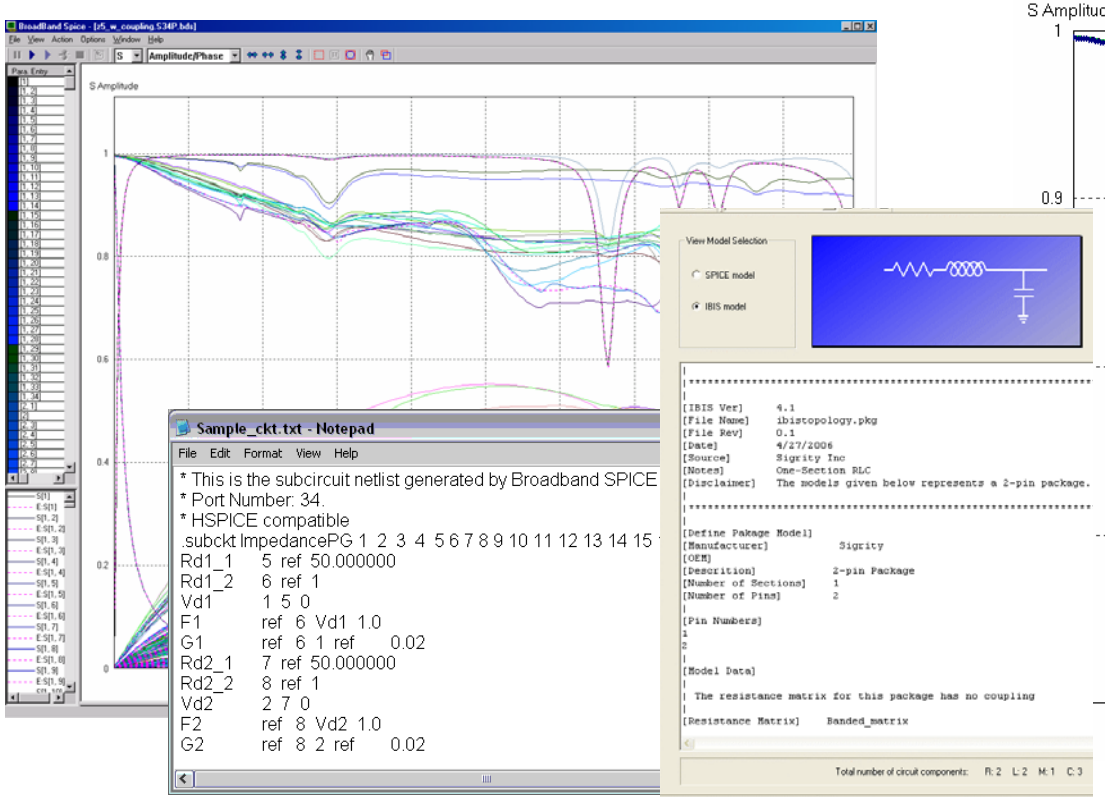


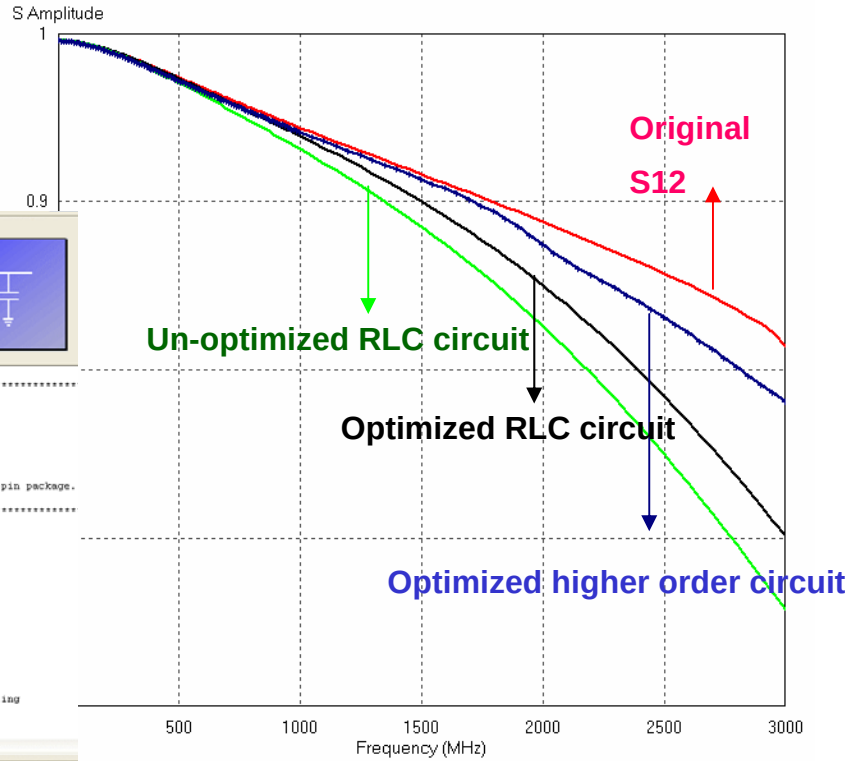
Set two of the data bits as stuck high and stuck low victims. These results can assist with more in-depth analysis of the power and ground rail fluctuations.

Typical IBIS-based SSO Analysis Setup

- PCB layout (including dielectric information)
- VRM location and model
- Decoupling capacitor locations and models
- Power, ground, and signal nets of interest
- Any interconnect terminations
- Switching patterns
  - PRBS recommended to find eye diagram and max PDS noise (simple 1010 repeating patters do not always yield worst-case)
- IBIS models
  - Drivers and receivers
  - On-die models highly recommended
  - Split c_comp and [Pin Mapping] should be requested from vendors for improved accuracy, otherwise make assumptions
  - IBIS supports multiple package models – which one to use?

Frequency Response and Accuracy of Various SPICE Equivalent Circuits for a Pkg I/O's S[1,2]

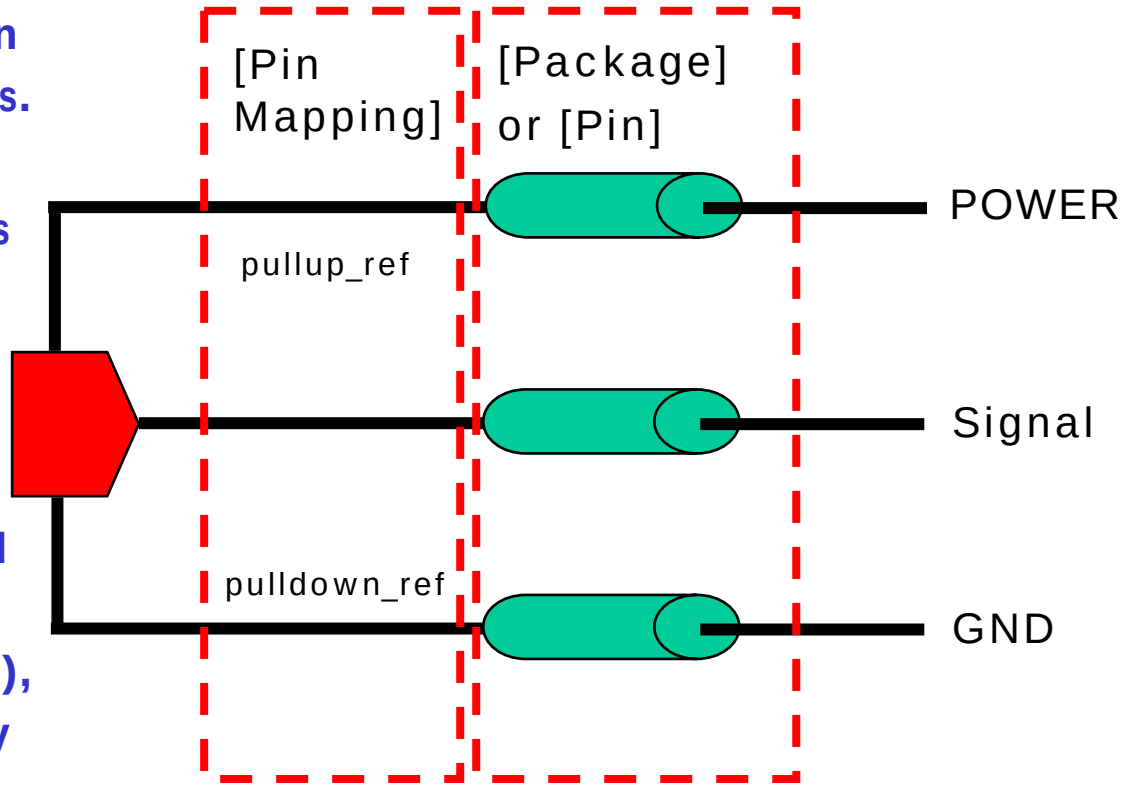




S-parameters are typically the most accurate modeling technique, but practically they can be difficult to use in system-level SSO simulations: more difficult to extract than RLCs, increased SSO simulation complexity, causality/passivity issues, and no formal integration with the IBIS specification makes simulation setup difficult in some tools.

Confusion with [Package] and [Pin] in IBIS

- The [Package] and [Pin] constructs do not allow any coupling between the power, signal, and ground nets.
- Therefore, these package models are only appropriate for two types of situations: ideal pwr/gnd simulations or packages that truly have negligible coupling between these three nets (e.g. leadframe).
- For packages that have power and ground planes (pins are inter-connected and nets have coupling), a per-pin RLC PDS model is usually not appropriate without great care.
- If RLCs for POWER and GND pins are present, how should they be interpreted / connected?



[Package Model] Can Include Coupling

- [Model Data] allows self and mutual inductances, capacitances, and resistances to be included
- The mutual terms are necessary to include all SSO mechanisms
- Power and ground pins can be lumped together to account for their interconnected nature on the package (one RLC for entire PDS)
- RLCs for individual power and ground pins are still not appropriate in general cases

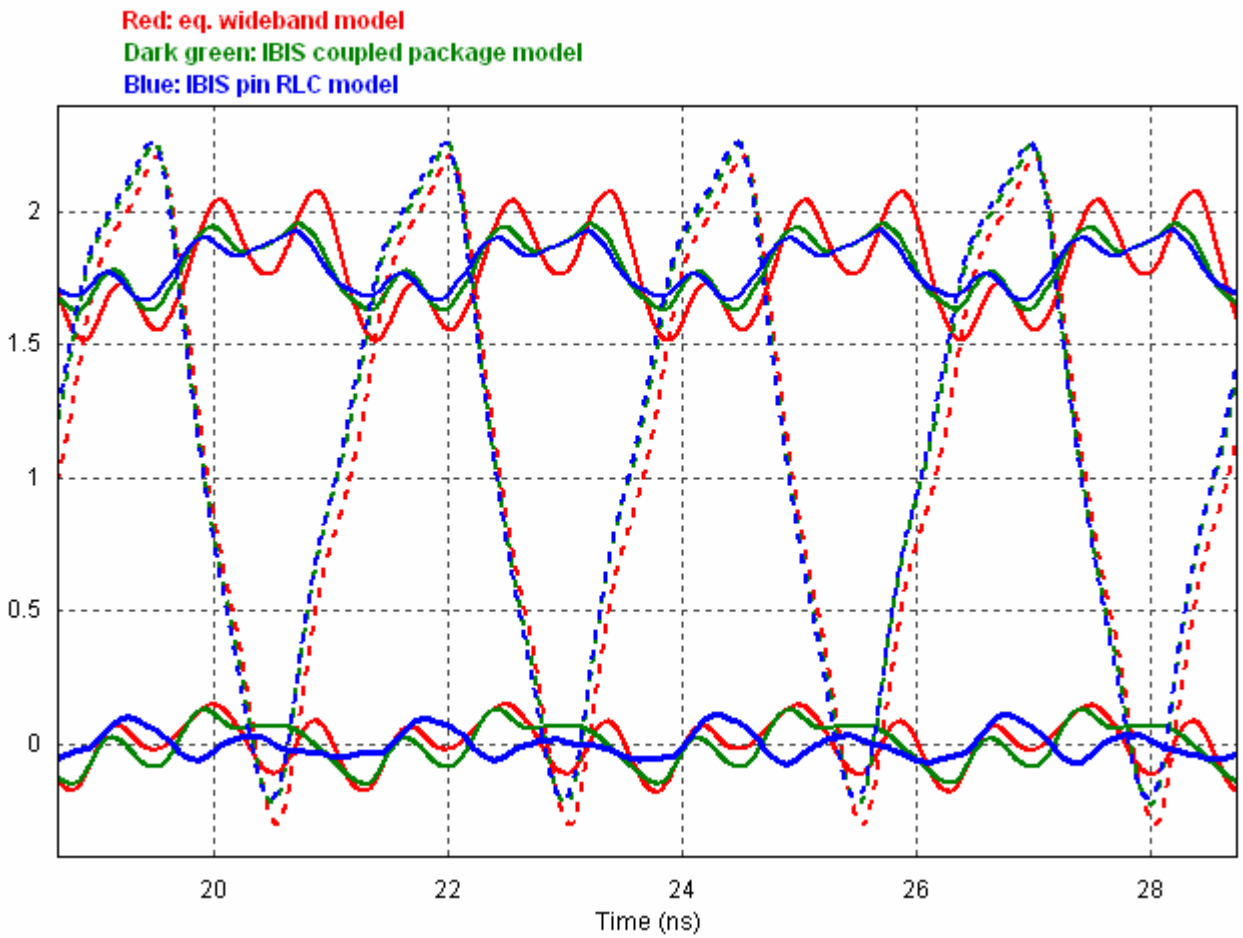
```
[IBIS Ver]      4.1
[Comment Char]  |_char
[File Name]     ibis_wirebond.pkg
[File Rev]      1.0
[Date]          8/9/2006
[Source]        Sigrity Extractor
[Notes]         One-Section RLC
[Disclaimer]    178-pin package
[Copyright]
|
|*****************************************
|
[Define Package Model]  ibis_wirebond
[Manufacturer]          Sigrity
[OEM]                   Sigrity
[Description]           178-pin Package
|
[Model Data]
|
[Inductance Matrix]     Sparse_matrix
[Row]     B19
B19      1.66704e-009
D3       3.71638e-010
W17      3.60196e-010
U16      3.90649e-010
```

Case Study: PCB DDRII Analysis to Compare the Three Package Choices

Analysis Methodology

- DDRII 800 interface (typical configuration)
- Three package choices were compared
  - [Pin] RLC model for signals only (no per-pin RLCs for PDS)
  - [Package Model] with full power/signal/ground coupling
  - Broadband S-parameter model
- Analyze PDS noise at the PCB, I/O waveforms at the receivers, and quiet nets (stuck high and low)
- 6 and 14 switching nets (8 and 16 I/Os total)
- On-die models were not included to enhance the waveform differences between the configurations

DDRII800 results – SSO signal noise
8 bits with 2 victims (stuck high and low)



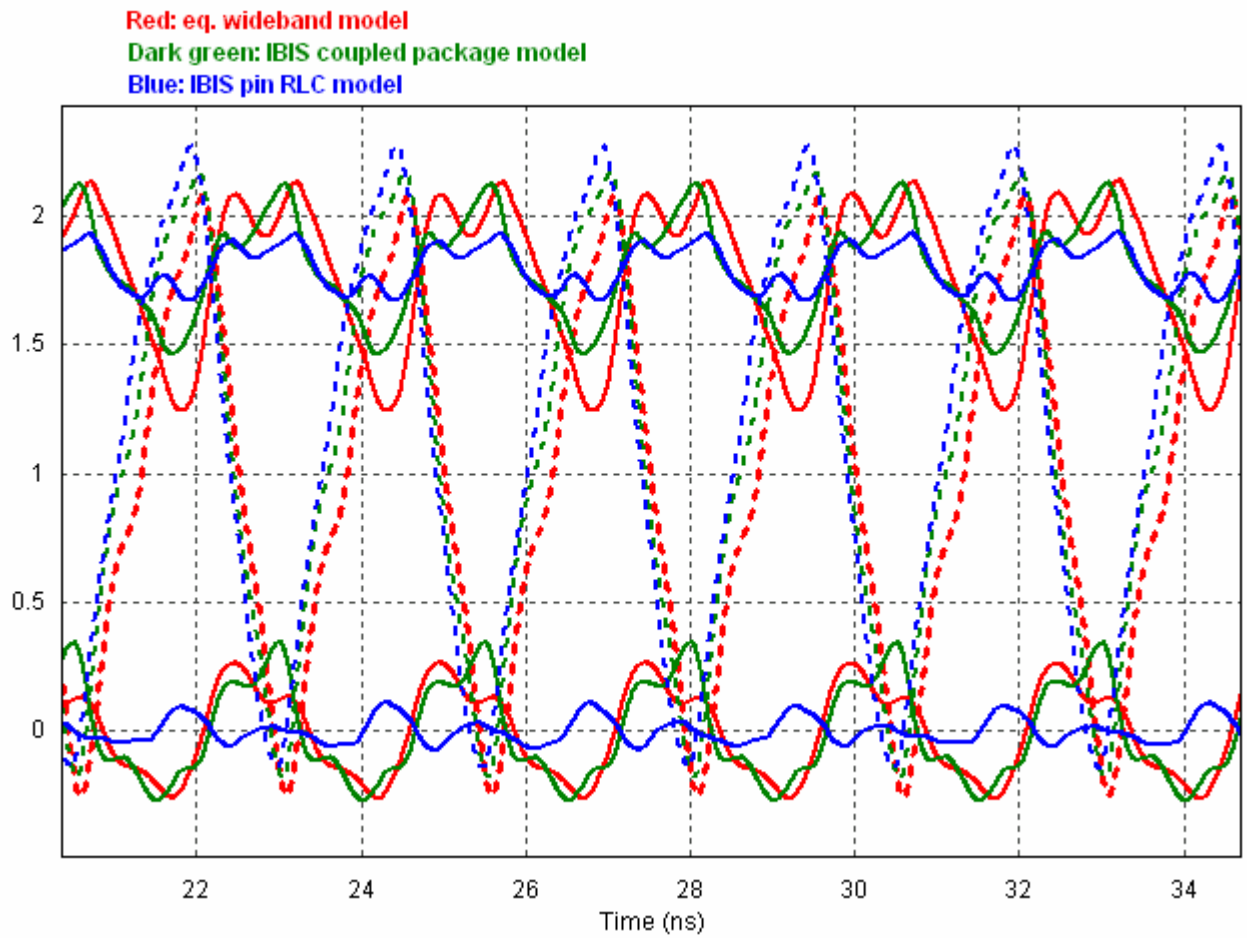
Broadband model yields the largest victim net SSO noise.

The three package models show their fundamental differences in capabilities.

The two IBIS package models show similar results for the stuck high line. This is because the stuck high noise will quite often follow the overall PDS noise when signals are only referenced to GND.

The stuck low results are quite different because signal-signal crosstalk can be a significant source of noise (not in the [Pin] model).

DDRII800 results – SSO signal noise
16 bits with 2 victims (stuck high and low)

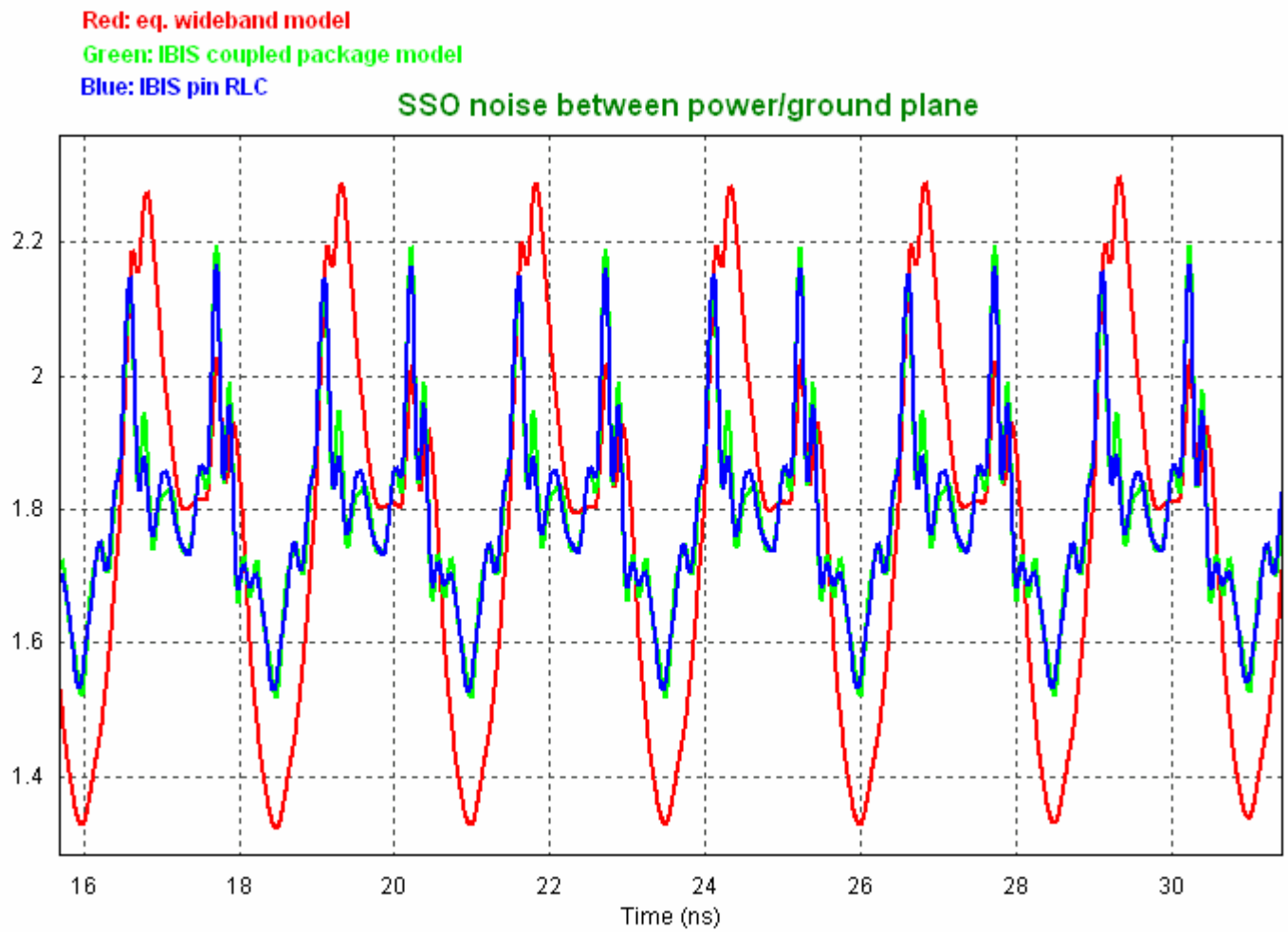


For the 16 driver case, the three package models show significant differences in the results. This is because the package PDS impedance and crosstalk are dominant factors in the overall simulation.

In the simulation results shown thus far, the PCB had excellent characteristics regarding PDS impedance and signal-signal crosstalk. This was purposely done in order to highlight the differences between the package models.

Broadband model yields the largest stuck high noise only.

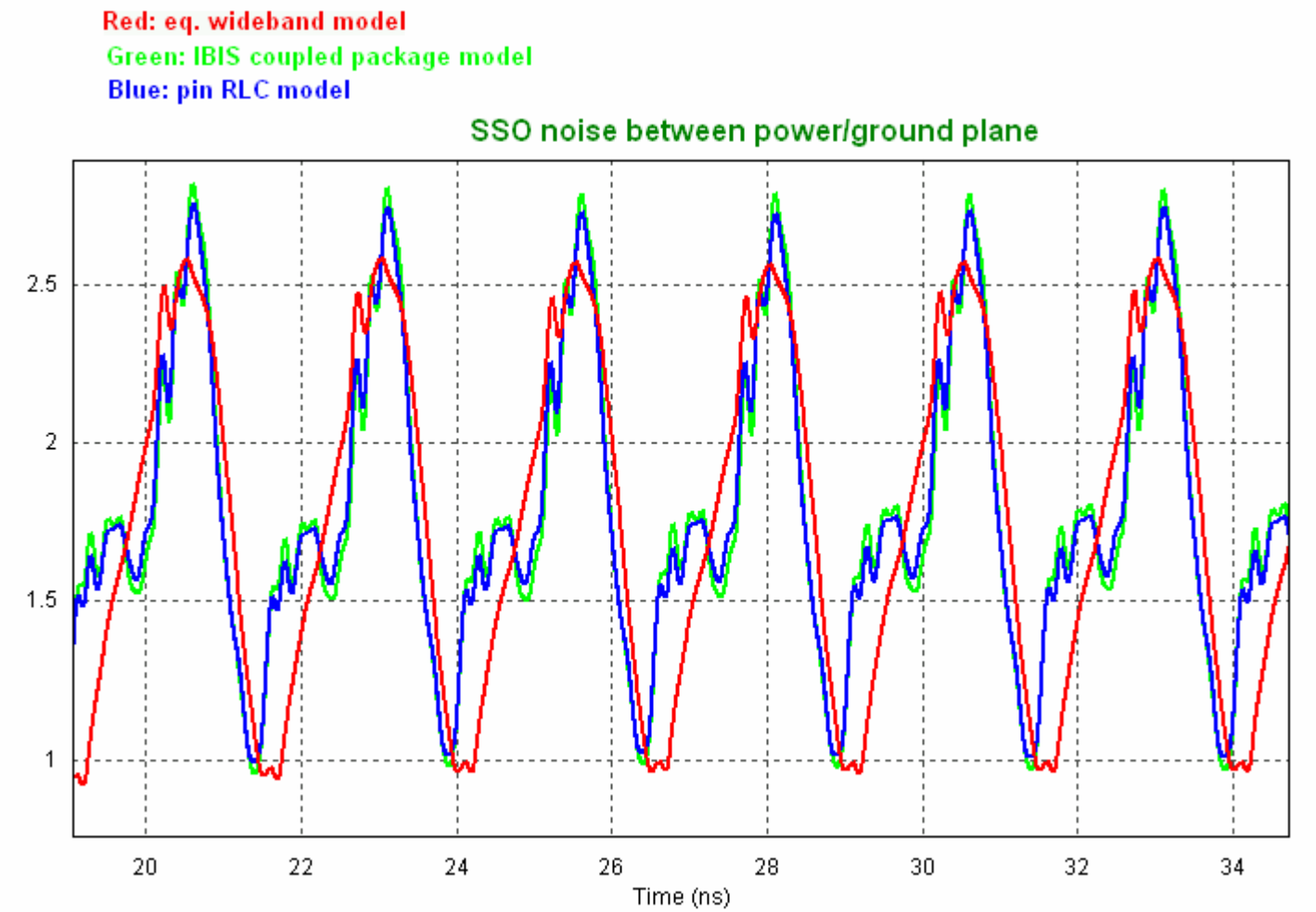
DDRII800 results – PDS Noise for 16 bits Package Impedance is dominant factor



For this case, the package is the dominant factor in the system's PDS impedance (the PCB PDS design is excellent).

Because the IBIS package PDS models are not as accurate as the S-parameter model, the results will typically be quite different in this scenario.

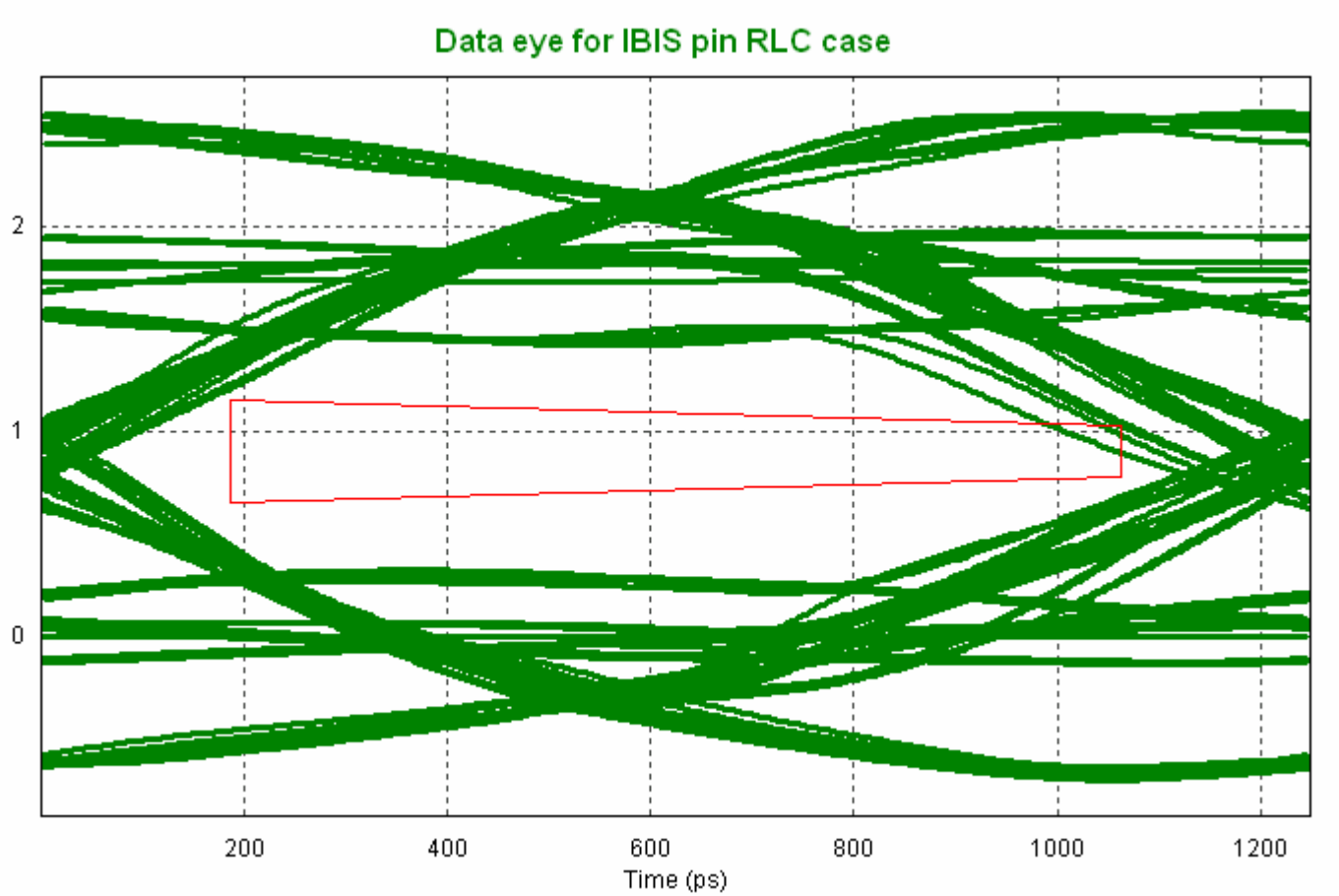
DDRII800 results – PDS Noise for 16 bits PCB Impedance is dominant factor



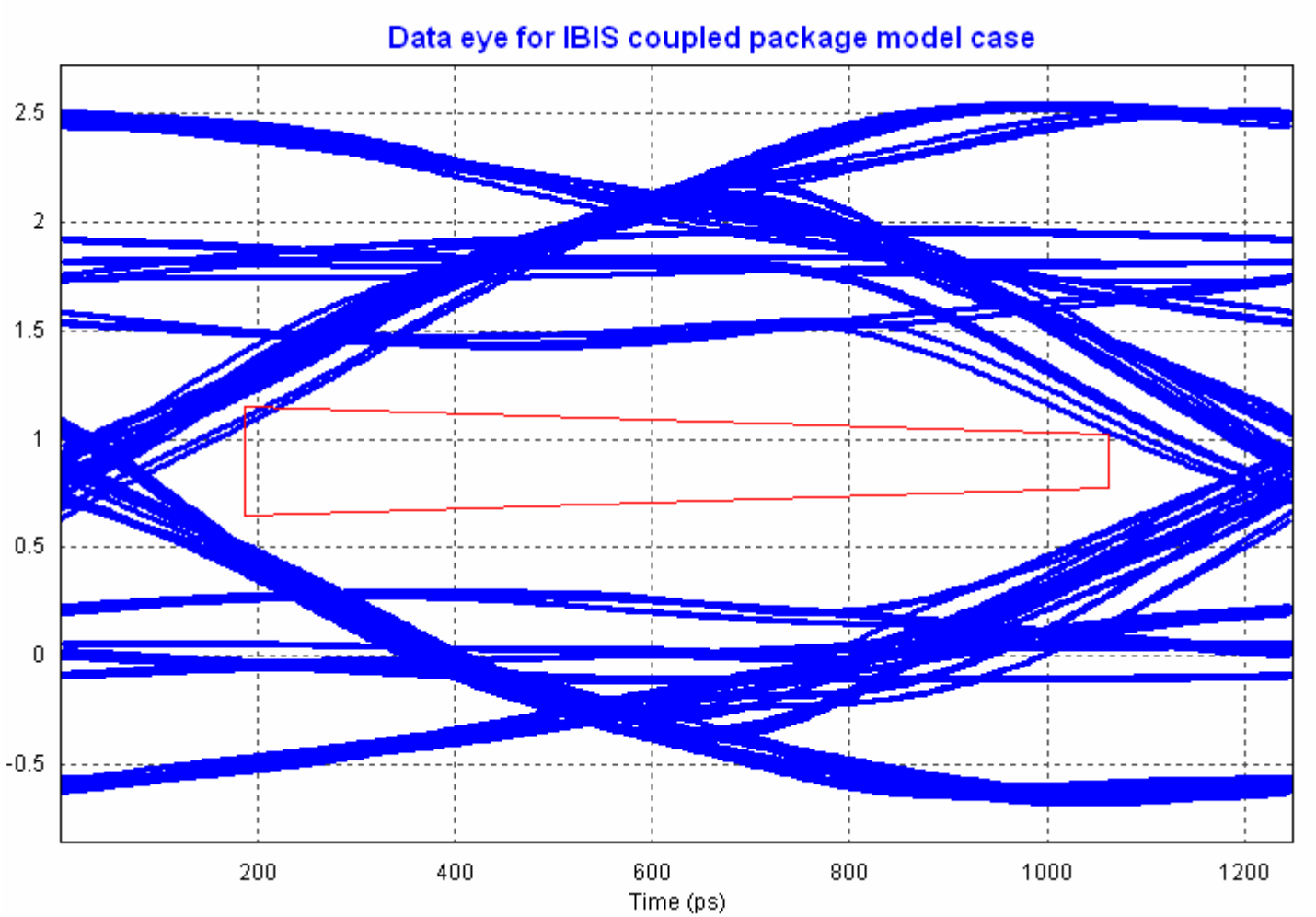
For this case, the PCB is now the dominant factor in the system's PDS impedance.
(The PCB impedance was intentionally degraded by removing some decaps.)

Therefore the choice between the three package models is not as critical and may yield similar results. This facilitates relative study optimization.

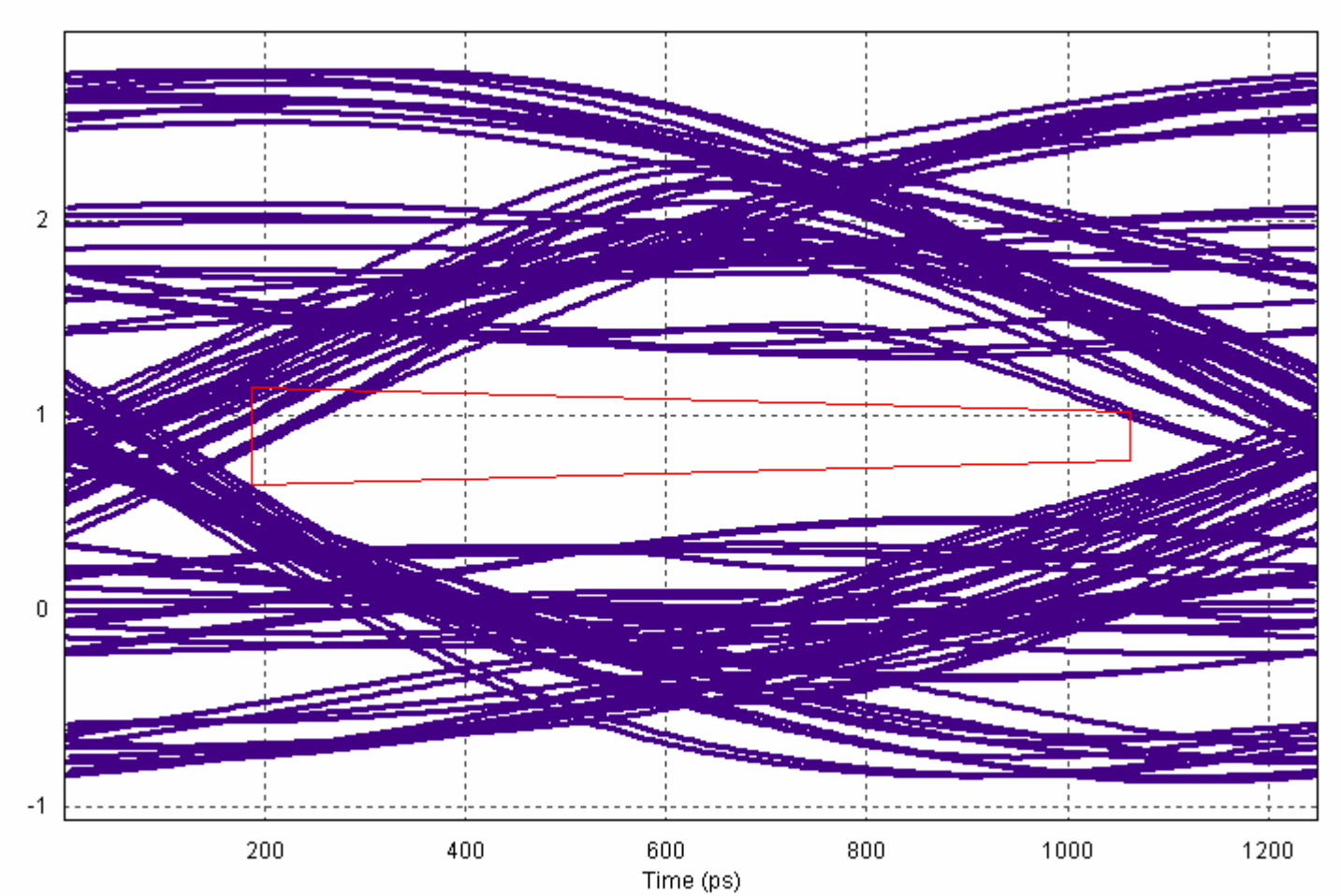
Eye Diagram for DDRII800 IBIS [Pin] RLC model



Eye Diagram for DDRII800 IBIS [Package Model] with coupled RLCs



Eye Diagram for DDRII800 Broadband S-parameter package model



Conclusions and Summary

- SSO noise is generated in circuits through many mechanisms. The primary contributors are 1) the many forms of crosstalk and 2) the impedance and interactions of the package and PCB power distribution systems.
- In full SSO simulations, it is difficult to separate the contribution of these two factors. However, the components can be separated with specially designed simulations that isolate particular effects.
- RLC models can over- or under-estimate the true behavior of the package. The RLC model should be sufficiently accurate over the necessary signal bandwidth.
- [Pin] package models have limited use in SSO simulations since they lack the coupling between the PDS and the signals. They are most appropriate for ideal PDS simulations.
- [Package Model] is very appropriate for SSO trend studies and “what-if” analysis.
- S-parameter package models are most appropriate for highly accurate SSO sign-off.
- The package may or may not be the dominant factor in system-level SSO analysis. If the package [Pin] model is the only model available, relative PCB optimization studies can still be performed.

Thank You!

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