Methodologies for Multi-Gigabit Interconnect Design
千兆比特高速互联设计

Andrew Byers, Application Engineer, abyers@ansoft.com
Lawrence Williams, Director Business Development, williams@ansoft.com

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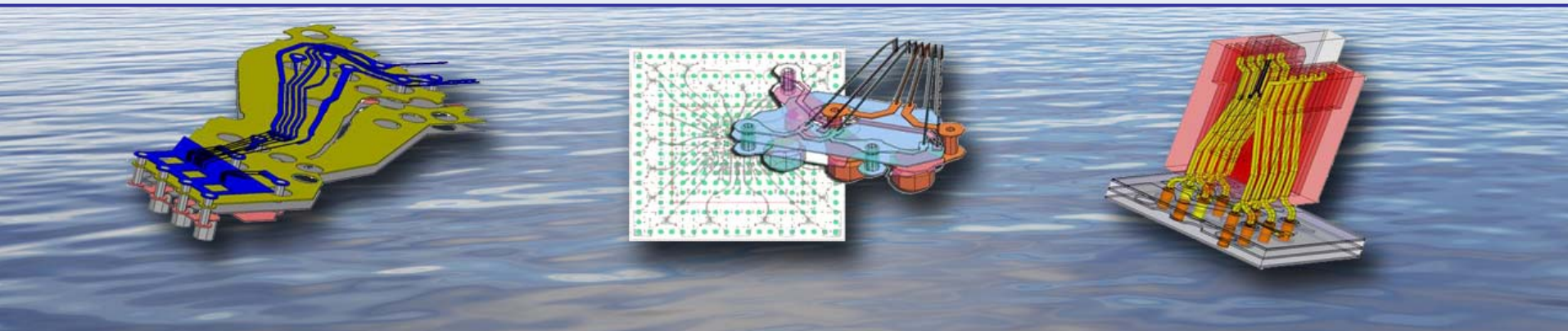
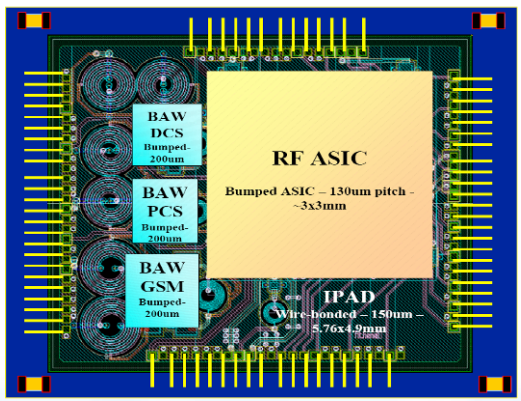


Multi-gigabit Devices

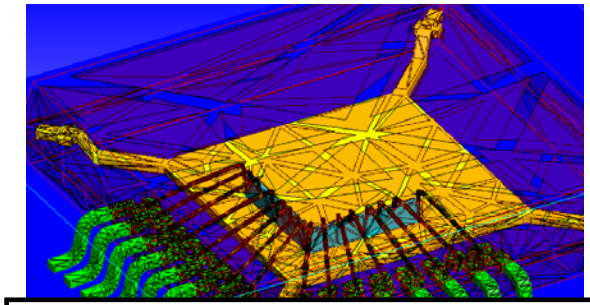
- The need for devices that are smaller and faster is driving multi-gigabit applications in several industries.
- *电子产品的高速、小型化趋势极大促进了千兆比特高速通信的应用*
- Slower parallel busses are being replaced by much faster serial busses (eg. PCIExpress, SATA, FBDIMM).
- *高速串行通信正逐渐替代低速并行总线方式得到更广泛的应用*
- Faster data speeds present a new set of challenges for signal and power integrity. ***New tools and methodologies are needed.***
- *必须采用全新的设计工具和设计方法才能应对新的信号及电源完整性设计挑战，进而满足高速数据通信设计要求*



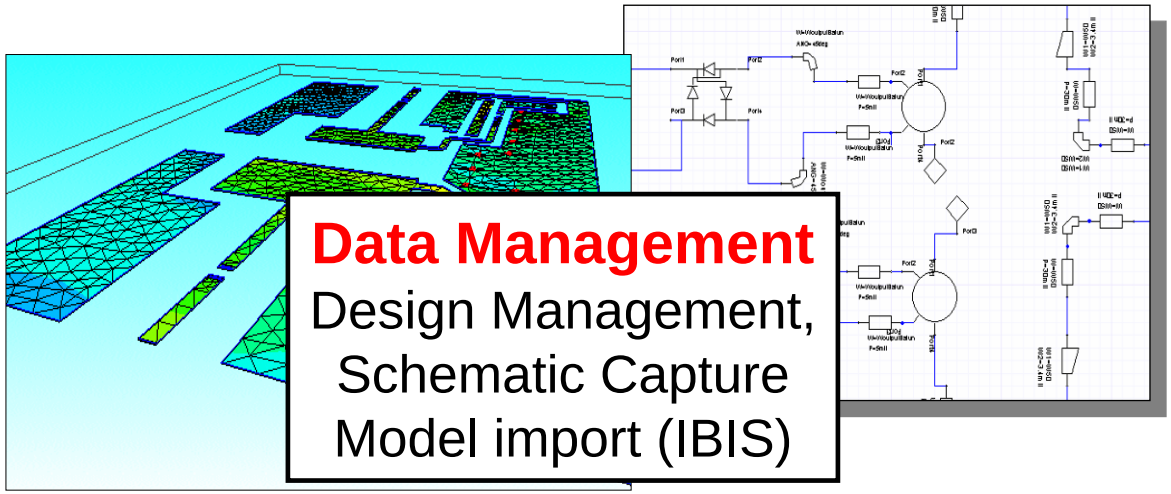
Multi-gigabit Design Challenges

- Before engineering teams can make it smaller, faster or better performing they require design strategies and tools that can:
  - **Extract** GHz-accurate signal path models based on the entire physical interconnect.
  - **Simulate** and optimize the performance of these high speed data lanes in time and frequency.
  - **Validate** the overall system performance, incorporating **IBIS** and/or transistor-level representation of critical components

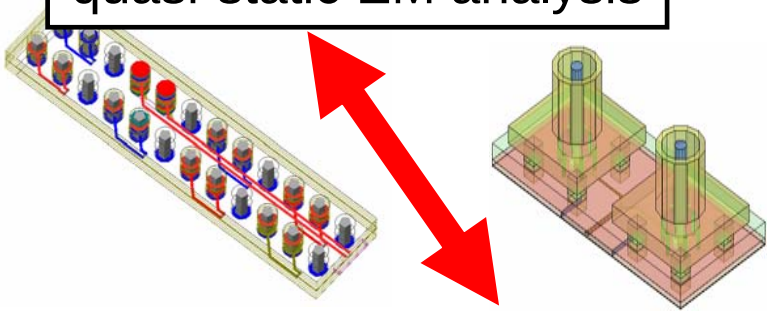
Electromagnetic modeling for Multi-gigabit Channel Design



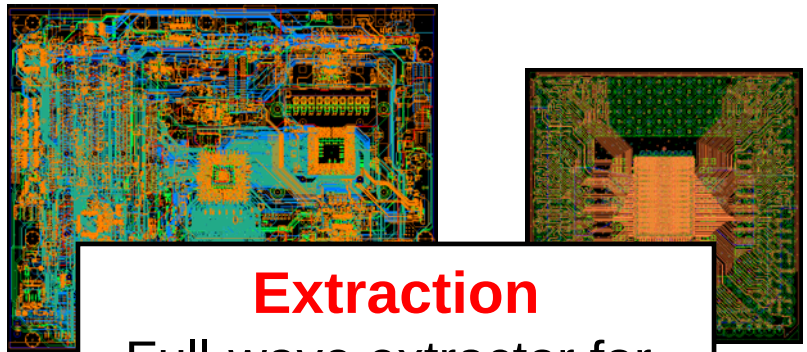
Extraction
3D Full-wave and quasi-static EM analysis



Data Management
Design Management, Schematic Capture Model import (IBIS)



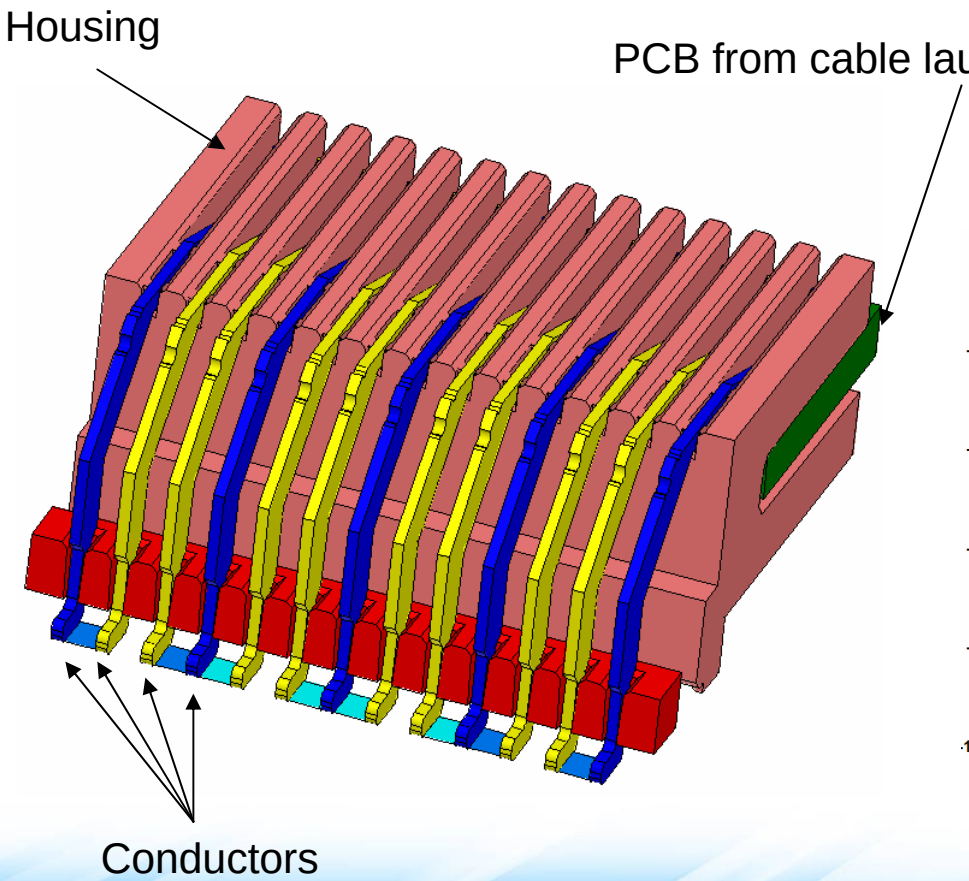
Circuit Simulation
High capacity and accuracy, Time and frequency domains



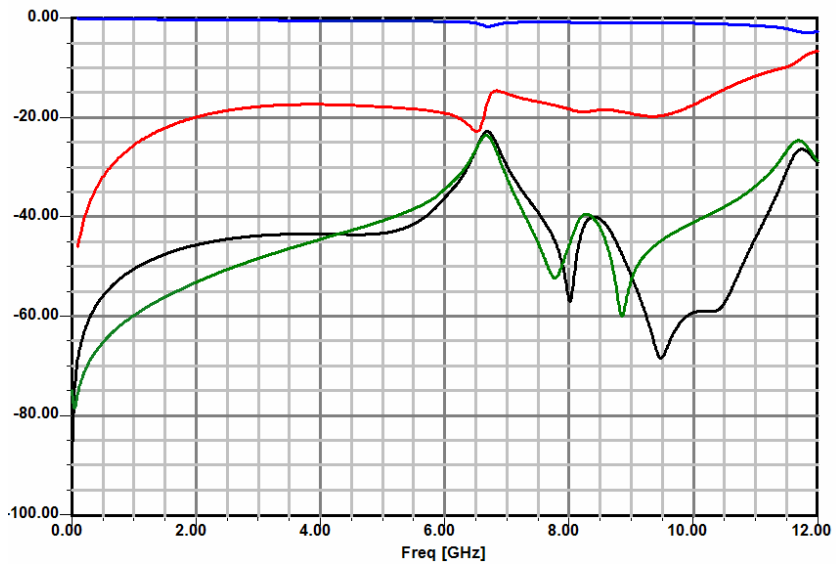
Extraction
Full-wave extractor for entire package and PCB

Simulation Requirements (仿真要求)

- 3D interconnect components should be modeled using full-wave electromagnetic solvers that produce S-parameters.
- 必须采用全波电磁场技术对3D互联结构进行建模，并抽取S参数

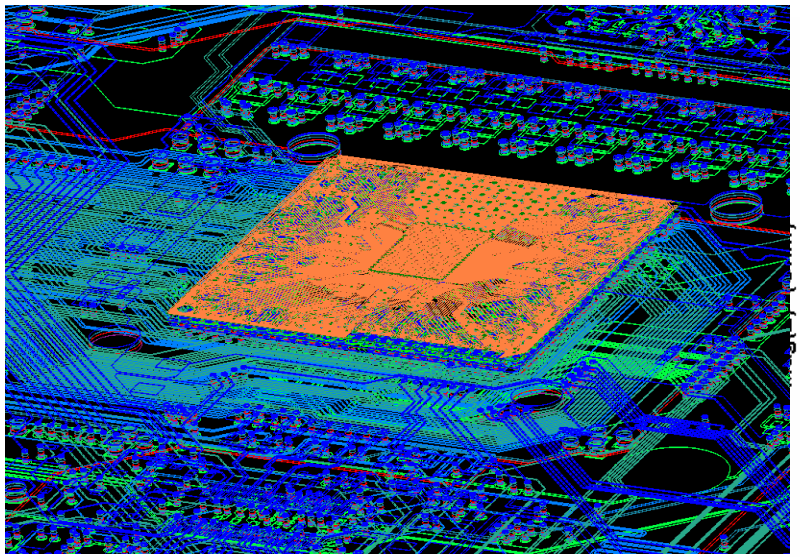


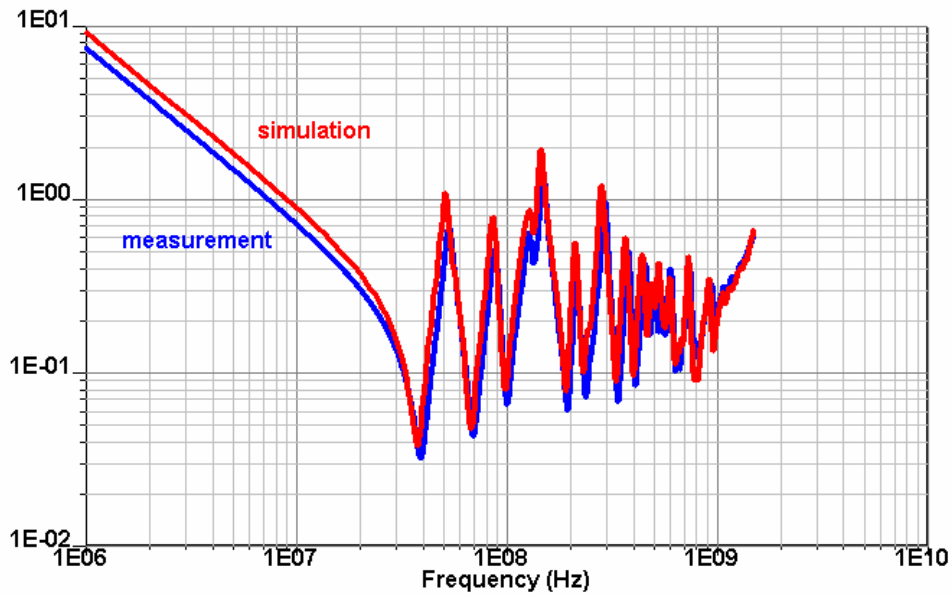
S-parameters for Connector



Simulation Requirements (仿真要求)

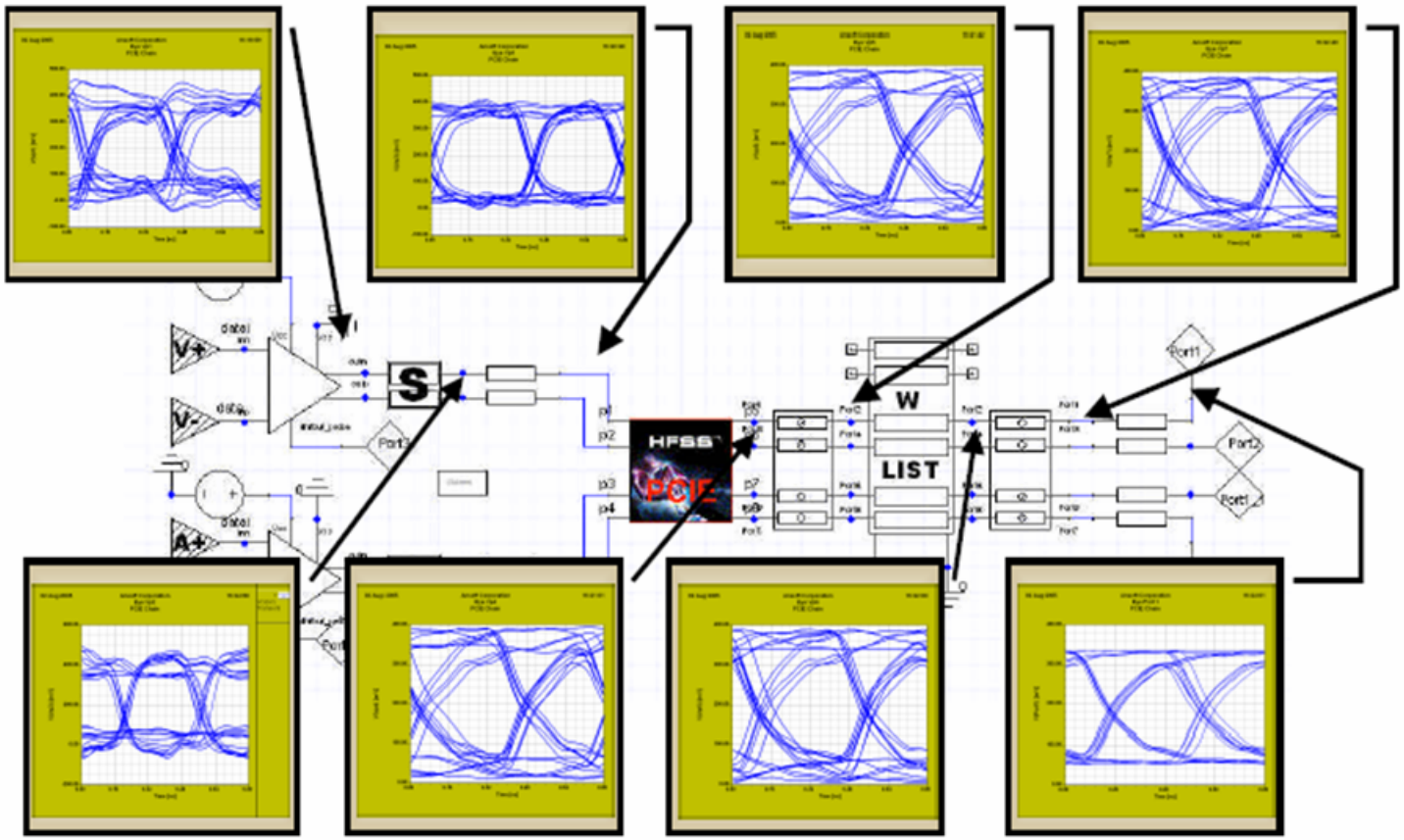
- Multi-gigabit backplanes must meet complex power-delivery requirements, and simulation tools are needed to verify designs before tapeout.
- 千兆比特电路板要求进行复杂供电系统设计，并在制板前进行仿真验证





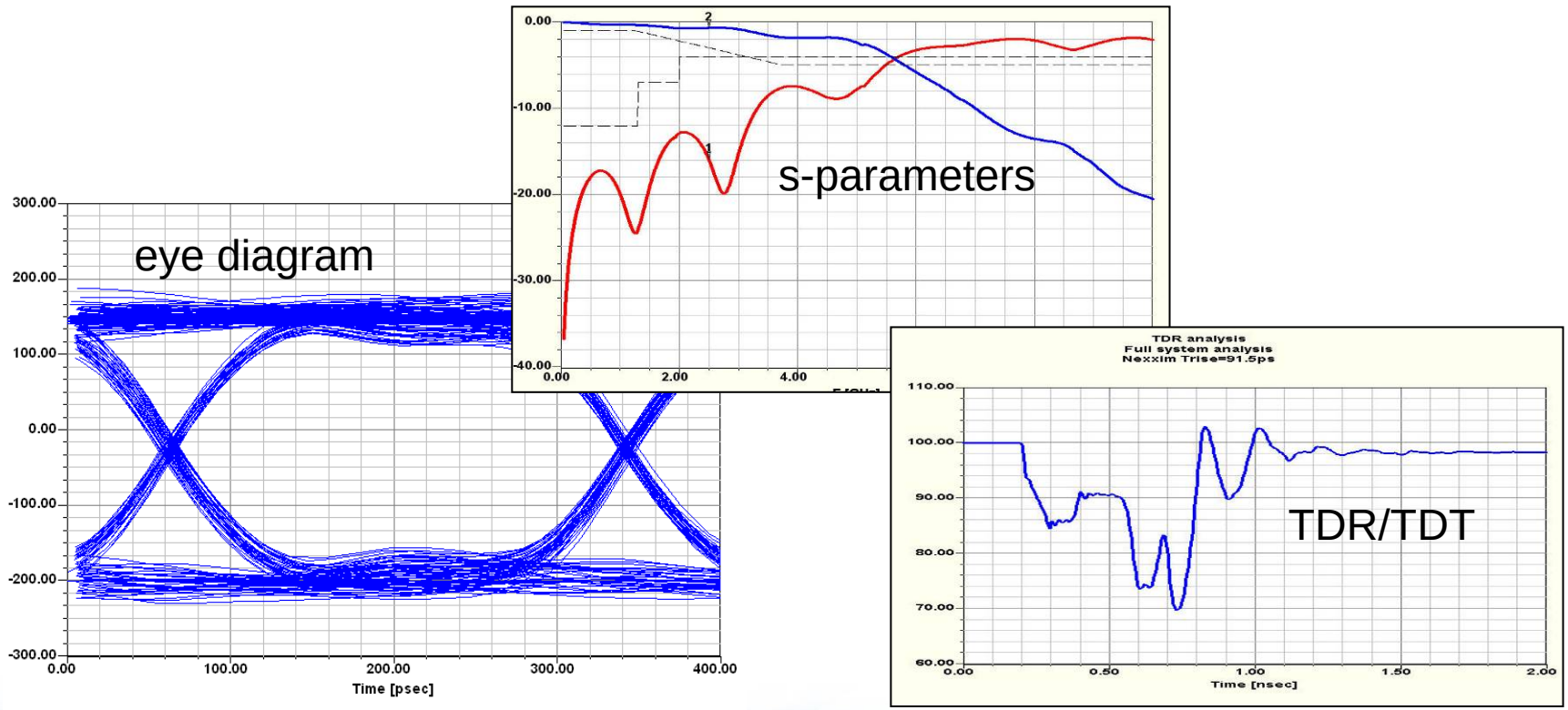
Simulation Requirements (仿真要求)

- Simulator must provide reliability and capacity by correctly including S-parameters along with other model types in transient simulations of channel.
- 功能强大的仿真器，对包括S参数及其他模型在内的完整信号通道提供精确、可靠的时域仿真结果。



Simulation Requirements (仿真要求)

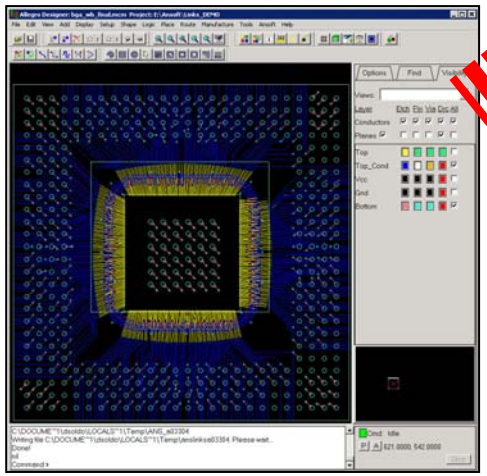
- Multi-gigabit channel designs require both frequency- and time-domain simulations to meet required specifications.
- 千兆比特信道设计要求兼具频域和时域的仿真功能，从而确保满足设计要求



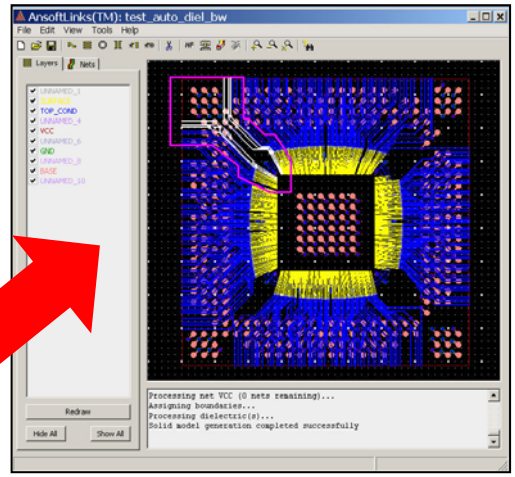
Simulation Requirements (仿真要求)

- Ability to transfer data from layout programs to EM extraction tool.
- 自动将布线信息转换到电磁场建模工具中

Cadence Advanced Package Designer (APD)

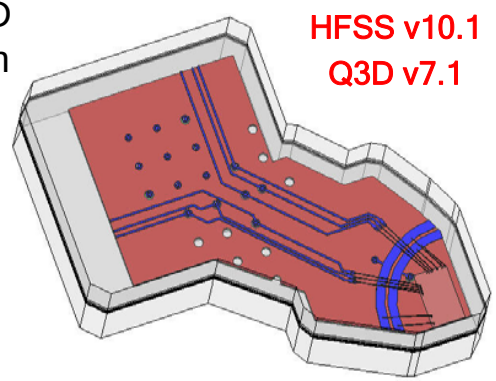


AnsoftLinks v4.0

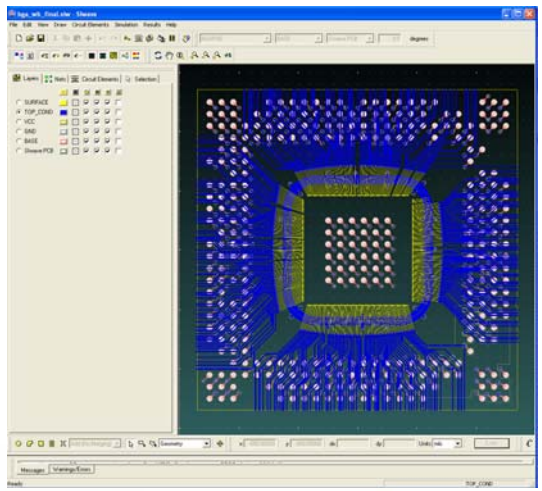


full-wave 3D EM Solution

HFSS v10.1
Q3D v7.1



full-wave 2D EM Package/PCB SI/PI Solution

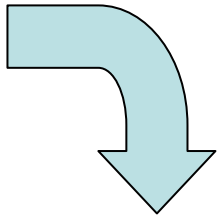


SIwave v3.1

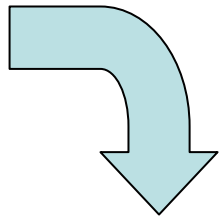
Phases of Interconnect Design

互联设计步骤

Phase 1: Feasibility
(*可能性*)
Which technologies to use?
First-pass SI and PI designs

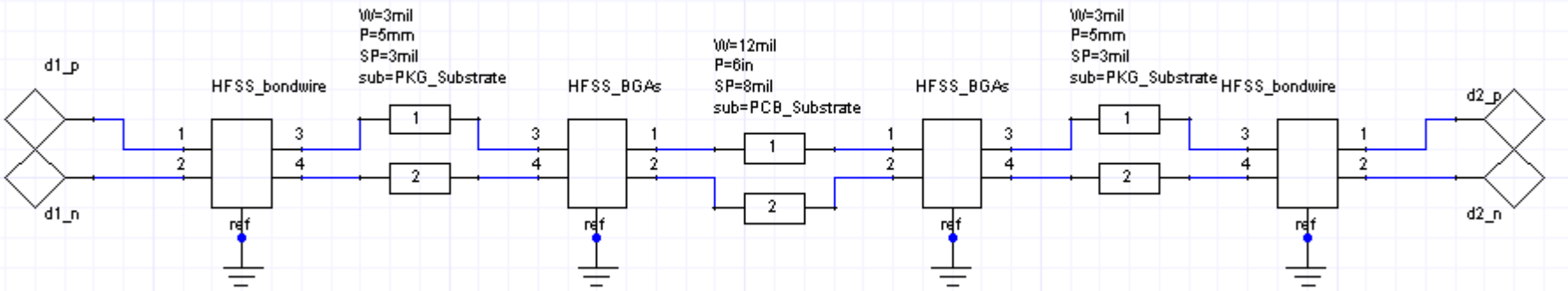


Phase 2: Design
(*设计*)
SI and PI optimization
Refinements to interconnect channel
Detailed simulations with IBIS buffer models



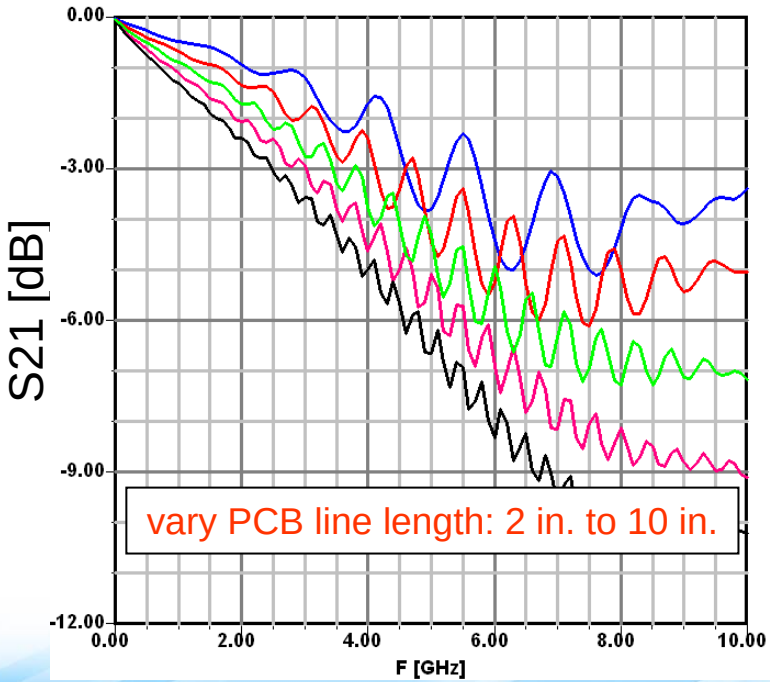
Phase 3: Validation
(*验证*)
Layouts completed
Extract critical nets – validate SI and PI
SSO simulations to check jitter specs

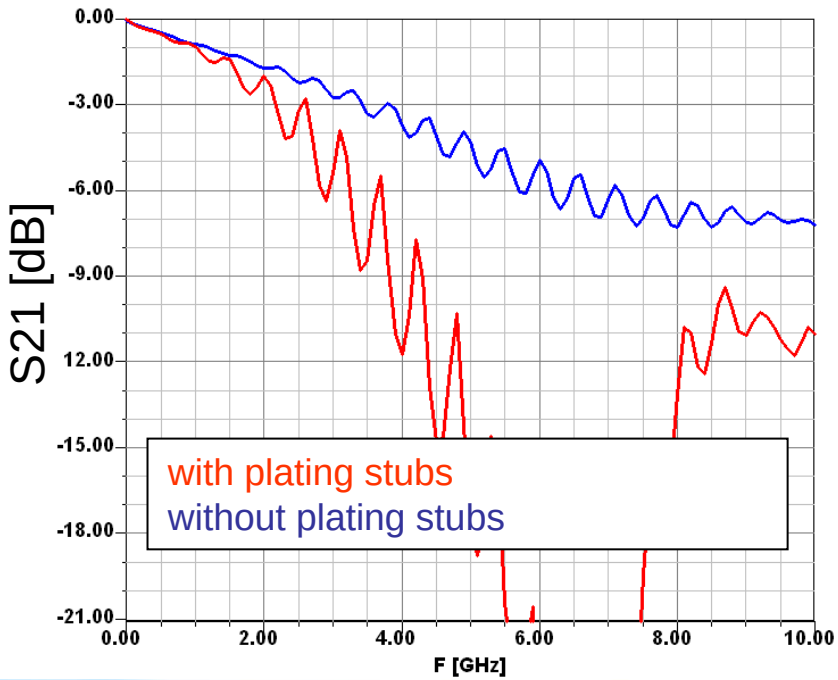
Phase 1: Feasibility



Explore Design Space

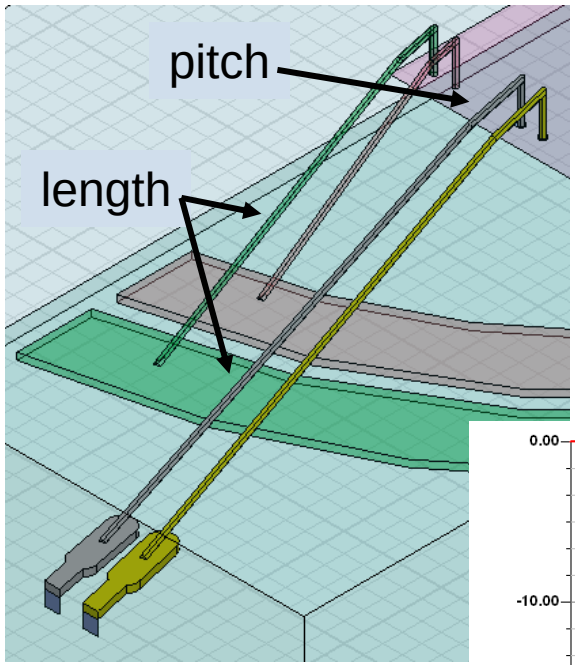
Investigate Technology Choices





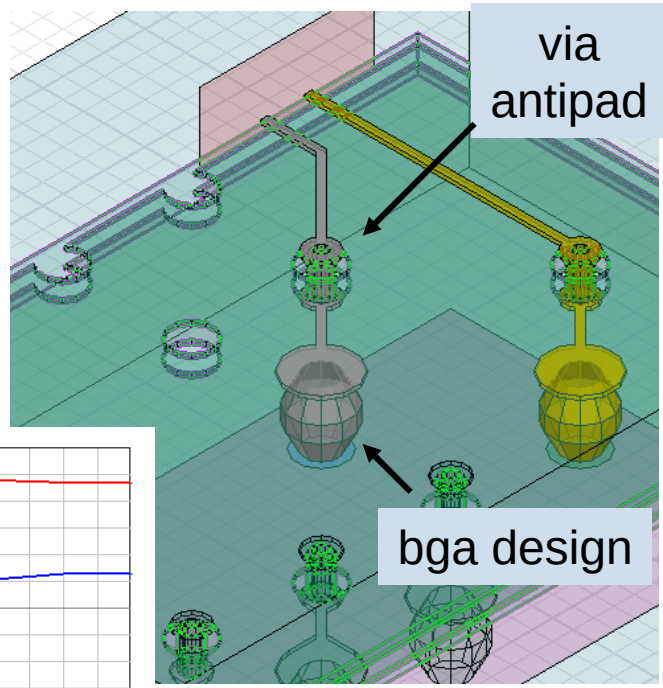
Phase 2: Design

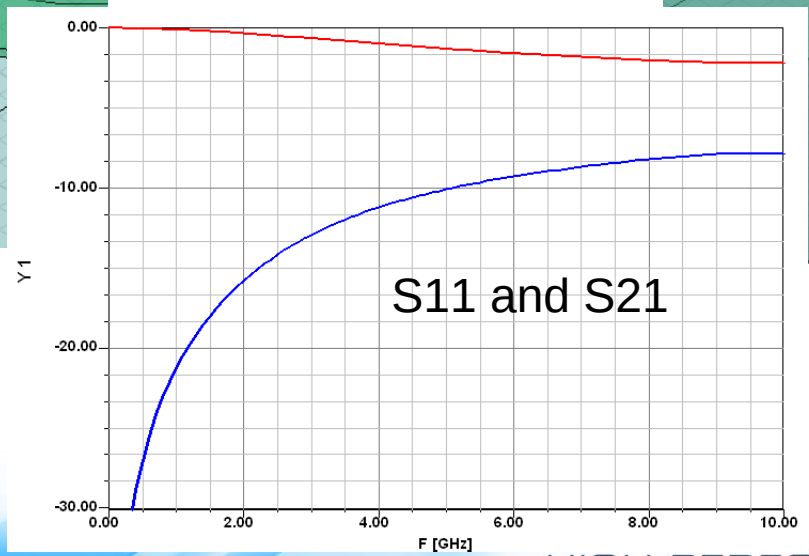
Optimize designs of the interconnect components of the multi-gigabit channel.



“virtual prototyping”

[“虚拟原型”]

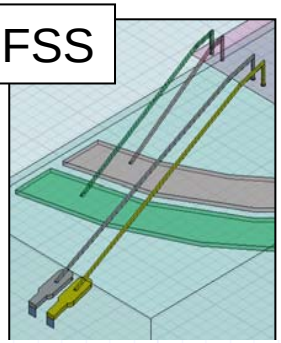




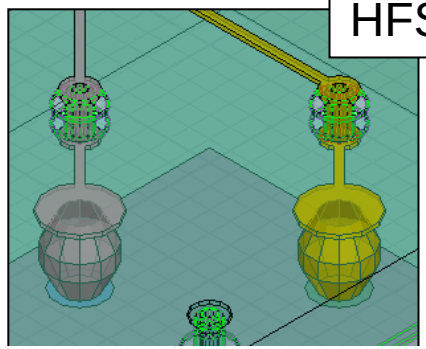
Phase 2: Design

Transient simulation of the channel with IBIS drivers.
仿真包括IBIS模型在内的整个信号通道的时域特性

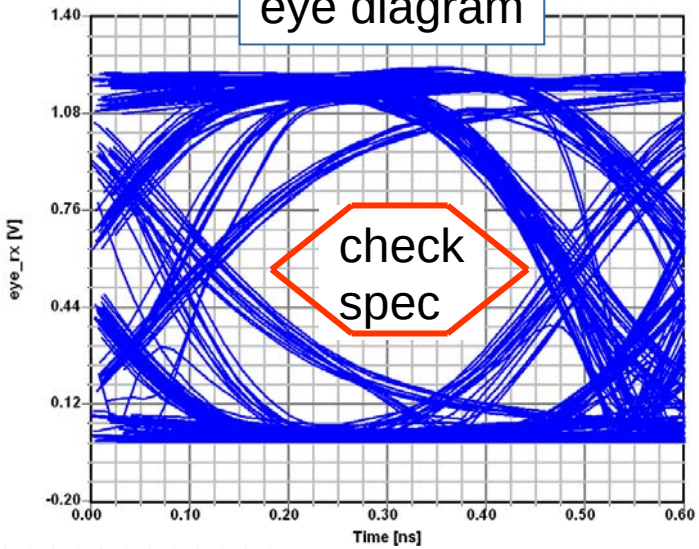
HFSS

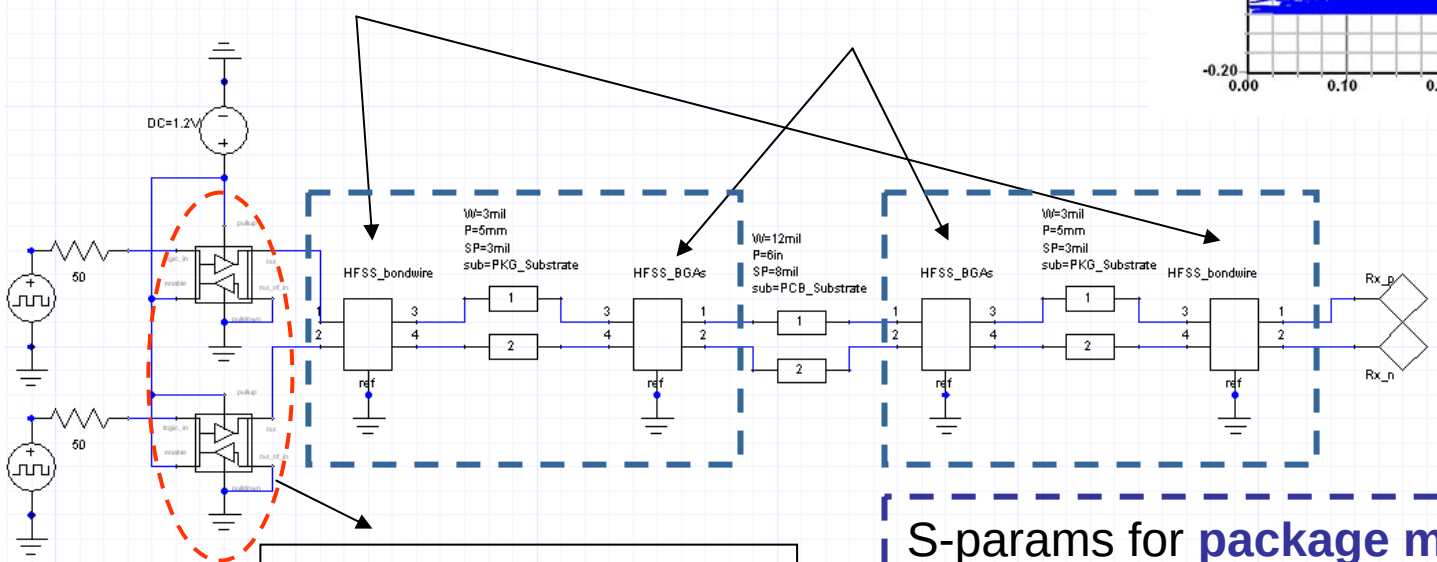


HFSS



eye diagram





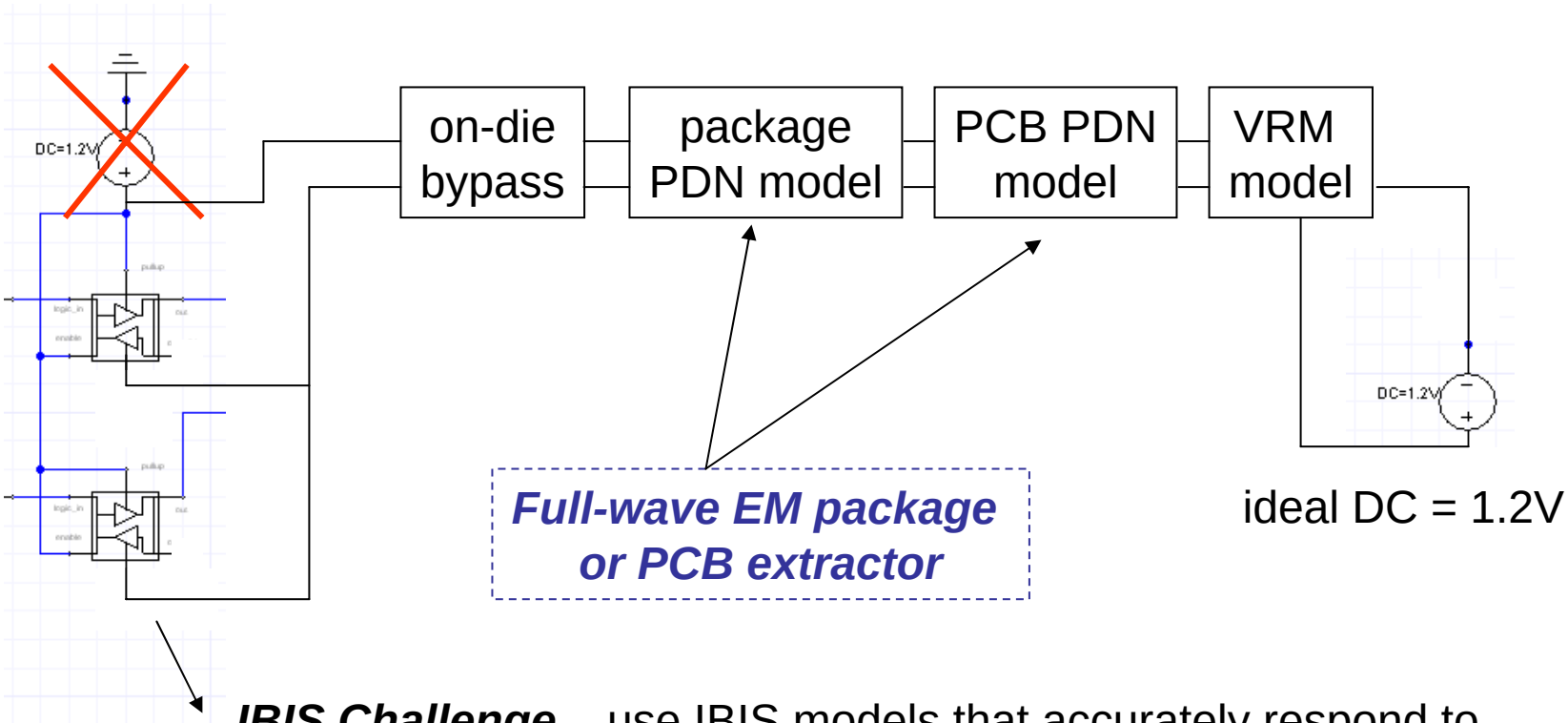
IBIS v4.0 driver models

S-params for **package model** may be included in ***ICM file***

Phase 2: Design

For more realistic design – also include ***Power Distribution Model (PDN)***

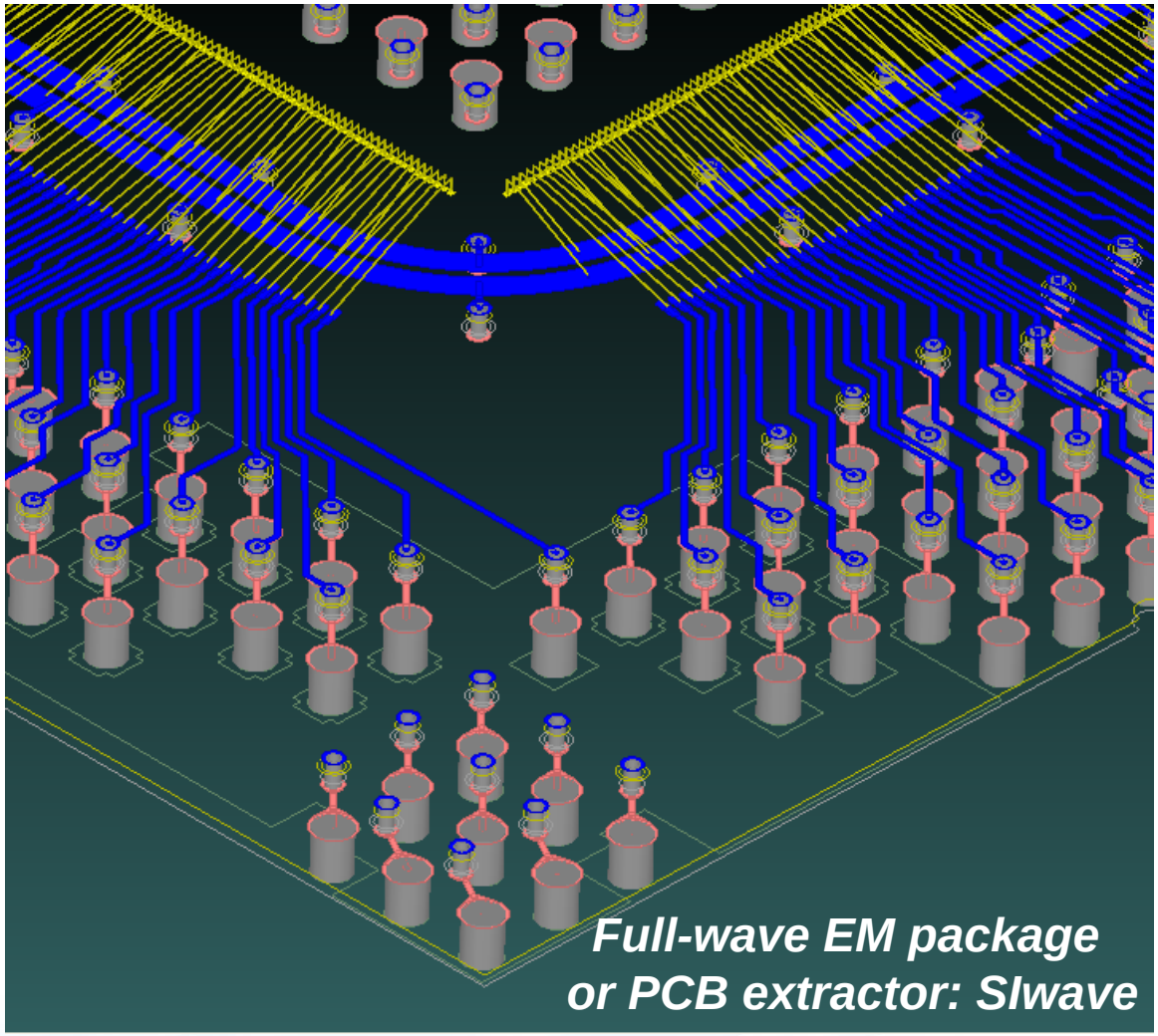
在更多的实际设计中必须精确考虑**PDN**系统的影响



IBIS Challenge – use IBIS models that accurately respond to noise on power rail caused by dI/dt effect.

如何用**IBIS**精确模拟由于瞬态电流变化导致的电源噪声影响

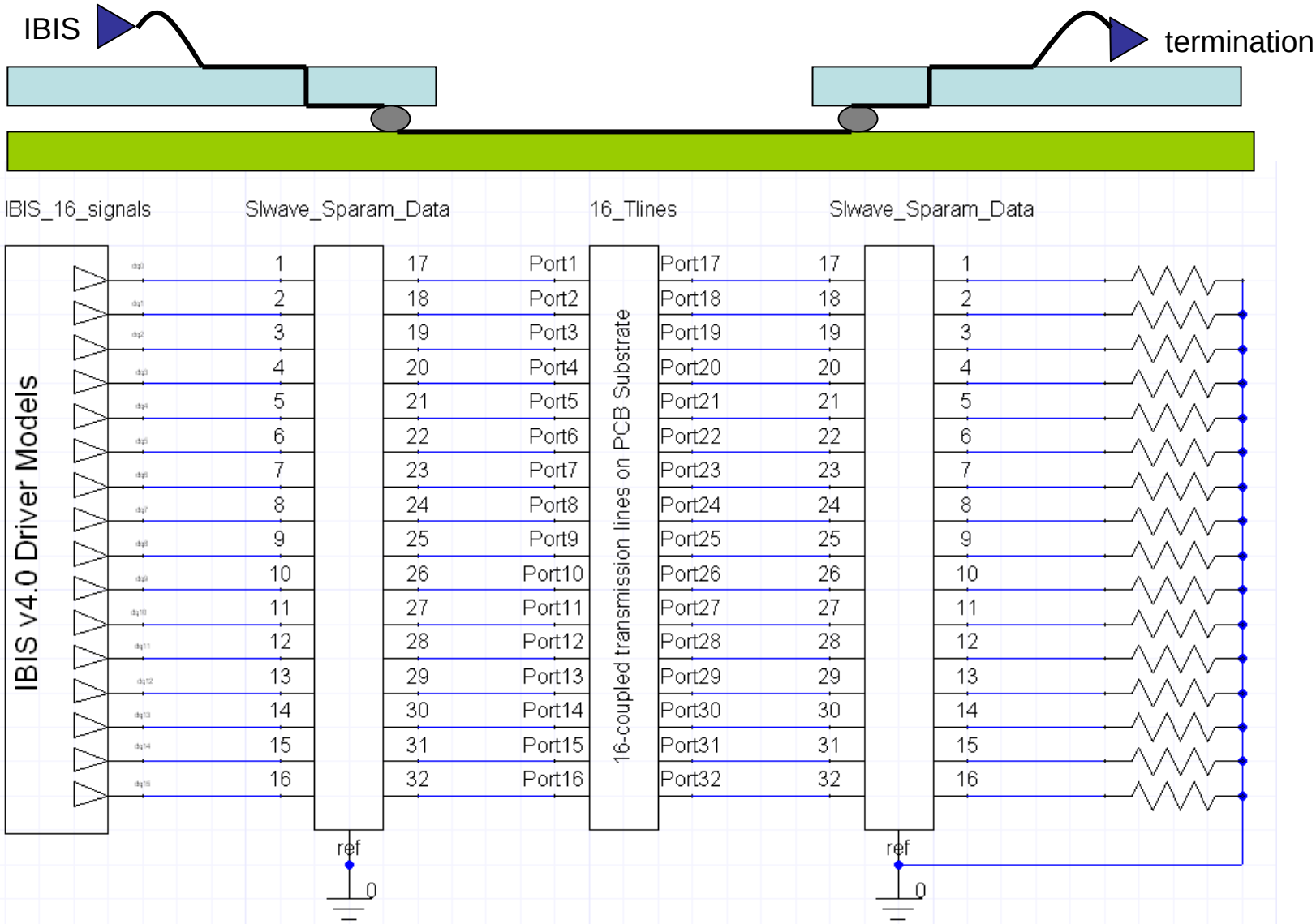
Phase 3: Validation



Look at more nets, including any impact of crosstalk and other post-layout design issues.

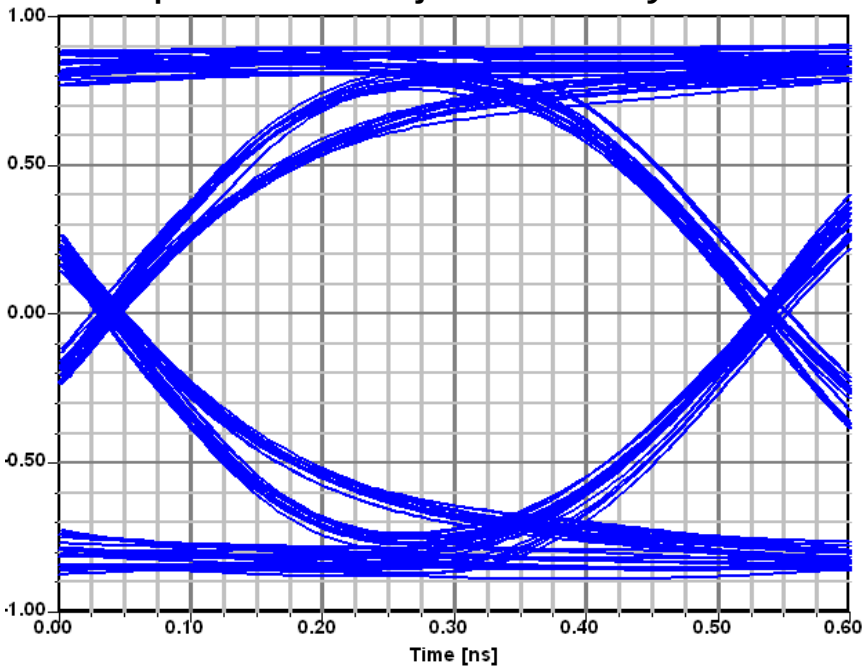
16-channel, 32-port S-parameter File

Phase 3: Validation

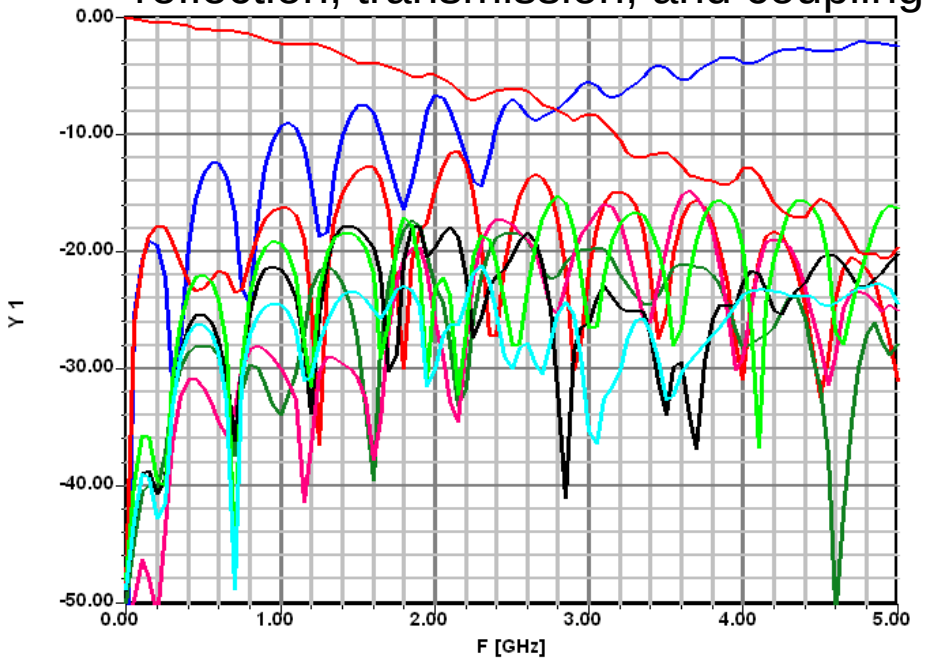


Phase 3: Validation

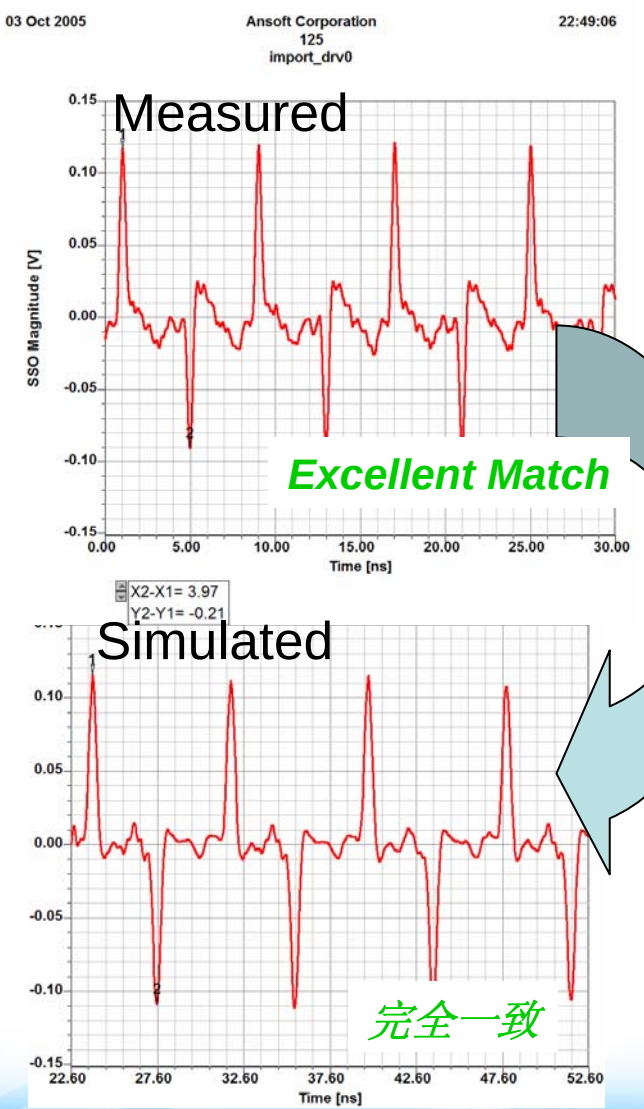
Time-domain:
Inspect eye opening for spec qualification, jitter, fidelity.

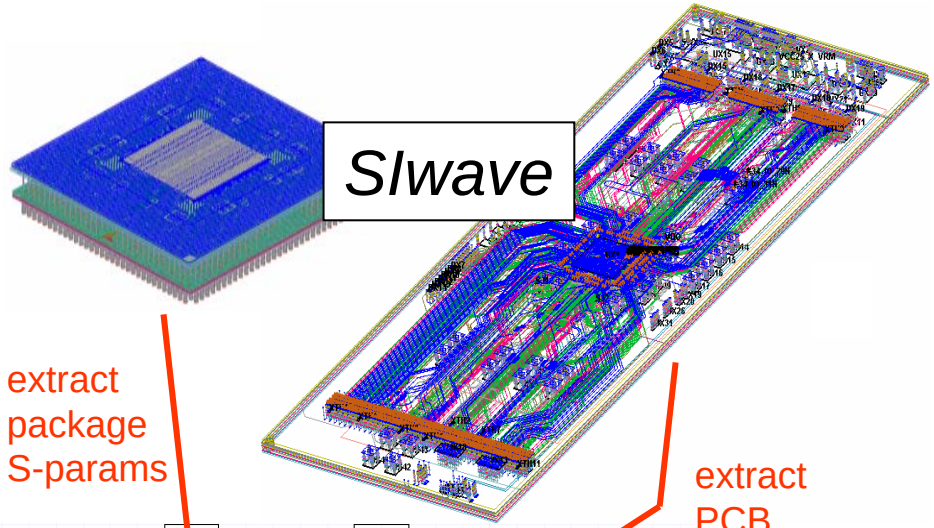


Frequency-domain:
inspect channel s-parameters for reflection, transmission, and coupling.



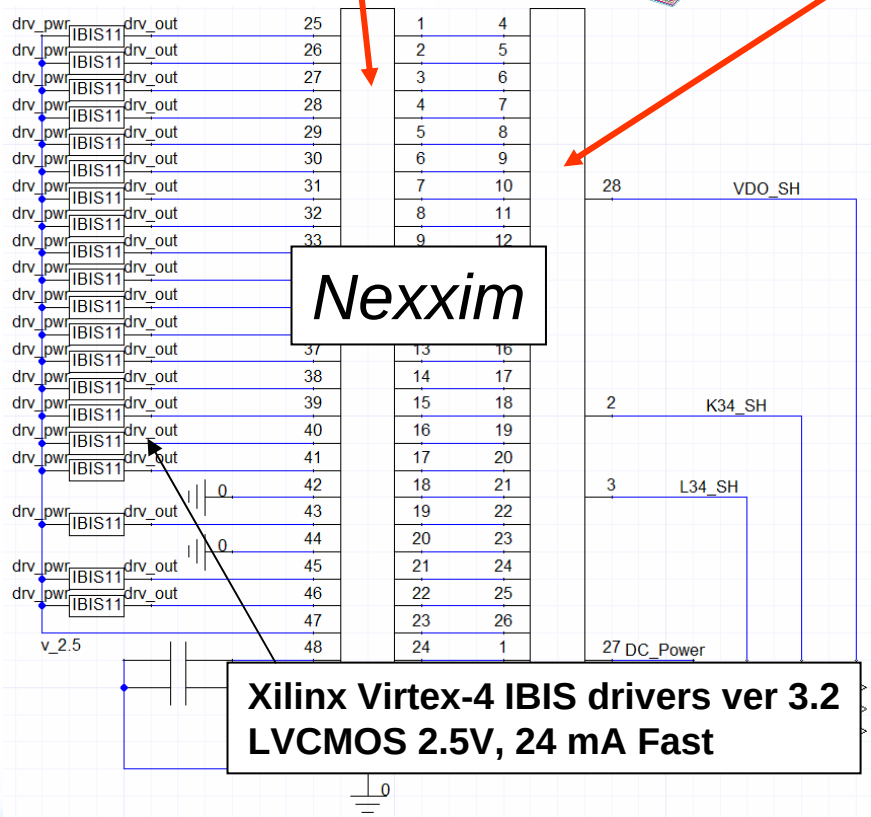
Customer Case Study





extract
package
S-params

extract
PCB
S-params



Summary

- Electromagnetic-based modeling tools play a critical role in multi-gigabit channel design.
- 基于电磁场技术的建模工具在千兆比特高速信道设计中极其重要

- The inclusion of S-parameters in IBIS models will open up higher bandwidths for signal integrity and provide complete SSN analyses for power integrity.
- IBIS模型与S参数结合将进一步拓展其在更高频段信号完整性上的应用，并提供全面的SSN分析用于电源完整性设计

- Thank you very much!