WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Open Forum, I would like to welcome you, our presenters and guests, to our second annual IBIS Summit in China.

Members of the worldwide IBIS community were greeted in China with great hospitality during our first summit last year. The large number of attendees and the high level of technical discussions made clear that China will contribute much to the development of behavioral modeling and related technologies. We know that this year's event will be just as enlightening and fruitful.

As always, we appreciate the generous support of our sponsors Huawei Technologies, Ansoft Corporation, Cadence Design Systems, Intel Corporation, Mentor Graphics Corporation, Signal Integrity Software (SiSoft), Sigrity and Synopsys. Their efforts made this event possible.

Once again, thanks to you for your participation and best wishes for an enjoyable summit.

Sincerely,
Michael Mirmak
Chair, EIA IBIS Open Forum

我代表 IBIS 委员会，欢迎各位演讲者和嘉宾参加在中国举办的第二次 IBIS 峰会。

在第一次 IBIS 峰会期间, 来自全球的 IBIS 委员会成员受到中国方面热情的接待。这次会议，参加人数的增多和研讨水平的增高使我们清楚的看到，中国会对行为级模型和相关技术的发展有更大的贡献。我们知道今年的会议将很成功。

一如以往, 我们特别感谢我们的赞助方：华为公司、Ansoft 公司、Cadence Design Systems 公司、英特尔公司、Mentor Graphics 公司、Signal Integrity Software (SiSoft) 公司、Sigrity 公司和 Synopsys 公司。没有他们，这次会议不可能顺利召开。

再次感谢所有到会人员，祝本次会议成功召开.

迈克尔 莫马克
IBIS 委员会主席

WELCOME FROM JIANG XIANGZHONG, HUAWEI TECHNOLOGIES

Dear Experts, Ladies and Gentlemen,

Good Morning

Last year's IBIS Asian Summit in China was a very successful start. This year, not only are attendance, paper quality and quantity increased, but also more companies are joining as sponsors.

Best wish to this IBIS Asian Summit for the greater success this year.

Jiang XiangZhong
Huawei Technologies

各位专家，各位来宾，

大家好。

去年 IBIS 在中国有一个非常成功的开端，今年的会议在来宾人数、文章数量质量都增加了，赞助公司也增加了。

祝愿今年的会议能开办得更成功。

华为公司 姜向中

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open

9:00 Introductions and Program Overview
- Welcome, Jiang, XiangZhong, (Huawei Technologies, China)
- Welcome to Summit, Mirmak, Michael (Intel Corporation, USA)
- Welcoming Comments, Invited Chinese Leader/Speaker (China)

9:30 **The Direction of IBIS as a Standard 5**
Mirmak, Michael (Intel Corporation, USA)

9:45 **IBIS Model Validation Report 10**
Zheng, Qi (Fiberhome Telecommunications Technology, China)

10:15 BREAK (Refreshments)

10:30 **IBIS Model Engineering for SI Analysis 17**
Kusunoki, Kazuhiko (Cybernet Systems, Japan)

11:00 **Case Study: Spice Macromodeling for PCI Express Using . . 27 IBIS 4.2**
Wang, Lance (Cadence Design Systems)

11:30 **System-Level Timing Closure Using IBIS Models 43**
Katz, Barry (Signal Integrity Software (SiSoft), USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

12:00 - 12:45 Press Conference for IBIS Officers and Sponsors

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

The Direction of IBIS as a Standard

Michael Mirmak
Intel Corporation
Chair, EIA IBIS Open Forum

IBIS Summit
Shanghai, China
October 27, 2006

马梦宽
英特尔公司
IBIS 委员会主席

亚洲 IBIS 技术研讨会
中国上海
2006 年 10 月 27 日

1

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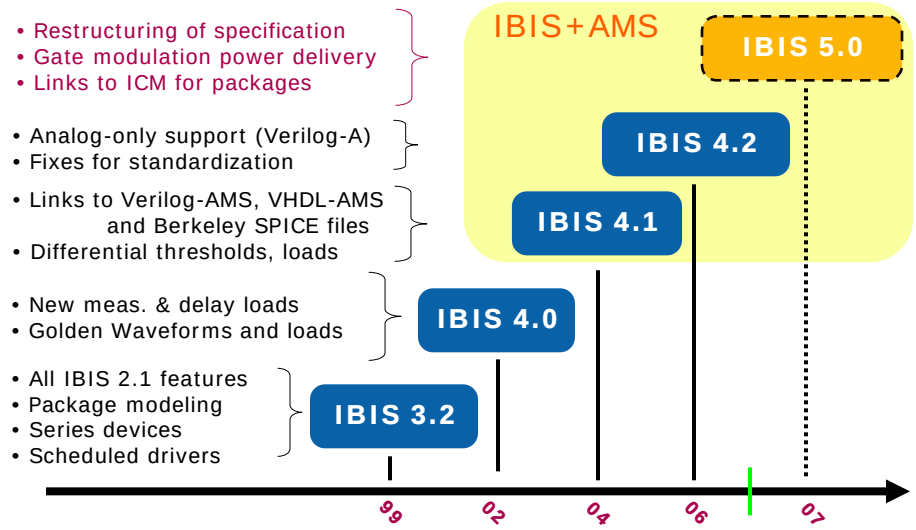
IBIS Development



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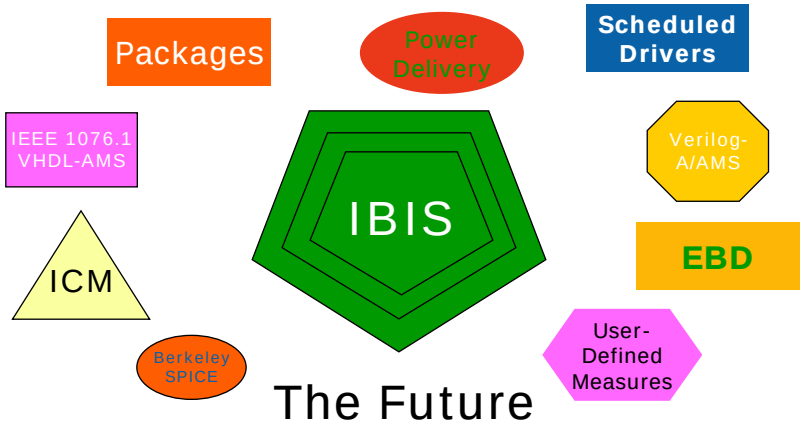
The Expansion of IBIS



The Future

To support new circuit design technologies, IBIS has grown and will continue to grow

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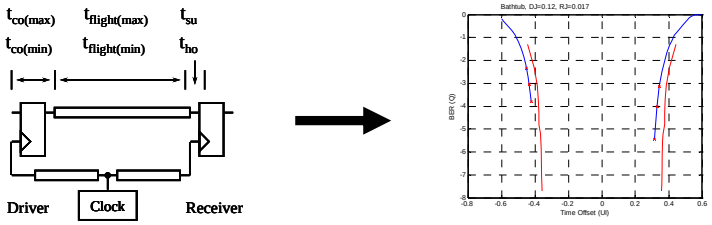
Industry Needs Are Changing Again

- Today's IBIS Technology Enables Today's Analysis Methods
  - *Single-ended, source-synchronous interfaces slower than 1 GHz*
  - *Setup and hold timing equations using pin measurements*
  - *Worst-case corners analyzed using a few hundred or thousand bits*
  - *Tools process analog waveform data taken at pins, pads*
- Newer Technologies Suggest New Techniques
  - *Differential, low-swing interfaces at 1 GHz and above*
  - *Eye diagram and statistical, BER analyses using 1e5, 1e6+ bits*
  - *Response of entire channel is often analyzed as a unit*
  - *Models are usually linear and may even support digital logic*



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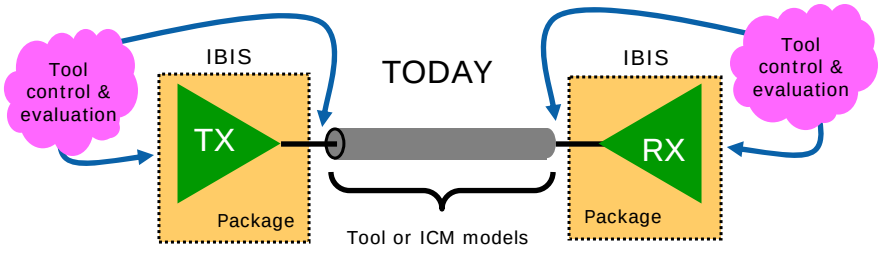
How Do We Support the New Methods?

- A new discussion in the IBIS Advanced Technology Modeling group
  - *Expand IBIS to include an API (application programming interface)*
  - *The API would link to external C code for signal processing analysis*
  - *Example: clock data recovery and bit-error rate (BER) estimation*
  - *Similar effort underway in VHDL (IEEE 1076c)*
- This would expand IBIS beyond circuits into systems



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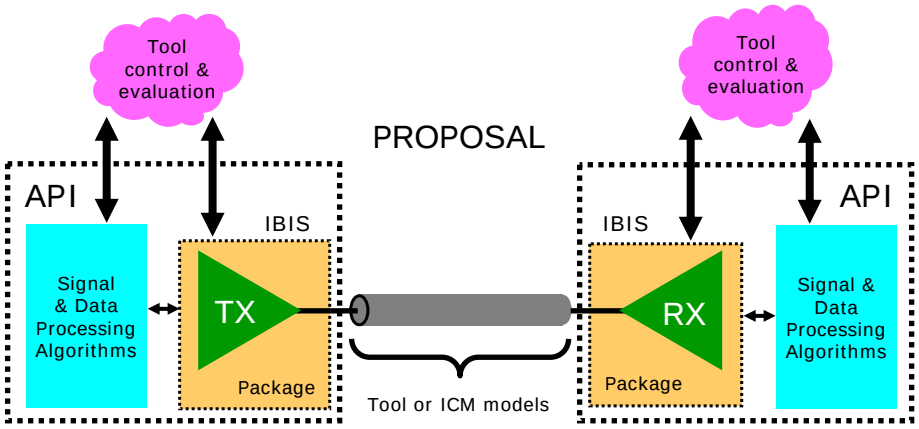
How Do We Support the New Methods?



Critical Choices

- Should IBIS remain a circuit analysis standard or expand to systems?
  - *– Would creating a new specification be more appropriate?*
- Is an API needed?
  - *– AMS languages under IBIS can support complex equations*
  - *– Can the AMS languages handle these new analysis needs?*
- Where should the "model" end and the "tool" begin?
  - *– Both AMS and an API would allow analysis procedures inside a model*
  - *– Should models include both circuit functions and tool functions?*
  - *– Example: tool or model API/AMS code could handle BER estimation*

This issue will be discussed at this Summit and arises frequently in the IBIS community.

Your opinion matters!

References

- Official IBIS Website, including tools, articles, IBIS & ICM specs
  - http://www.eigroup.org/ibis/
- The IBIS 4.0 Cookbook – recommended for model creation!
  - http://www.eda-stds.org/ibis/cookbook/
- IBIS Summit presentations
  - http://www.eda-stds.org/ibis/summits/index-bydate.htm
- Accelera* Verilog-AMS Working Group
  - http://www.eda-stds.org/verilog-ams/
- IEEE* 1076.1 (VHDL-AMS) Working Group
  - http://www.eda-stds.org/vhdl-ams/
- Behavioral Modeling and Simulation Conference 2006
  - http://www.bmas-conf.org/2006/
- On-line signal integrity classes & references
  - http://www.intel.com/education/highered/signal/elct762.htm
  - http://www.intel.com/education/highered/signal/elct865.htm
- Join the IBIS and IBIS-Users e-mail reflectors!

IBIS Model Validation Report

Asian IBIS Summit, Shanghai China
October 27, 2006

Zheng Qi
Qzheng@fiberhome.com.cn

1

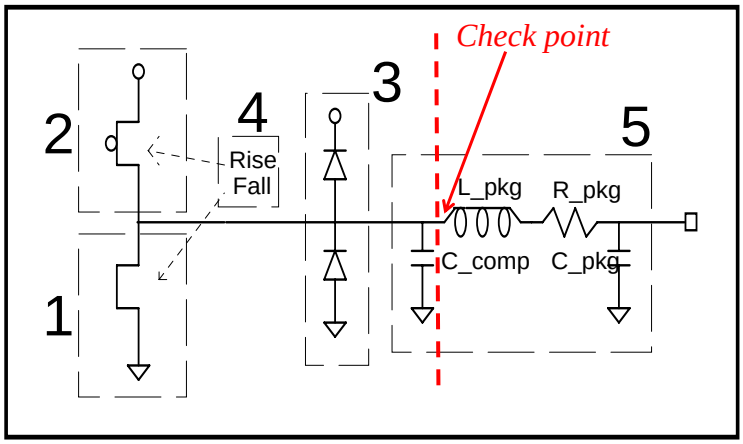
overview

- IBIS Models have played an important role in signal integrity analysis
  - Access Buffer Characteristics
    - Buffer's transition time
    - driver output impedance
  - Critical Net Quality Check
    - Incident Voltage
    - Monotonic
  - Timing Analysis
    - Flight Time Calculating
  - Power Integrity Analysis

2

overview

- Before playing with IBIS we have to know
  - behavioral model concept



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overview

- Model Validation (Comparison)
  - With & without Package parameter
  - Spice model Vs IBIS model
  - R-fixture comparison
- Test fixture
  - 50 Ω Resistor Load to GND
  - 10pf Capacitor load to GND
- Model (original model from *A* company)
  - Push-pull clock buffer
  - 1R+1F
  - R_fixture = 0.50k Ω

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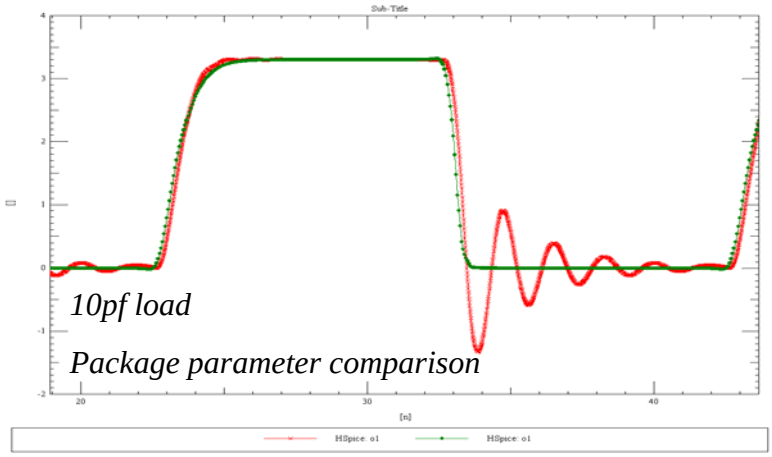
Spice model simulation

- Removing package parameter first



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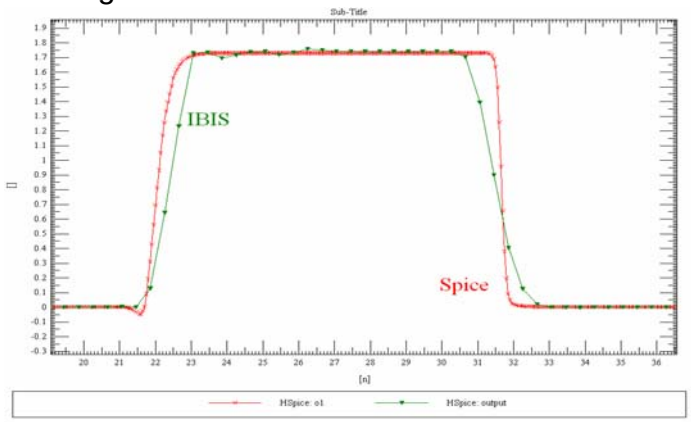
Spice model Vs IBIS model

- Original IBIS model
  - 1R+1F & R_fixture = 0.50K Ω
  - Using 50 Ω load for test



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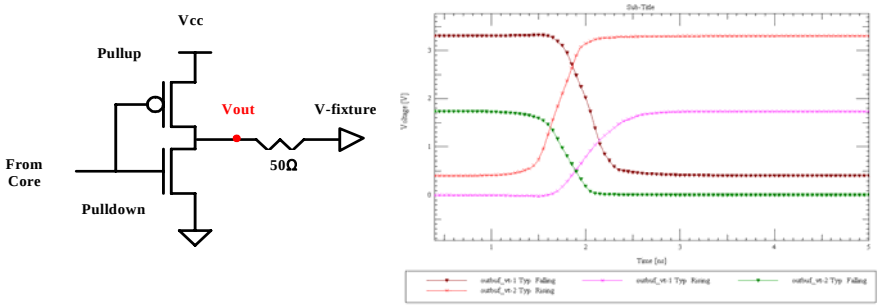
Model adjusting

- Add two V-T curves (2R + 2F)
- R-fixture changed to 50 Ω
- Add More points on V-T curves (lower timestep)



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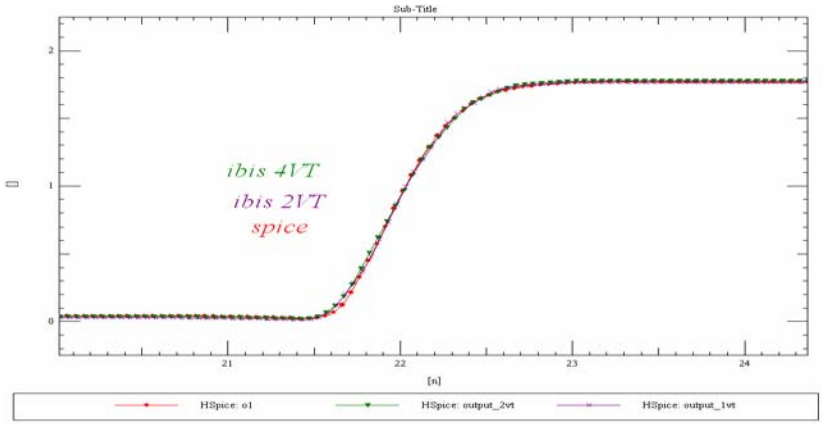
Model test

- Rising edge matched very well ☺
- No different between 2VT and 4VT



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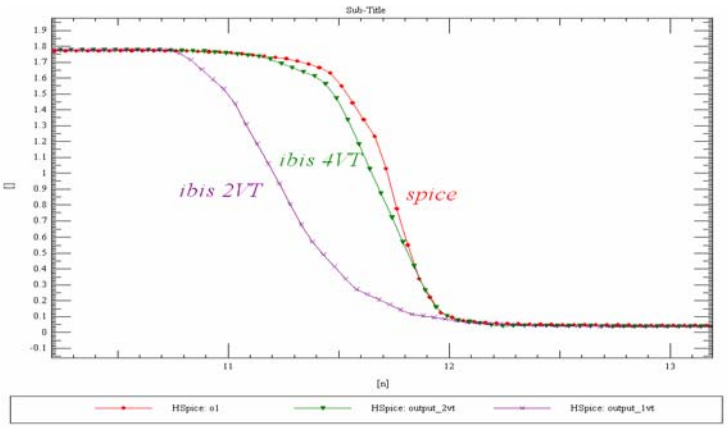
Model test

- 4VT Falling edge match good
- 2VT Falling time degrading (460ps → 750ps)



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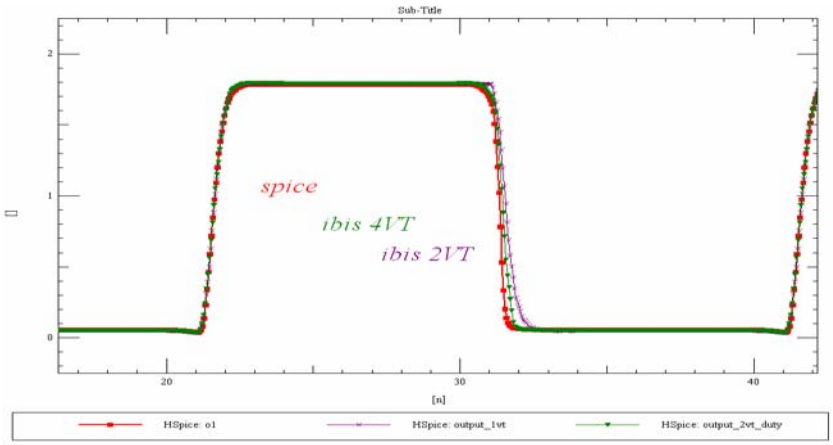
Model test

- Using 4VT and 2VT tables



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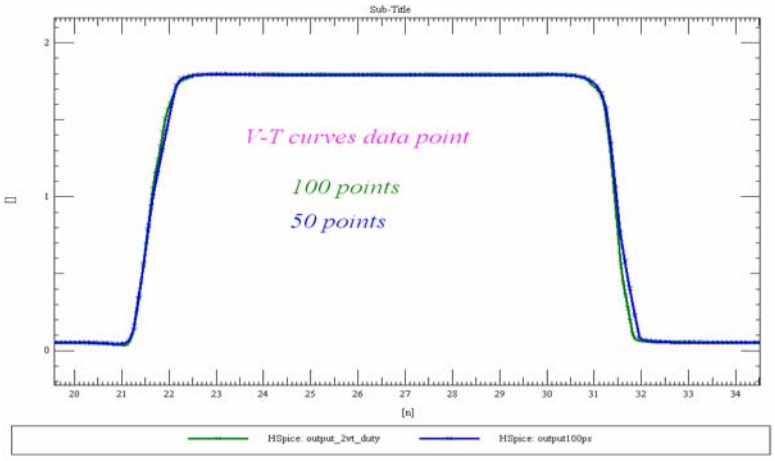
Model test

- Different V-T data points



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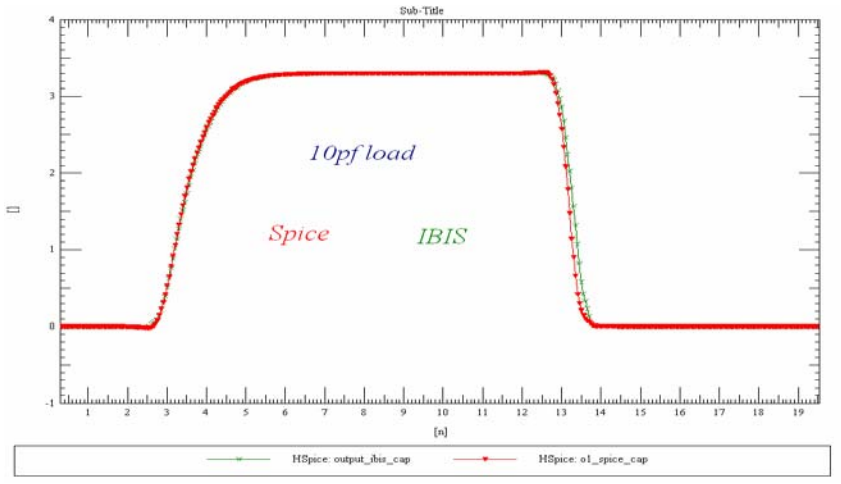
Model test

- Capacitor load (using modified model)



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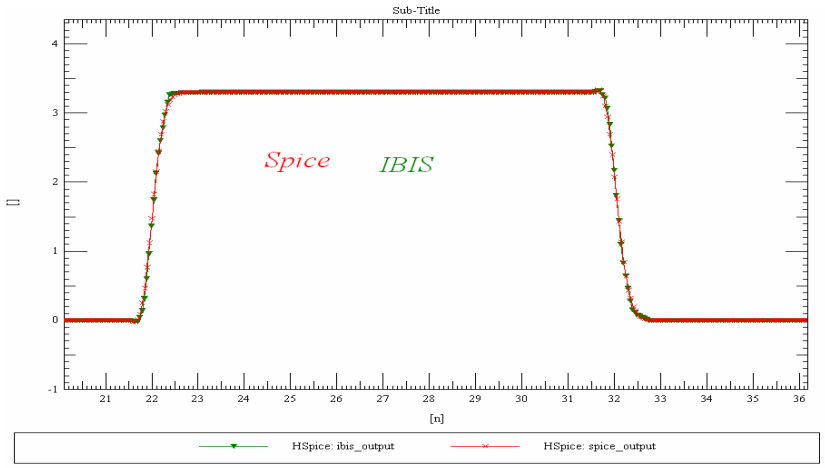
Good model

- B model comparison (good model)



13

Conclusion

- The waveform shape (edge and DC Level) are very close between IBIS and Spice simulation when the model is correctly generated
- Downloaded models always need careful checking
- Package parameters have great impact on waveform quality
- Power pin's package parameters need more attention

14

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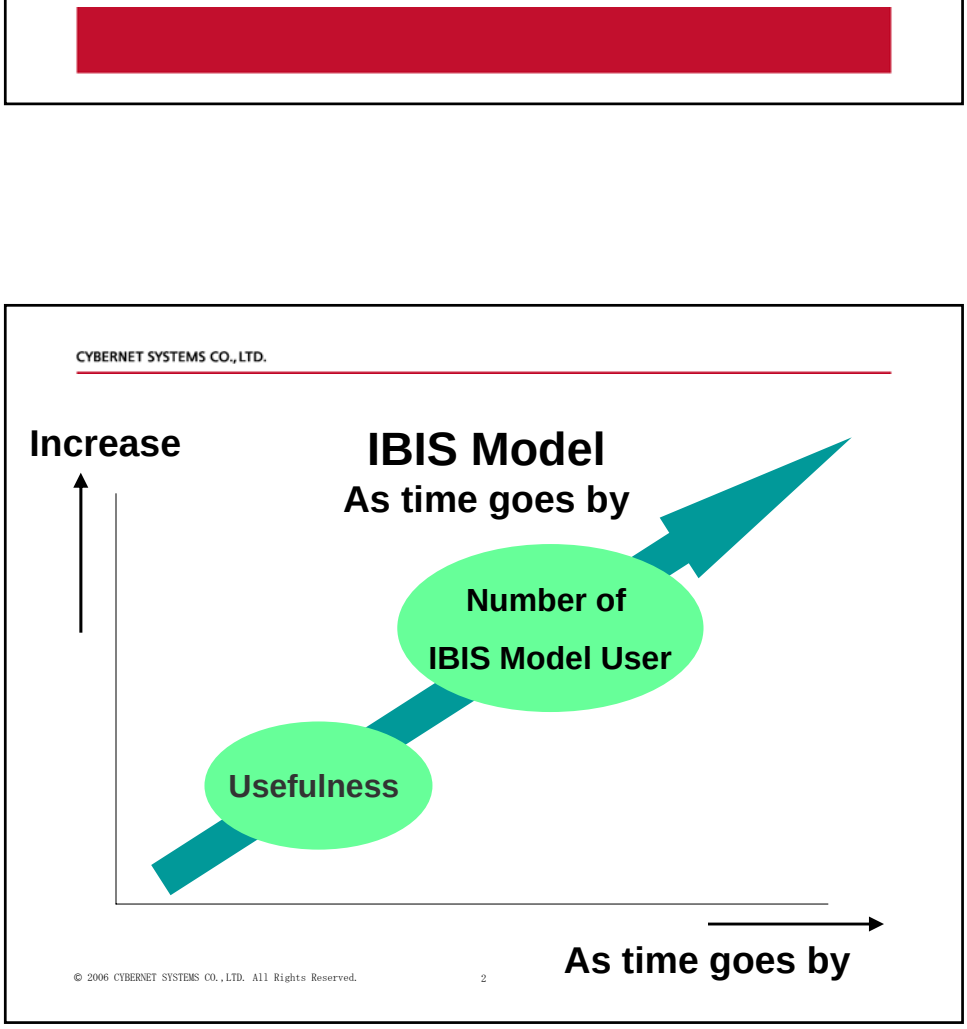
IBIS Model Engineering for SI Simulation

Asian IBIS Summit (CHINA), October 27, 2006

Kazuhiko Kusunoki
k-kusu@cybernet.co.jp



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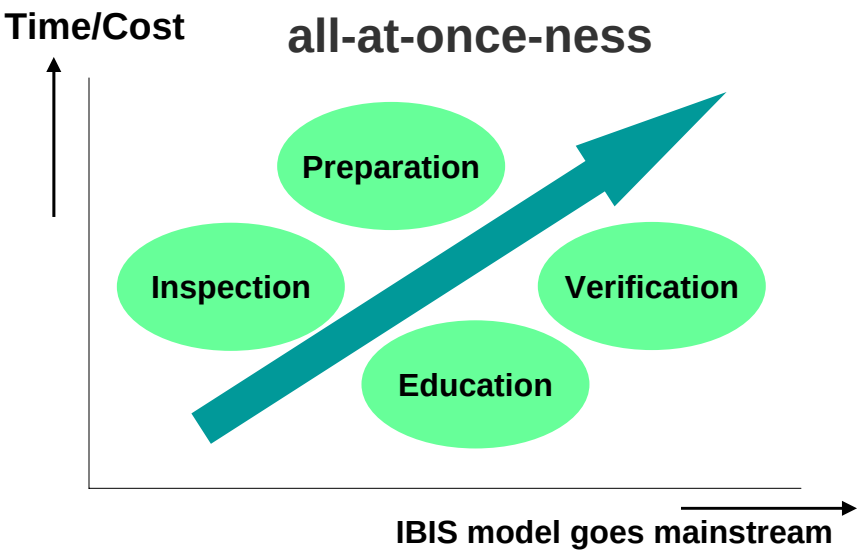

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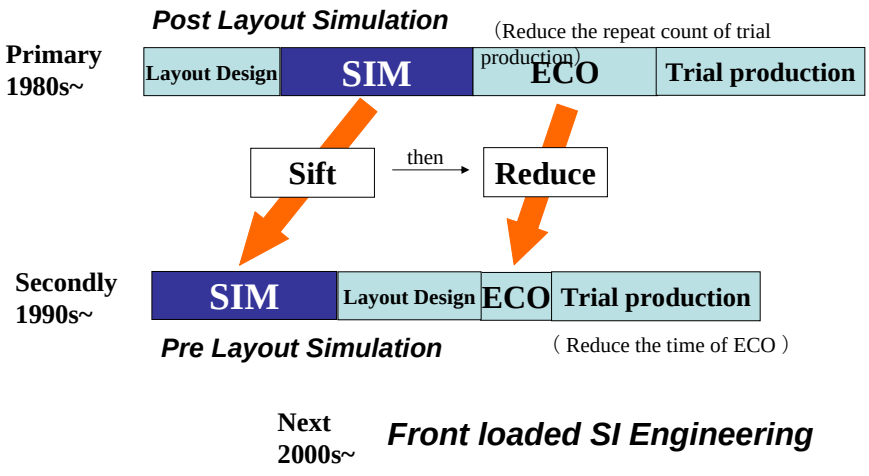
Challenge to the SI simulation Engineering of PCB Design



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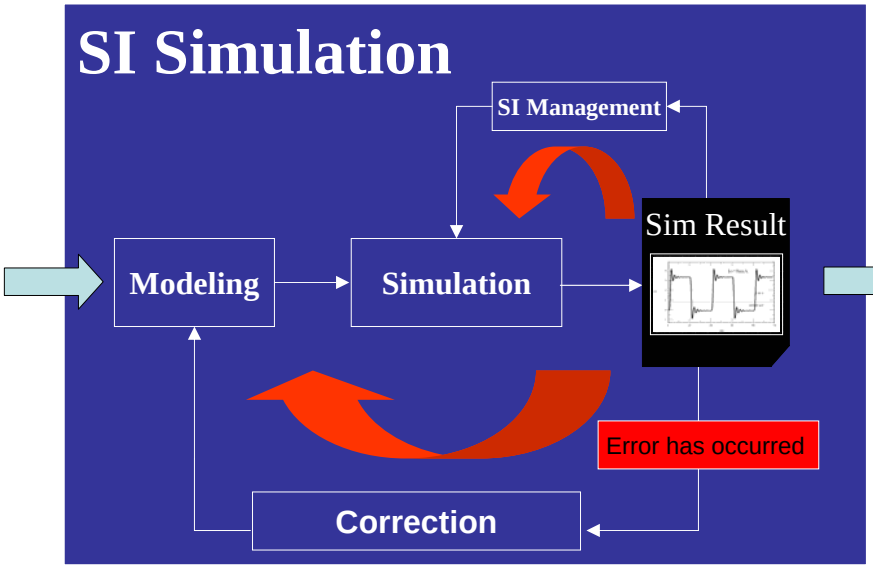

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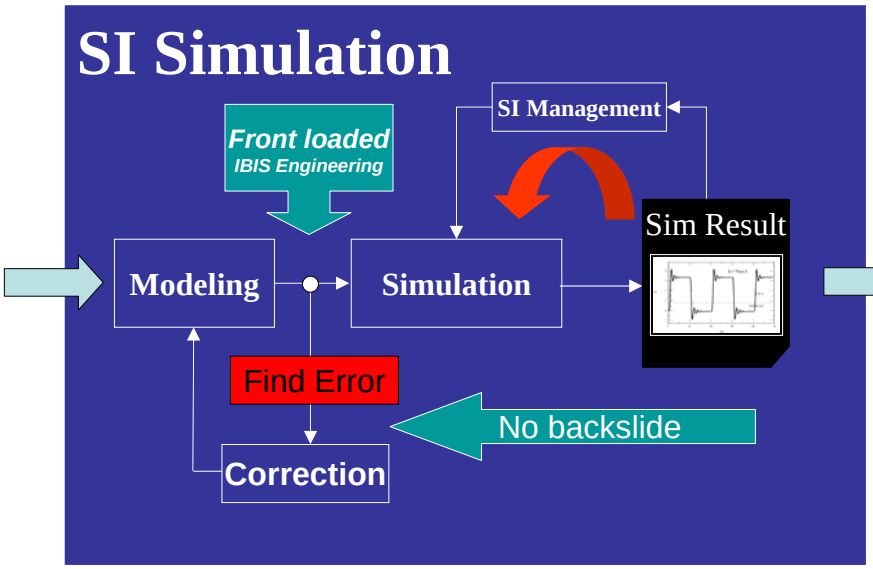

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IBIS model Engineering as Front loaded SI Engineering

To minimized the time of SI simulation

Modeling	SIM

- •Incoming inspection for IBIS Model
  - •Check IBIS Model
  - •Verification IBIS Model
  - •Correction IBIS Model
- •Prepare IBIS Model
- •Tune IBIS Model
- *Make decisions on SI view*

 7

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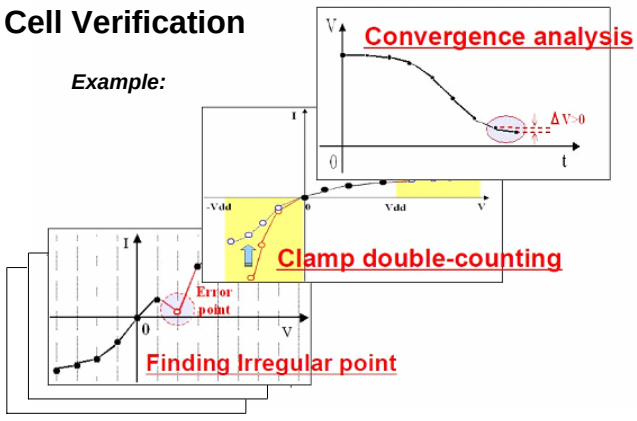
Incoming inspection for IBIS Model

- •Syntax Check
- •I/O Cell Verification

Example:



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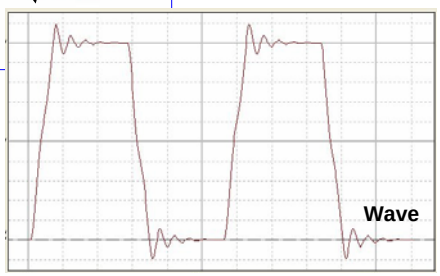
•Verification IBIS Model

Test circuit for IBIS Verification

Example:



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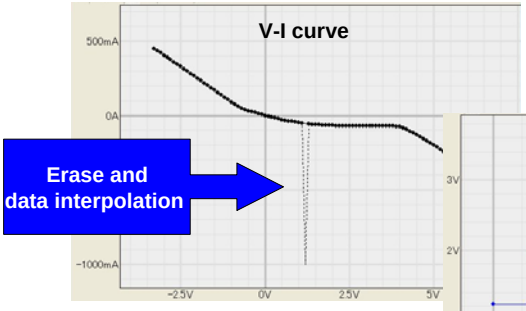
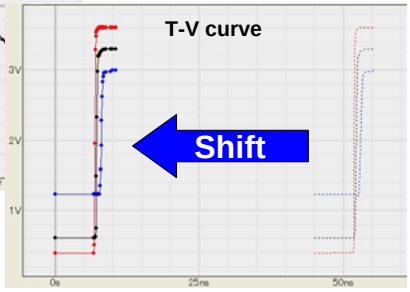
•Correction IBIS Model



Erase and data interpolation

Example:



Shift

 10

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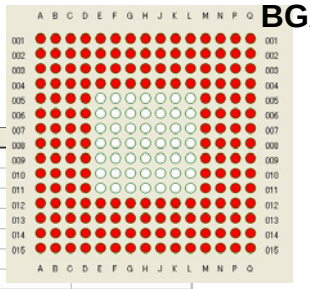
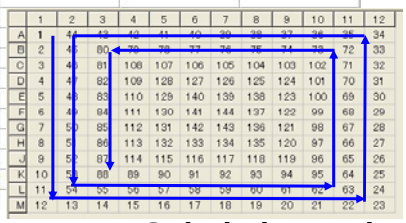
•Prepare IBIS Model

BGA



Pin/Signal/Model Assign

Pin#	Signal	Model	R_pin	L_pin
A001				
A002		EDA77244A_IN		
A003		EDA77244A_IN		
A004		EDA77244A_IN		
A005		EDA77244A_IN		
A006		EDA77244A_IN		
A007		EDA77244A_IN		
A008		GND		
A009		POWER		
A010		NC		
A011		EDA77244A_OUT		
A012		EDA77244A_OUT		
A013		EDA77244A_OUT		
A014		EDA77244A_OUT		
A015		EDA77244A_OUT		
B001		EDA77244A_OUT		
B002				
B003				



Spiral pin number location

11

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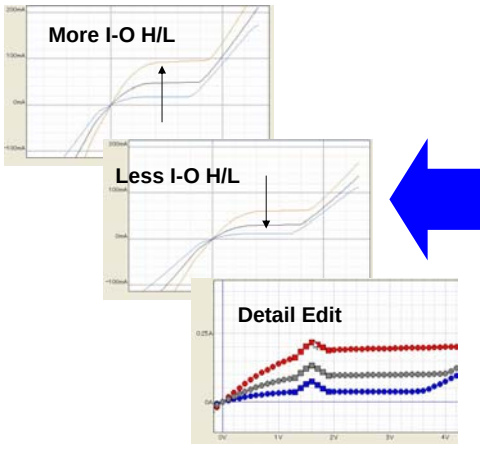
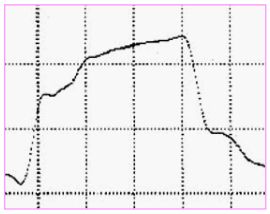
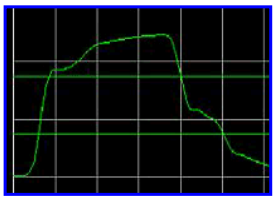
•Tune IBIS Model

Real and Virtual Wave







Comparison-data for the best result

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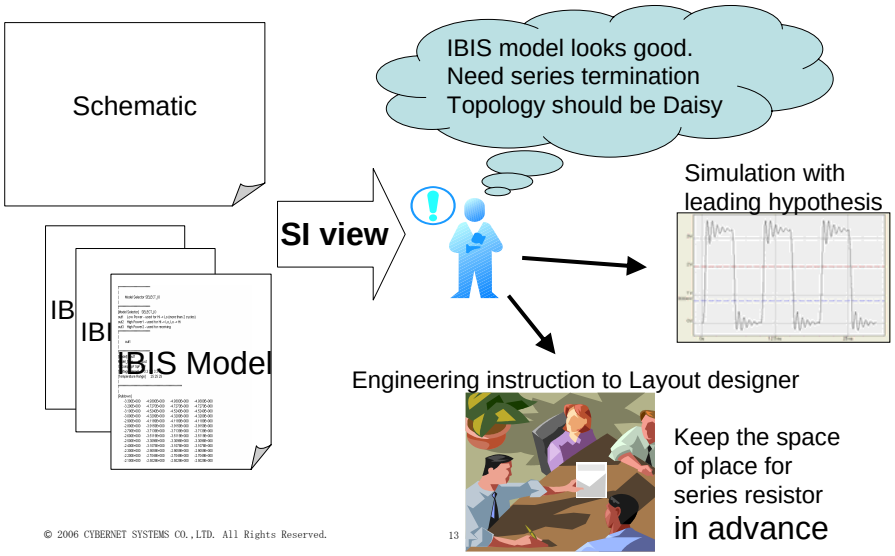
What the SI Electronics whiz does for IBIS?



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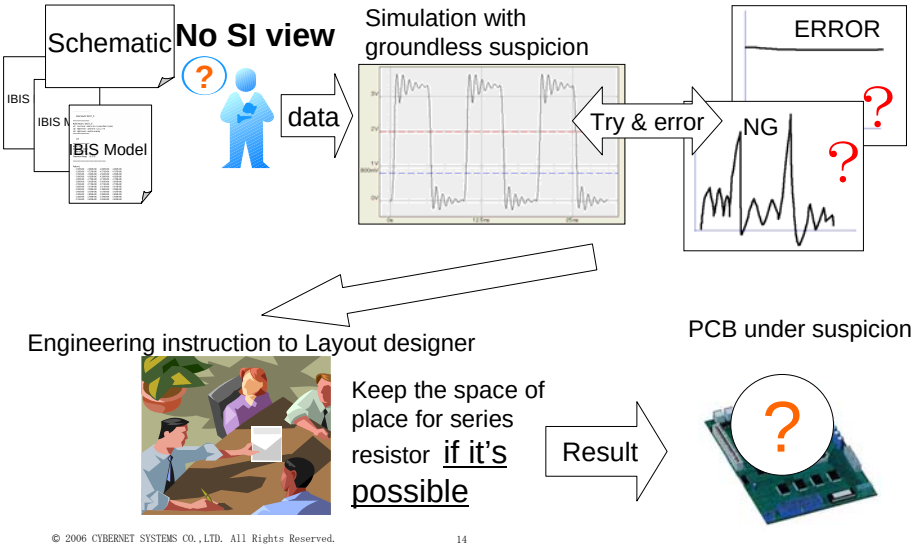
What the Non SI Electronics whiz may do?



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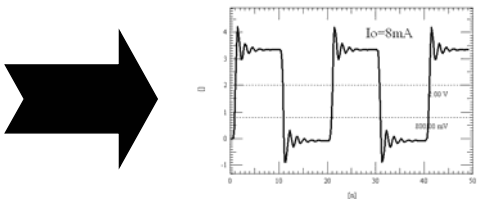
IBIS model Engineering as Front loaded SI Engineering

IBIS Model

```
|*******************************
[Model]  A
Model_type    I/O
Polarity      Non-Inverting
Enable        Active-Low
Vinl = 0.66V
Vinh = 2.00V
C_comp 2.55pF 1.18pF 3.91pF
[Voltage Range] 3.3V 3.0V 3.6V
[Power Clamp Reference] 3.3V 3.0V 3.6V
[GND Clamp Reference] 0.0V 0.0V 0.0V
[Pullup Reference] 3.3V 3.0V 3.6V
[Pulldown Reference] 0.0V 0.0V 0.0V
[Temperature Range] 49.0 125.0 -20.0
|
|*************************************************
|
[Pulldown]
      -3.300E+00     -2.7539E-01     -2.2720E-01     -3.4332E
      -3.200E+00     -2.6889E-01     -2.2122E-01     -3.3549E
      -3.100E+00     -2.6192E-01     -2.1499E-01     -3.2720E
```



Predict Signal Wave from IBIS Model

 15

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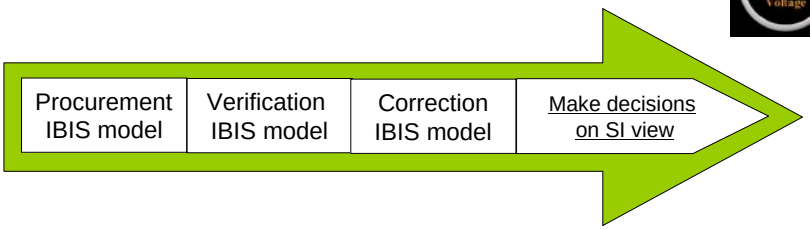
IBIS model Engineering as Front loaded SI Engineering

- Take a look (evaluate a symptom） of Output Current
- Take a look (evaluate a symptom） of Rise/Fall Speed
- Take a look (evaluate a symptom） of Signal amplitude
  - – Trend prediction for Routing Topology, Cross Talk ,etc



 16

CYBERNET SYSTEMS CO.,LTD.

To minimized the time of SI simulation

Pre Layout Simulation

Secondly 1990s~

SIM	Layout Design	ECO	Trial production

Prevention of the backslide

NEXT 2000s~

SIM	Layout Design	ECO	Trial production

Front loaded SI Engineering

As far in advance as possible

(Reduce the time of SIM)

 17

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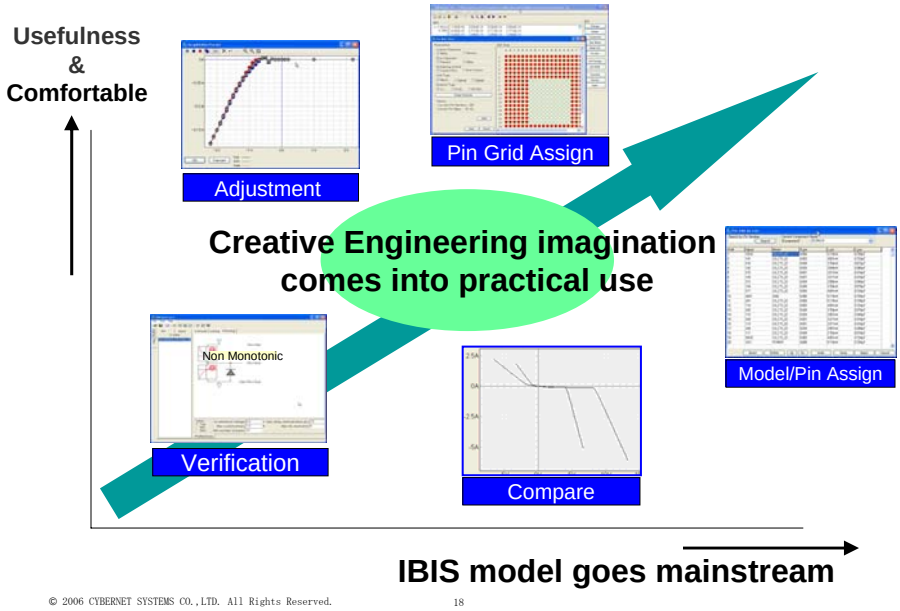
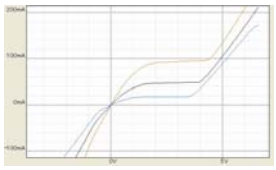


 18

CYBERNET SYSTEMS CO.,LTD.

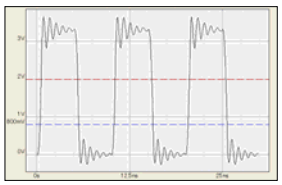
Make IBIS more comfortable

使IBIS使用更方便



Tune

Indicate



Verify

INVENTIVE

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Case Study: Spice Macromodeling for PCI Express using IBIS 4.2

Lance Wang
Email: lwang@cadence.com
IBIS Asian Summit
Oct. 27th, 2006, Shanghai, China

Outline

- PCI Express Serial Link
- Macromodeling Steps
- IBIS 4.2 Spice Macromodeling
- Validations and Optimizations
- Conclusions

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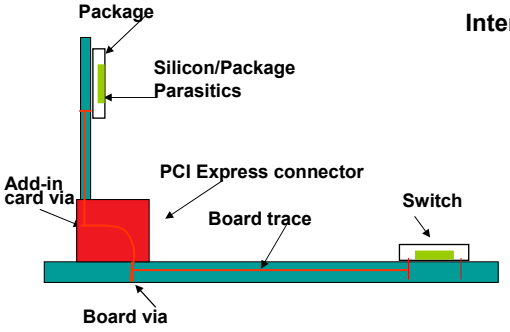
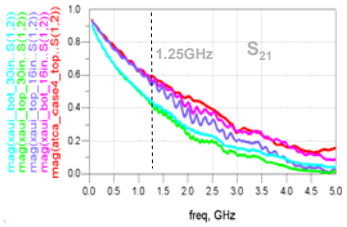
The PCI Express Environment



Inter Symbol Interference/Attenuation



Low Pass Filter

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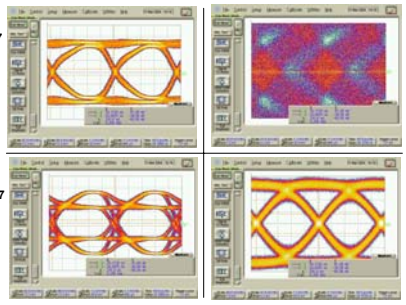
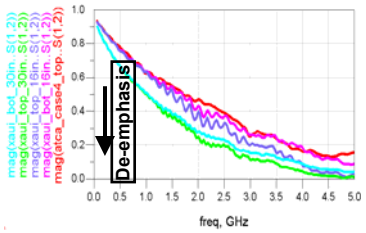
Overcoming ISI using Transmit Equalization (De-Emphasis)

Transmitter > 40" FR4 < At Receiver

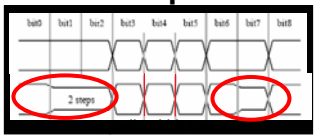
2.5Gbps, PRBS7 No Eq.

2.5 Gbps PRBS7 -3.5 dB Eq.





Transmit Equalization



PCI-Exp Features (Example)

EQ Control = 4 bit wide DEq bits

Swing Control =4 bit wide DTx, & HI/LO DRV bits

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Outline

- PCI Express Serial Link
- Macromodeling Steps
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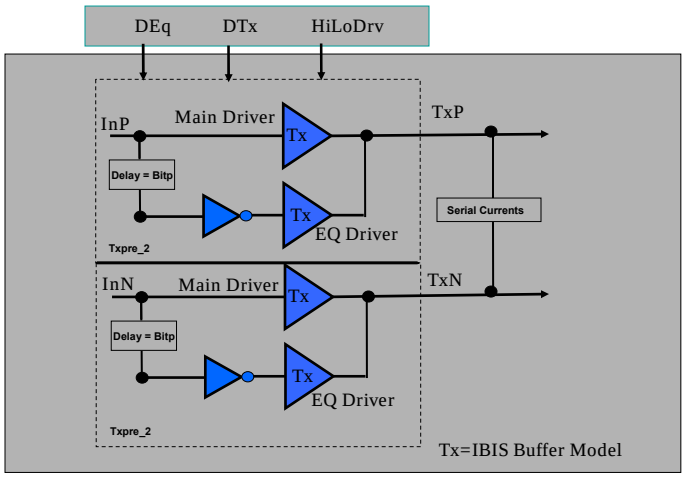
Macromodeling Steps
- Understanding Structures



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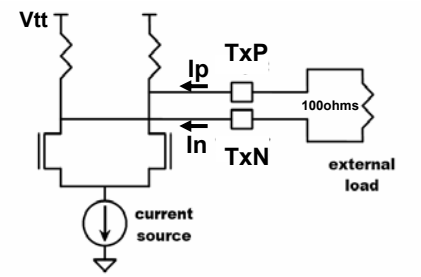
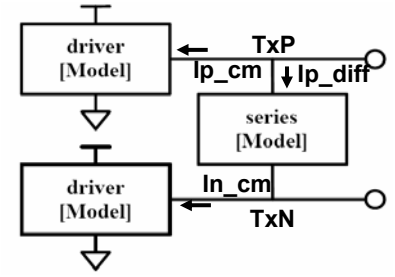
Macromodeling Steps

- True Differential Pair IBIS Models Extraction





- Common Mode I-V Tables
  - Pull-up
  - Pull-Down
  - Clamp to represent Rterm
- Differential Model
  - Non linear Series Mosfet Representation
  - Linear Resistor Representation
- V-t Table
  - Recommended to have 2 sets of curve for each TxP and TxN
  - 1)Low –High 2)High-Low
- C_Comp/Cdiff
  - Represents C of transistors, die pads and on-chip interconnects. It does not include pkg C

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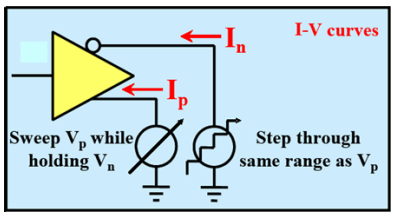
Macromodeling Steps

- Extracting Common and differential Mode Currents



- Pull up and Pull Down Common Mode and differential Mode Current
  - Vp = Vn we are measuring common mode current
  - When Vp ≠ Vn, we are measuring common + differential currents
  - To get the differential current, we need to subtract the common mode current
- I-V Table Extraction for Clamp Data & On-Die Termination
  - One way to include on-die termination is to use superposition and add the termination currents to the diode currents in the clamp sections
  - Clamps are always active in an IBIS model, regardless of whether the buffer is driving or receiving.

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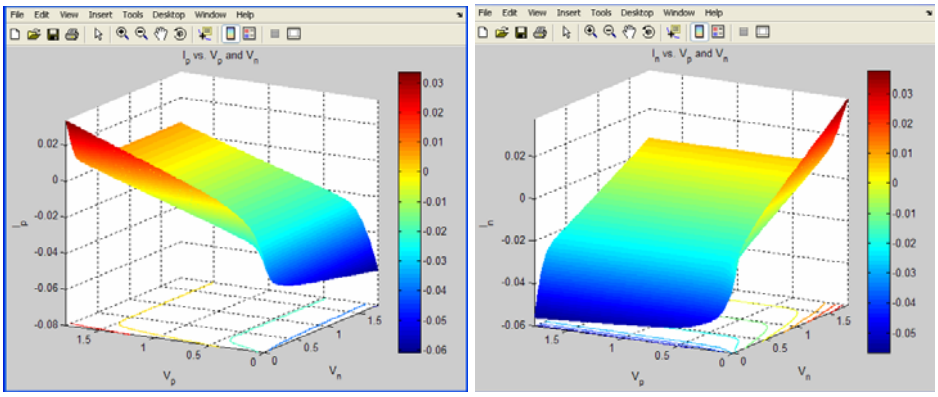
Macromodeling Steps
- In & Ip Surface Plots of Total Current



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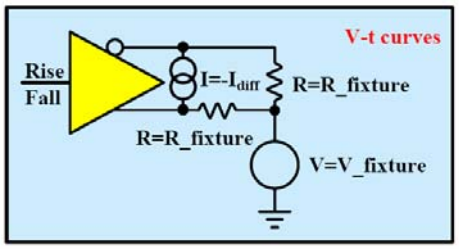
Macromodeling Steps
- V-t Data Extraction



V-t Table
V_fixture = 0V
V_fixture = 1.8V
R_fixture=
Typical load of 50 ohms

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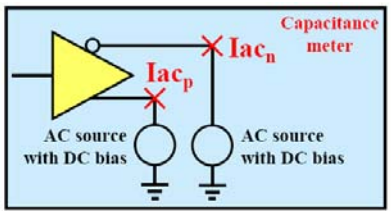
Pad Capacitance: Common and differential Ccomp



- Run frequency domain simulations (.AC) with the above circuit
  - **Give one of the AC sources 0 V AC amplitude (makes it a DC source)**
  - **Give the other AC source a small AC amplitude (1 mV)**
  - **Give both of the sources an appropriate DC bias**
- Calculate capacitance using:

  $C = Im(I) / (2\pi f * Amplitude)$
  - **For Ccommon use the current of the "DC" source**
  - **For Cdiff use the current of "AC" source minus "DC" source**
- Repeat everything at different DC bias voltages

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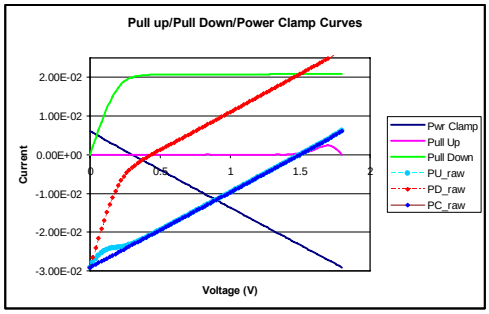
Macromodeling Steps
- Pull Up, Pull Down and Clamp Curves




```
|*****************************************************************
|          PULL UP Data
|*****************************************************************
[Pullup]
|Voltage        I(typ)        I(min)        I(max)
1.8             -2.34E-05     NA            NA
1.78            8.32E-04      NA            NA
1.76            1.47E-03      NA            NA
...
...
0.04            3.47E-06      NA            NA
0.02            8.07E-06      NA            NA
0               7.00E-06      NA            NA
|*****************************************************************
|          PULL DOWN Data
|*****************************************************************
[Pulldown]
|Voltage        I(typ)        I(min)        I(max)
1.8             2.09E-02      NA            NA
1.78            2.09E-02      NA            NA
1.76            2.09E-02      NA            NA
....
....
0.04            4.31E-03      NA            NA
0.02            2.19E-03      NA            NA
0               0.00E+00      NA            NA
[GND Clamp]
|   Voltage        I(typ)              I(min)        I(max)
0.0000          0.00000000e+000       NA            NA
1.8000          0.00000000e+000       NA            NA
[POWER Clamp]
|  Voltage        I(typ)              I(min)        I(max)
1.8             -2.91E-02             NA            NA
1.78            -2.87E-02             NA            NA
...
...
0.04            5.27E-03              NA            NA
0.02            5.70E-03              NA            NA
0               6.14E-03              NA            NA
```

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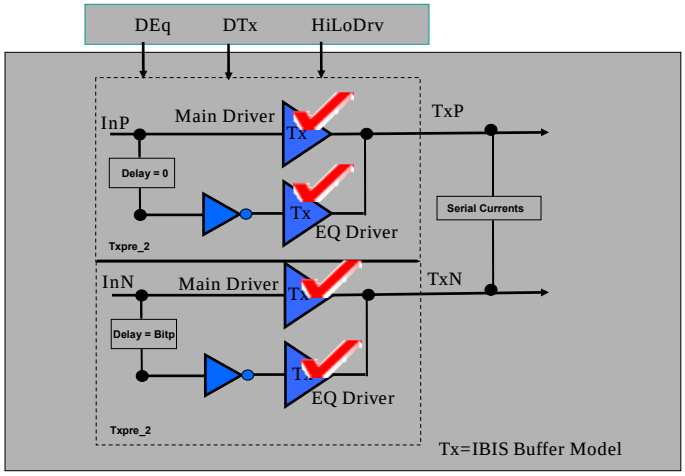
Macromodeling Steps
- Understanding Structures



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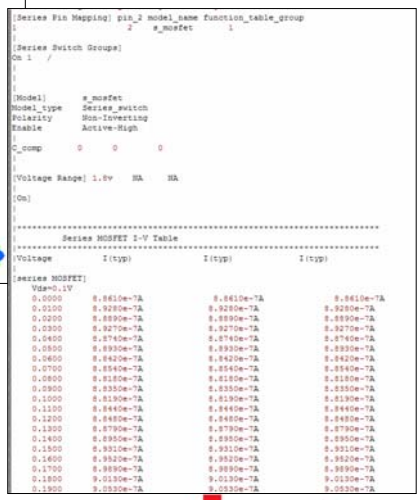
Separating the differential mode current

- **The off-diagonal current values represent the sum of the common and differential mode currents**
- **To obtain the differential mode currents alone, "normalize" the surface so that its diagonal values become zero**
  - Subtract the common mode component from the surface and use it for the Series [Model]'s [R Series], [Series Current], [Series MOSFET], etc… keywords
  - If the surface is linear (flat) [R Series] is sufficient
  - Otherwise use the [Series Current] or [Series MOSFET] keywords
  - Slice the surface along the necessary voltage value(s) to satisfy the syntax requirement of the IBIS keyword used

intel

page 11 CPD



Slide from Arpad Muranyi's true diffpair modeling IBIS Summit 2003

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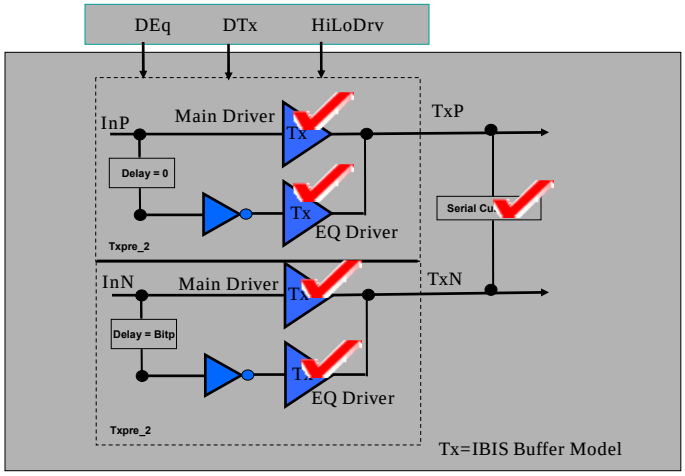
Macromodeling Steps
- Understanding Structures



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Macromodeling Steps
- Coefficient table for HiLoDrv, DEq and DTx

```
* coefficient to control the current source
.param ctrlcoef='if(hilodrv == 0) (1.00)
+ elseif(hilodrv == 1) (0.50)
+ elseif(hilodrv == 2) (1.4) else(1)'.....
+.....

* coefficient to control dtx bits
.param dtxcoef='if(dtx == 0) (1)
+ elseif(dtx == 1)  (1.05)
+ elseif(dtx == 2)  (1.1)
+ elseif(dtx == 8)  (0.6).....
+ .....

* coefficient to control the eq bits
.param deqcoef='if(deq == 0) (1.0)
+ elseif(deq == 1)  (0.96)
+ elseif(deq == 2)  (0.92)
+ elseif(deq == 3)  (0.88)
+ elseif(deq == 4)  (0.84).....
+.....
```

HSpice is capable for this circuit.

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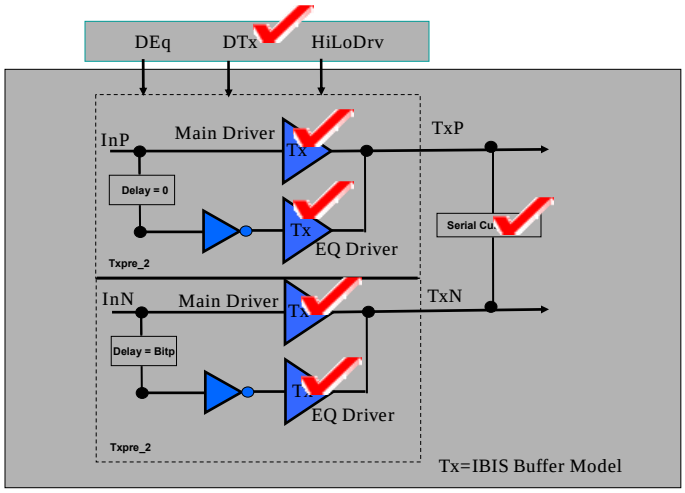
Macromodeling Steps
- Understanding Structures



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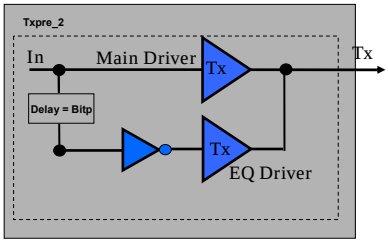
Macromodeling Steps
- Output Block Example




```
.subckt txpre_2 nvdd out ngnd in en
+ bitp=400p inv0=0 inv1=1
+ cf0=1 cf1=0 scale=1  padcap=1.2p ampctrl=1

* Here are the subcircuit calls for the tap inputs
xin0 in0 in ngnd delayin inv=inv0
xin1 in1 in ngnd delayin inv='inv1' del='bitp'

xtx0 nvdd out ngnd in0 en tx sclpux='scale*cf0*ampctrl' sclpdx='scale*cf0*ampctrl'
xtx1 nvdd out ngnd in1 en tx sclpux='scale*cf1*ampctrl' sclpdx='scale*cf1*ampctrl'

* This is the subcircuit definition for tx, used for the taps.
.subckt tx nvdd out ngnd in en sclpux=1 sclpdx=1
bdrvr nvdd out ngnd in en Model=BUFF File=ibis_file
+ VIScale_pullup='sclpux'
+ VIScale_pulldown='sclpdx'
.ends tx
```

HSpice is capable for this circuit.

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Macromodeling Steps - P & N Pins

```
* P side driver subcircuit call
xp nvdd outp ngnd in en txpre_2 BUFF=BUFF ibis_file=ibis_file
+ bitp=bitp inv0=inv0 inv1=inv1
+ scale=scale
+ cf0=cf0
+ cf1=cf1
+ rt=rt
+ ampctrl=ampctrl

* N side driver subcircuit call
xn nvdd outn ngnd inn en txpre_2 BUFF=BUFF ibis_file=ibis_file
+ bitp=bitp inv0=inv0 inv1=inv1
+ scale=scale
+ cf0=cf0
+ cf1=cf1
+ rt=rt
+ ampctrl=ampctrl
```

HSpice is capable for this circuit.

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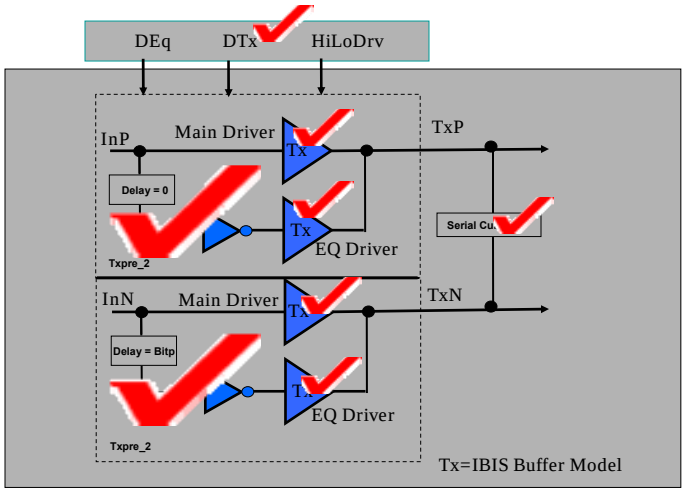
Macromodeling Steps - Understanding Structures



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Outline

- PCI Express Serial Link
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cadence

Wrap into IBIS 4.2

```
|*************************************************************************
[IBIS Ver]      4.2
[File Name]     pcie_rs2314.ibs
[File Rev]      1.0
[Date]          4/7/2006
[Source]        Converted from PCIe Macromodel
[Notes]
[Disclaimer]
[Copyright]     Copyright 2006,
|*************************************************************************
[Component]     rs2314_tx
[Manufacturer]  ABC Inc.
[Package]
|               typ             min             max
R_pkg           0.001           0.001           0.001
L_pkg           1e-013          1e-013          1e-013
C_pkg           1e-015          1e-015          1e-015
|*************************************************************************
[PIN]   signal_name     model_name      R_pin   L_pin   C_pin
|
A1      txoutp          pcie_behav  0.086 4.3e-009 0.72e-012
B1      txoutn          pcie_behav  0.086 4.3e-009 0.72e-012
Base    test_single     behav_base
|*************************************************************************
[Diff Pin]   inv_pin   vdiff   tdelay_typ  tdelay_min  tdelay_max
A1           B1        200mv      0           0           0
|
|*************************************************************************
[Model] pcie_behav
| need to use *_diff for ture differential pair models
Model_type Output_diff
|
Rref diff = 100
```

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Wrap into IBIS 4.2

```
|*****************************************************************
|[Model] pcie_behav
| need to use *_diff for ture differential pair models
Model_type Output_diff
|
Rref_diff = 100
|
| Other model subparameters are optional
|
|              typ    min    max
|[Voltage Range]   1.5    1.5    1.5
|
|[Ramp]
|dV/dt_r      300mV/95ps   240mV/80ps   360mV/110ps
|dV/dt_f      300mV/95ps   240mV/80ps   360mV/110ps
|
|[External Model]
Language SPICE
|
| Corner corner_name file_name       circuit_name (.subckt name)
| specify the corners
Corner    Typ        pcie.spc       pcie_behav
Corner    Min        pcie.spc       pcie_behav
Corner    Max        pcie.spc       pcie_behav
|
| Parameter definitions
| prefix BUFF will be traded as buffer model setting.
Parameters BUFF=behav_base
|
| all regular parameters are here. Change them for different settings
Parameters bitp=400p
Parameters scale=1.60
Parameters rt=50
Parameters dtw=5
Parameters deq=3
Parameters hilodrv=0
|
| Ports List of port names (in same order as in SPICE)
|
Ports  A_pure    A_signal_pos  A_pdref  my_drive
Ports  A_pcref       A_gcref  A_signal_neg
|
| D_to_A d_port   port1      port2     vlow vhigh trise tfall corner_name
D_to_A    D_drive  my_drive   A_pdref  0.0  1.0  95p   95p   Typ
D_to_A    D_drive  my_drive   A_pdref  0.0  1.0  80p   80p   Min
D_to_A    D_drive  my_drive   A_pdref  0.0  1.0  110p  110p  Max
| D_to_A will be used as escale my_drive 3 v=[vhigh - vlow]*v[D_drive]+vlow
| trise and tfall will be the ramping data
|
| no A_to_D required
|
|End External Model]
```

```
|*****************************************************************
|                    Model behave_base
|                    Your base IBIS model
|*****************************************************************
|
|[Model]           behav_base
|Model_type        Output
|Polarity          Non-Inverting
|Vmeas = 1.5V
|Cref = 0pf
|Rref = 50
|
|C_comp            0.1pF              0.1pF              0.1pF
|
|[Temperature Range]       25.00              110.00             0
|[Voltage Range]           1.5V               1.5V               1.5V
|
|[Pulldown]
| Voltage     I(typ)              I(min)              I(max)
|
  -1.50000000    -0.15536276  -1.7720580e-01  -1.5186892e-01
  -1.49550000    -0.15460042  -1.7637204e-01  -1.5124756e-01
  -1.44600000    -0.14637165  -1.6724147e-01  -1.4492167e-01
  -1.39200000    -0.13770218  -1.5736305e-01  -1.3570920e-01
  -1.34250000    -0.13024052  -1.4860655e-01  -1.3352146e-01
  -1.29300000    -0.12349249  -1.3957303e-01  -1.2863052e-01
  -1.24800000    -0.11808127  -1.3167686e-01  -1.2429165e-01
```

```
  2.19000000    -6.7012511e-02  -6.1060134e-02  -6.1723691e-02
  2.20350000    -6.7835275e-02  -6.2736430e-02  -6.2232266e-02
  2.23950000    -8.0127845e-02  -6.7561165e-02  -6.3749560e-02
  2.29800000    -8.4085115e-02  -7.6244530e-02  -6.6782908e-02
  2.31400000    -8.5347973e-02  -7.9074838e-02  -6.7833665e-02
  2.40150000    -6.1614040e-02  -9.3217729e-02  -8.3398839e-02
  2.50050000    -7.0014198e-02  -1.1054306e-01  -6.0607386e-02
  2.59950000    -8.1788518e-02  -1.2844615e-01  -6.8253345e-02
  2.60400000    -8.2422850e-02  -1.2928914e-01  -6.8408244e-02
  2.69850000    -9.6898578e-02  -1.4675844e-01  -7.6294170e-02
  2.70300000    -9.7743191e-02  -1.4759714e-01  -7.6682360e-02
  2.80200000      -0.11476617   -1.6615378e-01  -8.6584787e-02
  3.00000000      -0.15094998   -2.0375806e-01  -1.1672558e-01
|
|[Ramp]
| variable      typ                 min                 max
|dV/dt_r      300mV/95ps   240mV/80ps   360mV/110ps
|dV/dt_f      300mV/95ps   240mV/80ps   360mV/110ps
|R_load = 50.00
|
| End [Model] pcie_behave_base
|
|*****************************************************************
```

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Outline

- PCI Express Serial Link
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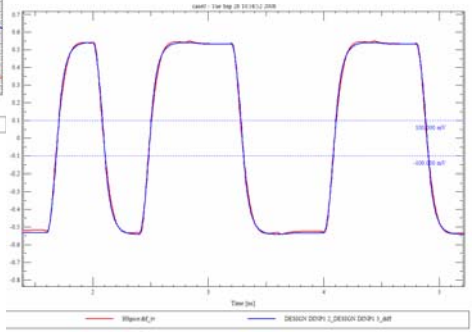
Validations and Optimizations
- DEq = 0, DTx = 0, HiLoDrv = 0



- Use combined die capacitor instead of C_comp in IBIS model
- Use combined on-die terminator instead of clamps
- Adjust DEq and DTx initial levels

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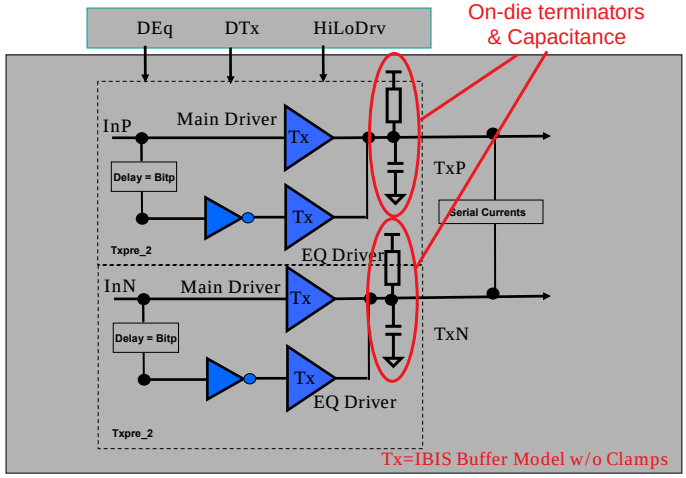
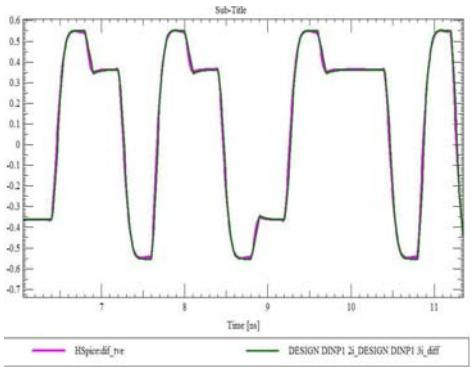
Macromodeling Steps
- Understanding Structures



cadence

Validations and Optimizations
- DEq = 8, DTx = 0, HiLoDrv = 0



- Added one more series_switch on parallel
- Added Miller Capacitances

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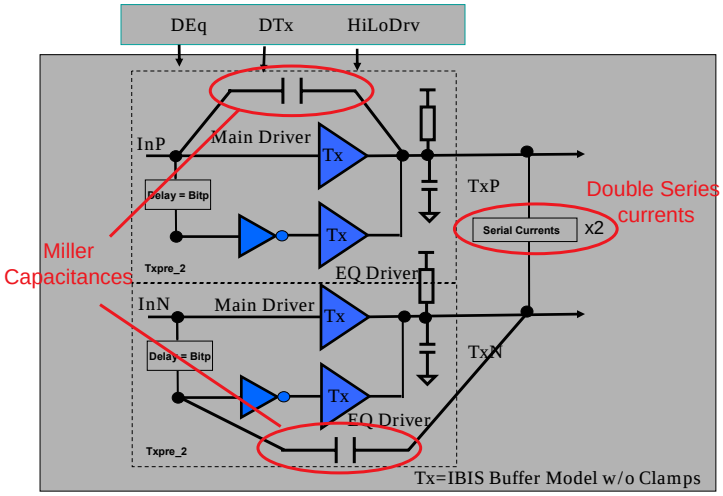
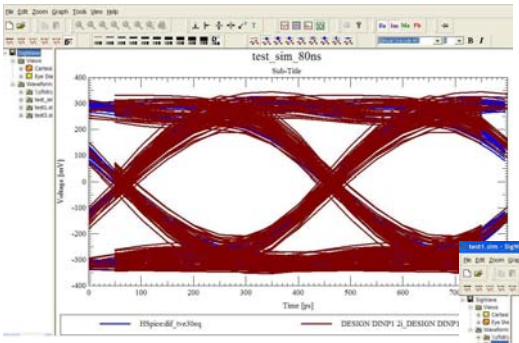
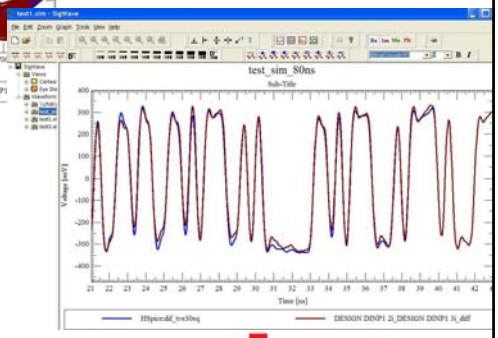
Macromodeling Steps
- Understanding Structures



cadence

Simulation Results 30” Backplane





Simulation Time (WinXp, 2.1GHz CPU, 2GB RAM)		
IBIS Macromodels		Transistor Models
PCB SI (3000 bits)	HSpice (2000 bits)	HSpice (2000bits)
12mins.	7mins.	1.5 hrs

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Outline

- PCI Express 3.125 Gbps Serial Link
- Macromodeling Steps
- IBIS 4.2 Spice Macromodeling
- Validations and Optimizations
- Conclusions

cadence

Conclusions

- Spice Macromodeling using IBIS 4.2 [External Model] is accurate and much faster than transistor-level models
- Spice Macromodeling is durable and can work on existing Spice simulators
  - Understanding the structure is the key
- IBIS future enhancement requests
  - Open IBIS for other commercial Spice simulators
  - Spice [External Model] needs to pass Parameters too
  - “Self-containing” IBIS Buffer from [External Model] is required for Spice Macromodeling. (Some commercial Spice simulators have this capability already)

cadence

Thank You!

- Acknowledgements / References
  - CDNLive Silicon Valley Paper from Nirmal Jain @Rambus
  - IBIS Summit 2003, True Diffpair Modeling, Arpad Muranyi @Intel
  - IBIS Cookbook

cadence

System-Level Timing Closure Using IBIS Models

Barry Katz
President/CTO, SiSoft
Asian IBIS Summit

SiSoft

- Signal Integrity

Agenda

- High Speed System Design
- Establishing timing model
  - Derivation of timing equations
  - Idealized timing analysis
  - The role of signal integrity
  - Reconciling signal integrity with timing
- Pre-route exploration
- Driving physical design
- Post-route validation
- Design analysis reuse
- Case study: DDR2 memory

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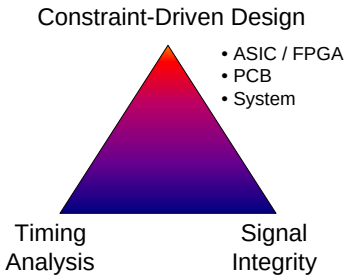
High Speed System Design … Not Just "Signal Integrity"



- High Speed Design involves multiple disciplines
- Changes in any area drive changes in others
- Mastery of modeling details & process flow is essential for success

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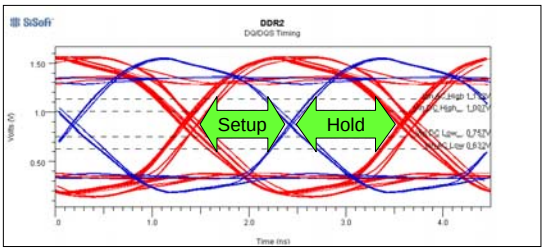
System Level Timing Closure



- Successful high speed design requires a rigorous methodology for ensuring positive design margin across all combinations of:
  - Component timing (process)
  - Voltage & temperature
  - Package & PCB routing lengths
  - PCB manufacturing variations (Z_0, loss)

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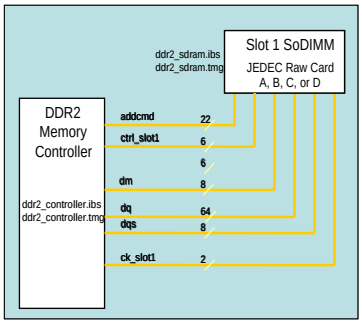
Establishing Timing Budgets



- High speed interfaces have one or more “transactions” that require timing closure
- Memory example:
  - Address/control
  - Data read
  - Data write
  - Strobe to Clock
- Timing relationships must be identified and closed for each different transaction

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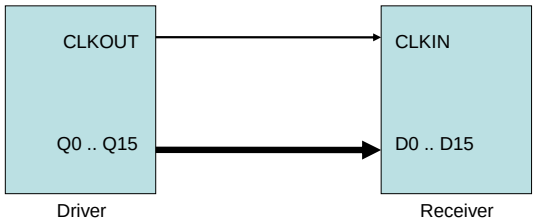
Source-Sync Transaction Example



- Establish component timing & transfer protocol
- Derive timing equations
- Idealized timing analysis
- Signal integrity analysis and Timing Closure

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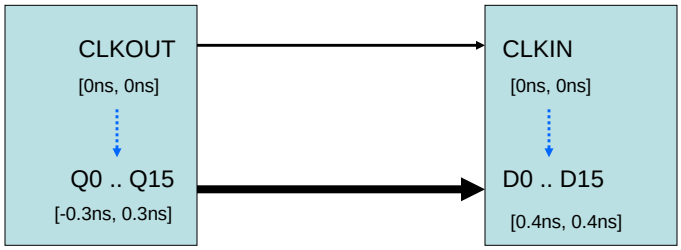
Component Timing, Transfer Protocol



Driver Output Timing

Receiver Setup / Hold Requirements

Clock = 250 MHz
Source Sync, DDR transfer
Data Unit Interval = 2ns
90^{o} clock shift on PCB

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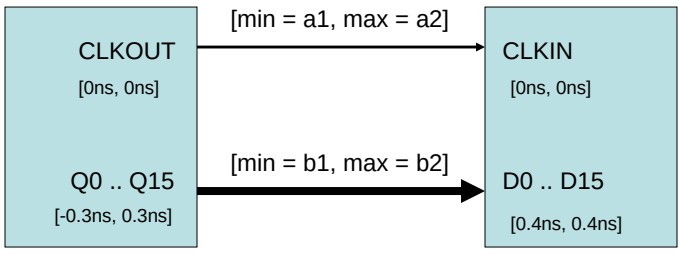
Derive Timing Equations



Setup margin = [early clock] – [late data] – [setup requirement]
= [0ns + a1] – [0.3ns + b2] - [0.4ns]
= a1 – b2 – 0.7ns

Hold margin = [Data UI] + [early data] – [late clock] - [hold requirement]
= [2ns] + [-0.3ns + b1] – [0ns + a2] - [0.4ns]
= 1.3ns + b1 – a2

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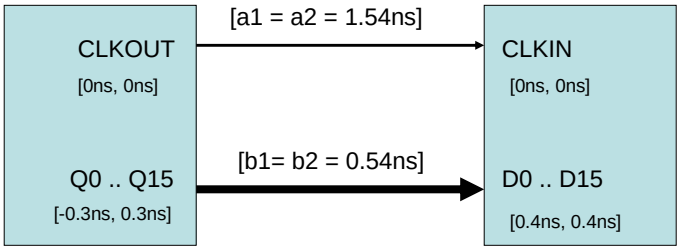
Idealized Timing Analysis

Minimum data length = 3”, at 180ps/in = 0.54ns



Setup margin = a1 – b2 – 0.7ns
= 1.54ns – 0.54ns – 0.7ns
= 0.3 ns

Hold margin = 1.3ns + b1 – a2
= 1.3ns + 0.54ns – 1.54ns
= 0.3ns

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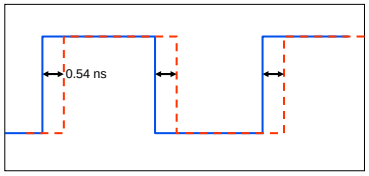
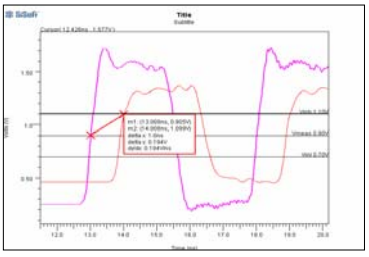
The Role of Signal Integrity



Idealized Delays



Real-World Delays

- Detailed analysis of digital switching behavior
- IBIS or HSpice models define I/O buffer behavior
- Accounts for
  - Actual circuit loading
  - Reflections / ringing
  - Circuit topology
  - Inter-symbol interference
  - Switching thresholds

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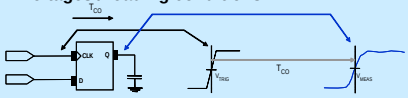
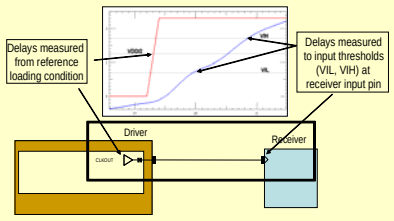
Reconciling SI with Timing

- **Device delays are measured using specific voltages / loading conditions:**



- **SI flight times must be measured based on those same conditions:**



- Static timing and signal integrity measurements *must* be compatible
- SI measurements are "normalized" to conditions under which loading is specified
  - IBIS Vref, Cref, Rref, Vmeas
- Timing Closure occurs when integrated timing/SI results show acceptable setup/hold margins

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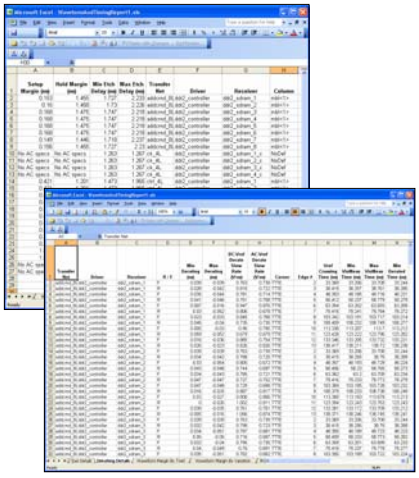
Building an Executable Timing Model



- For each interface, all transactions must be validated for all cases:
  - Component timing (process)
  - Voltage, temperature
  - PCB variations
- Creating an executable timing model to perform automatic regression is ideal
- Possibilities
  - Excel
  - Custom scripting
  - EDA tools

$$t_{cycle} = t_{co} + t_{final\ settling} + t_{setup} + t_{skew} + t_{jitter} + t_{SSO} + t_{ISI}$$

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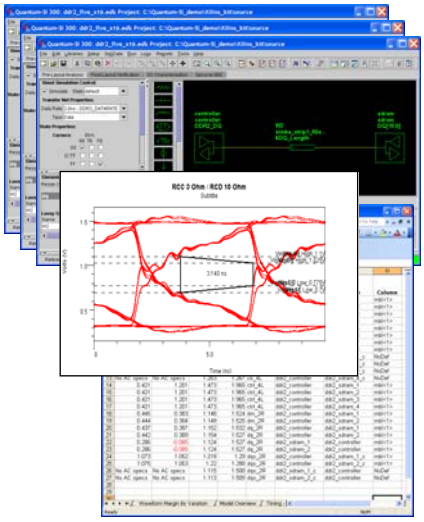
Pre-Route SI Exploration



- Pre-route simulations model planned
  - Drivers
  - Receivers
  - Routing topology & lengths
  - Termination
- Simulated interconnect delays are extracted and plugged back into the Executable Timing Model
- Setup and hold margins are calculated for temperature, process and voltage corners

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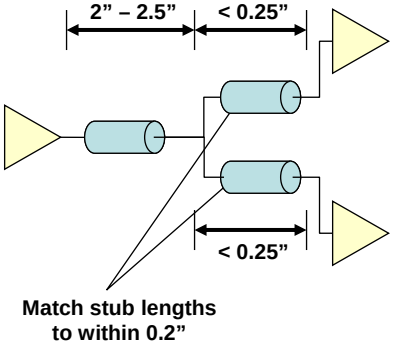
Driving Physical Design



- Pre-route SI/Timing analysis defines PCB routing rules
- Rules usually include pin ordering, length limits and stub matching
- Driving automated rules into PCB CAD is essential

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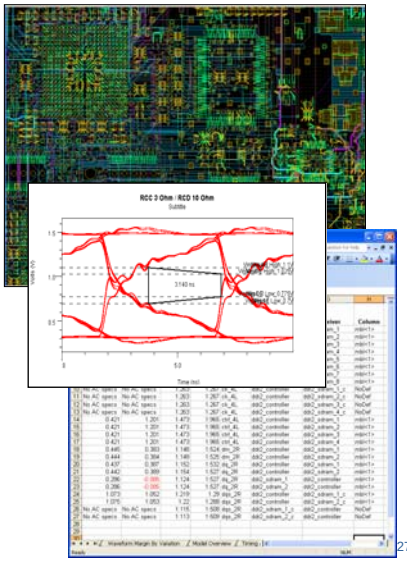
Post-Route Validation



- Routed topologies are extracted from PCB database and simulated
- Simulated interconnect delays are extracted and plugged back into system timing model
- Setup and hold margins are calculated for temperature, process and voltage corners

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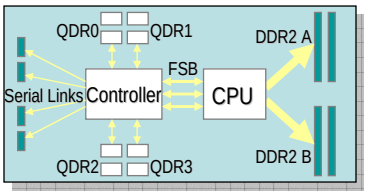
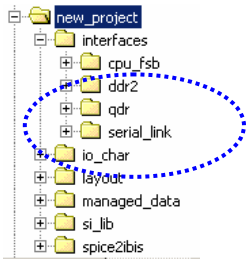
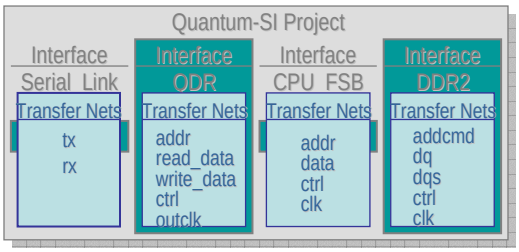
Design Analysis Reuse



Once all the SI/timing data for an interface has been captured, it should be possible to directly reuse that information for multiple instances in a project or other projects





Each interface kit contains net class schematics, timing data & SI models

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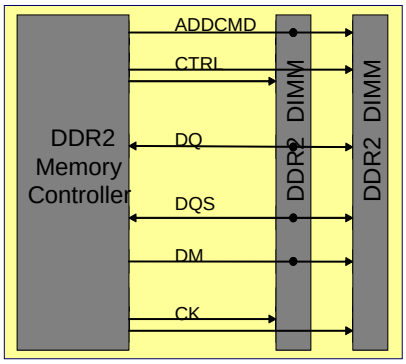
Case Study: DDR2 System Memory



- DDR2 supports one or two DIMM modules
- DIMM Modules
  - Registered and Unbuffered
  - 4 to 18 memory devices
- Two module, data write transaction is presented here
- Complete case study:

  "Features and Implementation of High-Performance 667Mbs and 800Mbs DDRII Memory Systems"
  - Presented by Micron & SiSoft
  - DesignCon West, 2005
- http://www.sisoft.com/papers.asp

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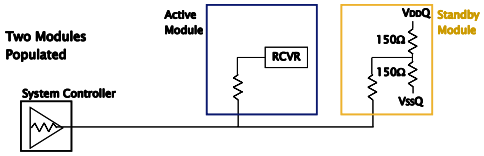
DDR2 Data Write Configuration



Write Configurations

Configuration	Write to	DQ Active-Term Resistance				
		Controller	Dram at Slot 1		Dram at Slot 2	
			Front Side	Back Side	Front Side	Back Side
2R / 2R	Slot 1	No Term	No Term	No Term	50 or 75 ohm	No Term
	Slot 2	No Term	50 or 75 ohm	No Term	No Term	No Term
2R / 1R	Slot 1	No Term	No Term	No Term	50 or 75 ohm	Empty
	Slot 2	No Term	50 or 75 ohm	No Term	No Term	Empty
1R / 2R	Slot 1	No Term	No Term	Empty	50 or 75 ohm	No Term
	Slot 2	No Term	50 or 75 ohm	Empty	No Term	No Term
1R / 1R	Slot 1	No Term	No Term	Empty	50 or 75 ohm	Empty
	Slot 2	No Term	50 or 75 ohm	Empty	No Term	Empty
2R / Empty	Slot 1	No Term	150 ohm	No Term	Empty	Empty
Empty / 2R	Slot 2	No Term	Empty	Empty	150 ohm	No Term
1R / Empty	Slot 1	No Term	150 ohm	Empty	Empty	Empty
Empty / 1R	Slot 2	No Term	Empty	Empty	150 ohm	Empty

- Termination strategy is dynamic; depends on how many DIMMs are present and which device is receiving
- Simulation environment must switch receiver models based on which case is being analyzed

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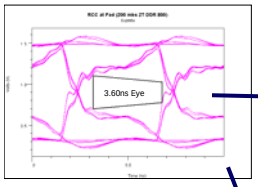
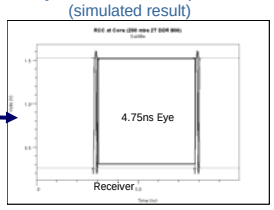
Slew Rate Derating – "Virtual Eye"

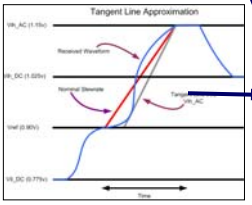
Eye at device pad
(simulated result)



Eye at receiver output
(simulated result)

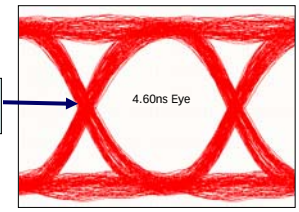


Waveform derating scheme



Waveform processing

Virtual eye at receiver
(computed result)



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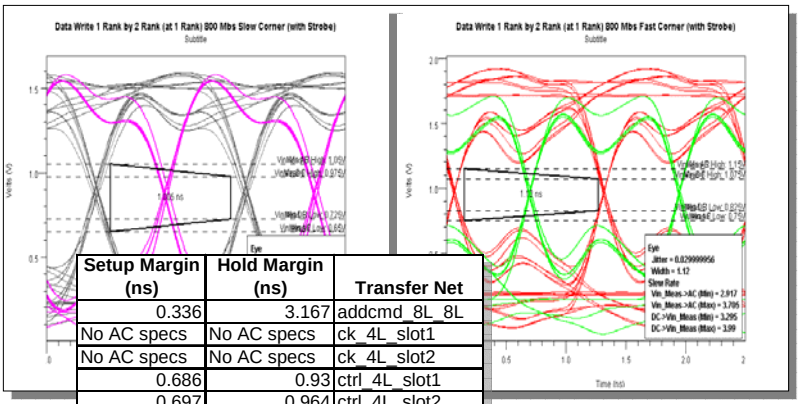
DDR2 Analysis Results

Data Write Slow / Fast Corners



Setup Margin (ns)	Hold Margin (ns)	Transfer Net
0.336	3.167	addcmd_8L_8L
No AC specs	No AC specs	ck_4L_slot1
No AC specs	No AC specs	ck_4L_slot2
0.686	0.93	ctrl_4L_slot1
0.697	0.964	ctrl_4L_slot2
0.468	0.205	dm_2R_2R
0.213	-0.148	dq_2R_2R
1.155	0.944	dqs_2R_2R

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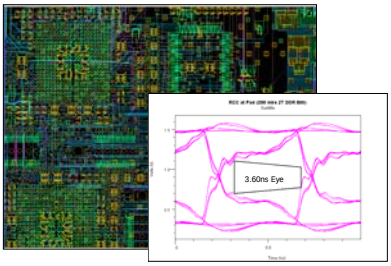
Summary



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0.686	0.93	ctrl_4L_slot1
0.697	0.964	ctrl_4L_slot2
0.468	0.205	dm_2R_2R
0.213	-0.148	dq_2R_2R
1.155	0.944	dqs_2R_2R

- High-speed system design requires a rigorous, repeatable methodology for achieving Timing Closure
- Static Timing, Signal Integrity, and physical design rules are all interrelated
- An Executable Timing Model allows for a user to validate all transactions across all cases
- Signal Integrity analysis must be performed in accordance with the system timing model

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27. Aug. 2006 Security Level:

Statistical Eye Simulation Requirements

Asian IBIS Summit, Shanghai China
October 27, 2006

Huang Chunxing
huangchunxing@huawei.com

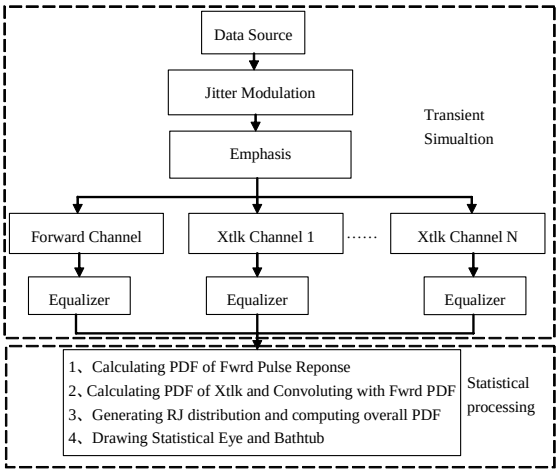
HUAWEI TECHNOLOGIES Co., Ltd.

Statistical Eye Simulation Flow

Simulation flow:

- **Time domain simulation**
- **Statistical post-processing**

The data source could be signal source or real serdes model.

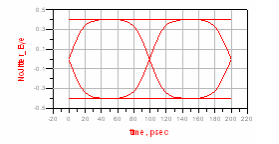


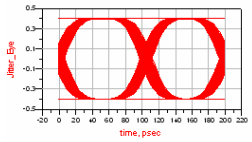
Simulation Requirements

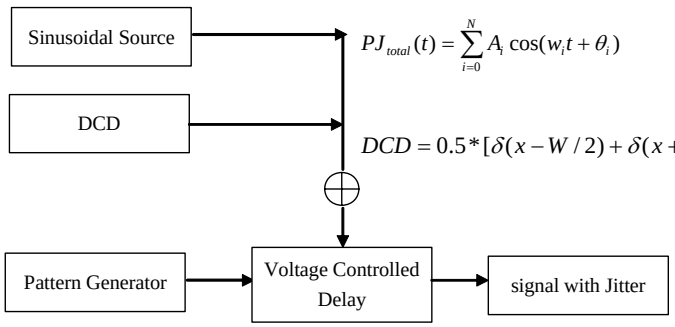
- Simulation platform should support IBIS or Hspice serdes model.
- Simulation platform should simulate channel responses by using convolution method.
- Simulation platform should easily realize jitter modulation, equalizer and emphasis.
- Simulation platform should support equalizers, such as LFE, DFE and CTE.
- Powerful post-processing ability.
- Simulation platform may further support co-simulating with Matlab for user defined statistical processing.

Jitter Modulation

- Using Voltage Controlled Delay to add jitter
- Jitter at transmitter includes PJ, DCD
- RJ will be consider in statistical post-processing

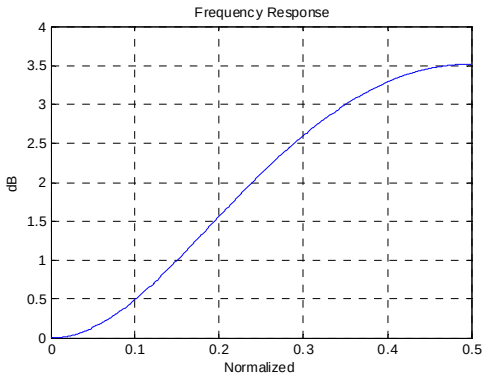


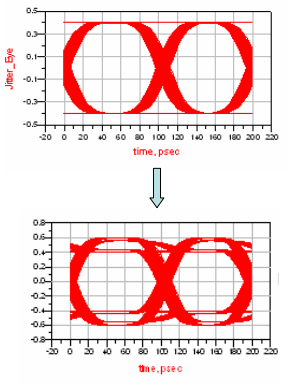




Emphasis

- Emphasis technique includes pre-emphasis and de-emphasis
- Both pre-emphasis and de-emphasis could be expressed as FIR filter

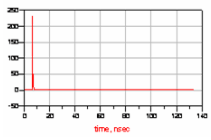




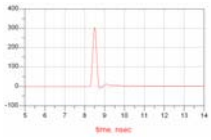
Channel Models

- **Channel models, including fwrd and xtlks, could be expressed in S-parameter**
- **Supporting transient simulation with touchstone files**

Impulse response

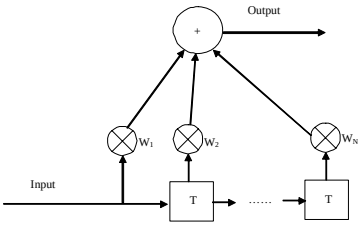


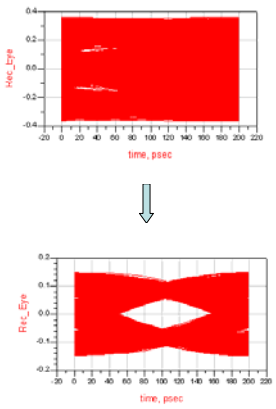
pulse response



Equalizer-LFE

LFE is linear feed-forward equalizer



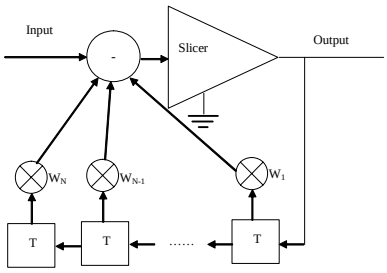


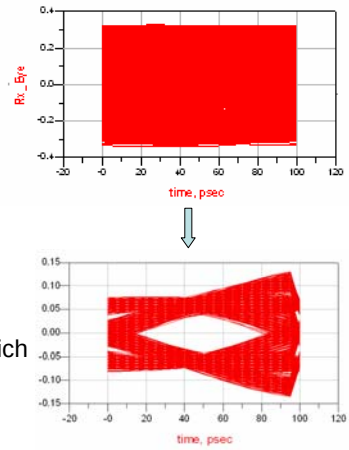
- discrete – usually just one tap per bit
- finite – not long enough to completely correct the impulse response
- May result in noise gain

$$V(T_0) = W_1 * V_{in}(T_0) + W_2 * V_{in}(T_{-1}) + \cdots + W_N * V_{in}(T_{N-1})$$

Equalizer-DFE

DFE is decision feed-back equalizer





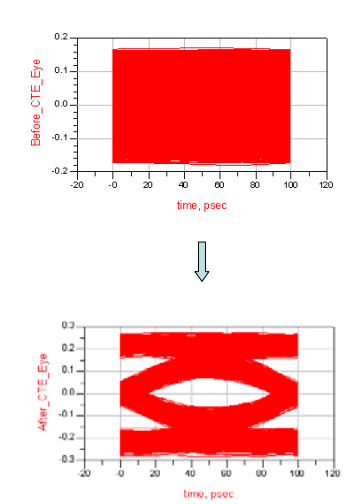
- DFE uses a feedback loop of the desired signal which is decoded from the output of a slicer
- DFE can further correct the residual ISI

$$V(T_0) = V_{in}(T_0) - W_1 * D(T_{-1}) - W_2 * D(T_{-2}) - \cdots - W_N * D(T_{-N})$$

Equalizer-CTE

- **CTE is continuous time equalizer**
- **CTE model is an ideal circuit with the desired pole, zero response.**
- **p0 and z0 are programmable**

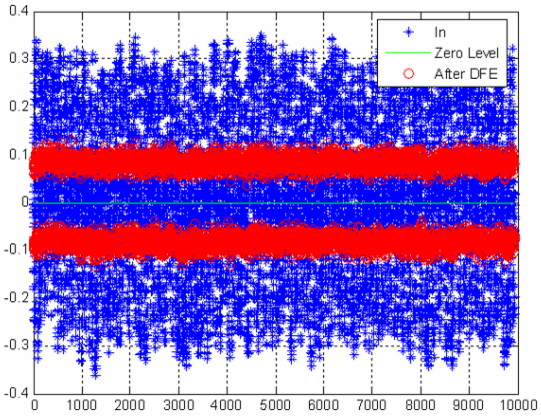
$$H_{CTE}(f) = a\frac{p_0}{z_0}\frac{(s+z_0)}{(s+p_0)}$$



Equalizer-Algorithm

Calculating the optimal sampling point and equalizer coefficients

- **LMS adaptive algorithm**
- **Zero Forcing algorithm**

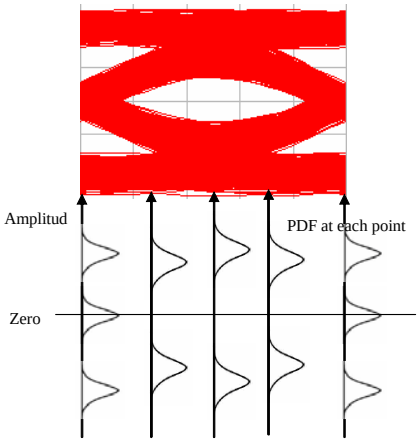


Statistical Post-processing

Calculating Forward channel PDF

1.Overlapping each bit at one UI range.

2. At each UI sampling point, computing PDF of Overlapping data.



Statistical Post-processing

Xtlk Convolution Method

1.Interpolating each Xtlk channel responses to small enough time interval

2. Overlapping each bit in one UI range

3. Computing PDF of Overlapping data at each UI sampling point

4. Averaging PDFs through whole UI sampling points to get the average PDF.

5. Repeating 1-4 for each aggressors.

6. Convolving average PDFs of all aggressors to get the whole crosstalk PDF.

Charles Moore presented convolution method in his paper "Computing effect of cross talk using Convolution" at 802.3ap.

http://grouper.ieee.org/groups/802/3/ap/public/channel_adhoc/moore_c1_0305.pdf

Statistical Post-processing

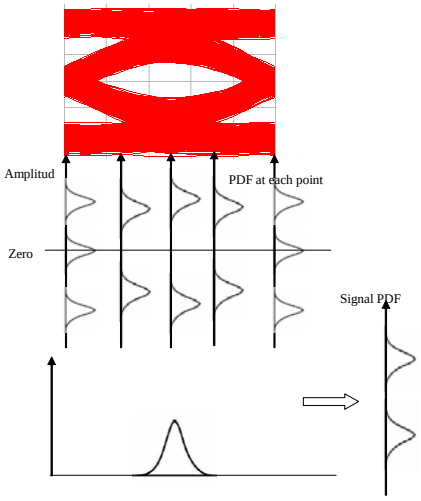
Random Jitter

Random Jitter distribution

$$P_{RJ} = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{t^2}{2\sigma^2}}$$

Overall PDF

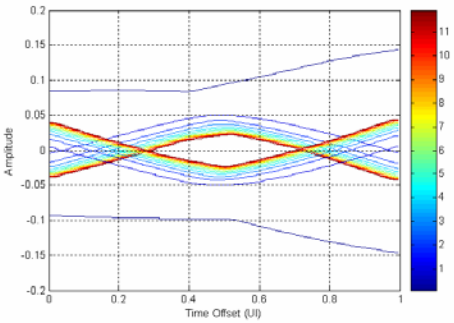
$$P(ISI, \tau) = \int_{-\infty}^{\infty} P(ISI, \tau + \upsilon) \cdot P_{RJ}(\upsilon) d\upsilon$$



Statistical Post-processing

Statistical Eye

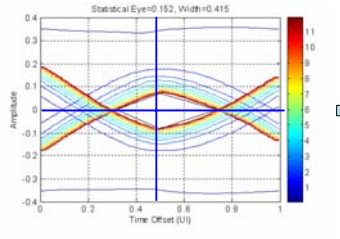
- Statistical eye is set of probability contours
- Horizontal axis is with respect to sampling point
- Vertical axis is with respect to signal amplitude
- Different colored lines represent BER

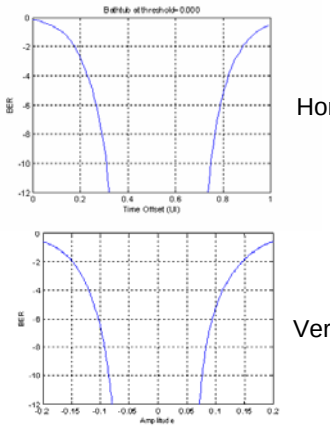


Statistical Post-processing

Bathtub

- Intercept through statistical eye along horizontal axis to get horizontal Bathtub at definite voltage
- Intercept through statistical eye along vertical axis to get vertical Bathtub at definite sampling time

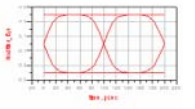




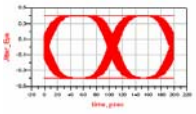
Horizontal

Vertical

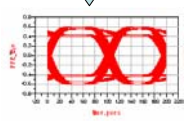
Overall Simulation Eye Flow



Transmitter Eye

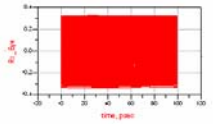


Eye after Jitter Modulation

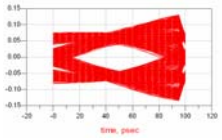


Eye after Emphasis

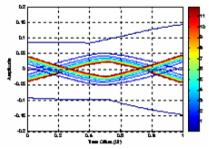
Channel

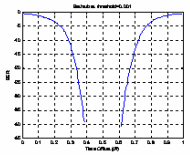


Eye after Channel



Eye after Equalizer





Example - Channel pre-simulation

Assumed conditions:

10Gbps NRZ, PRBS 23, 100000 bits, amplitude 800mvpp, Tr(f) = 24ps

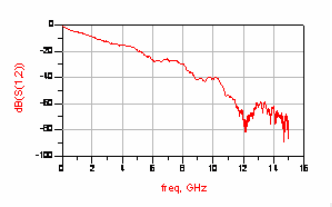
0.15UIpp DJ = 0.05UI DCD+0.1UI PJ, 0.15UIpp RJ @10^{-12}BER

BER = 1e-12 (2*Q=14.069)

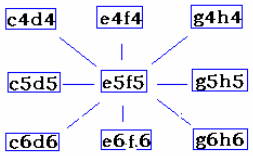
3tap de-emphasis, 5tap DFE

Slice voltage: 10mV

Forward Channel



Eight crosstalk channels



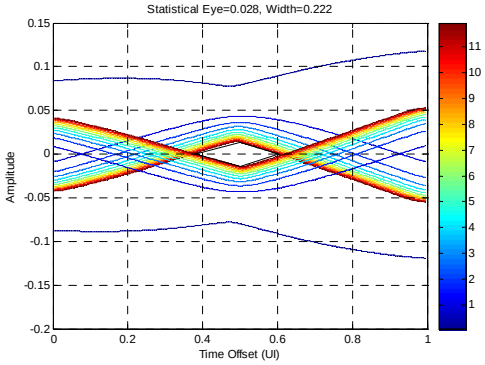
Example - Channel pre-simulation

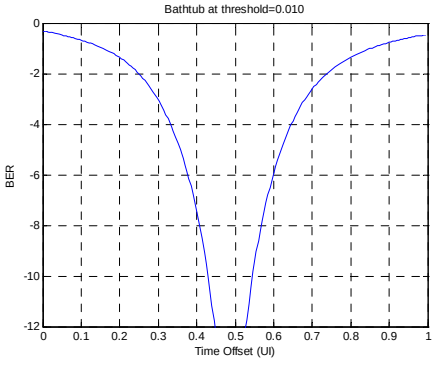
- Simulation result:

  28mv eye-height

  0.222UI eye-width

- It shows that the channel could undertake 10Gbps data transmission





Conclusion

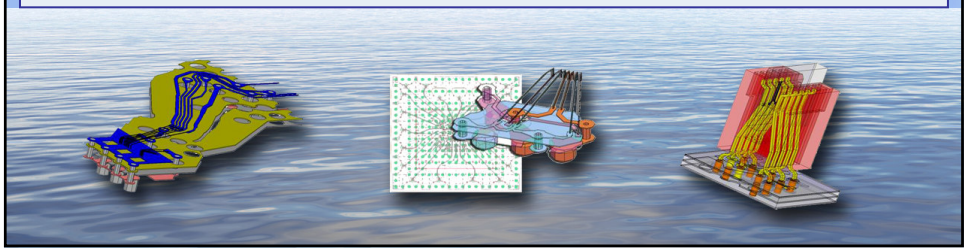
- **Basic method of statistical eye simulation has been presented here**

- **An ideal platform to realize statistical eye simulation:**
  - ✓ Jitter Modulation at transmitter
  - ✓ Pre-emphasis or de-emphasis
  - ✓ Supporting Forward channel, Xtlk channel models
  - ✓ Equalizer
  - ✓ Statistical post-processing

Methodologies for Multi-Gigabit Interconnect Design

Andrew Byers, Application Engineer, abyers@ansoft.com
Lawrence Williams, Director Business Development, williams@ansoft.com

ASIAN IBIS Summit Shanghai, PRC October 27, 2006



Multi-gigabit Devices

- The need for devices that are smaller and faster is driving multi-gigabit applications in several industries.
- Slower parallel busses are being replaced by much faster serial busses (eg. PCIExpress, SATA, FBDIMM).
- Faster data speeds present a new set of challenges for signal and power integrity. ***New tools and methodologies are needed.***

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Multi-gigabit Design Challenges

- Before engineering teams can make it smaller, faster or better performing they require design strategies and tools that can:
  - **Extract** GHz-accurate signal path models based on the entire physical interconnect.
  - **Simulate** and optimize the performance of these high speed data lanes in time and frequency.
  - **Validate** the overall system performance, incorporating **IBIS** and/or transistor-level representation of critical components

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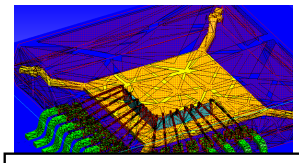
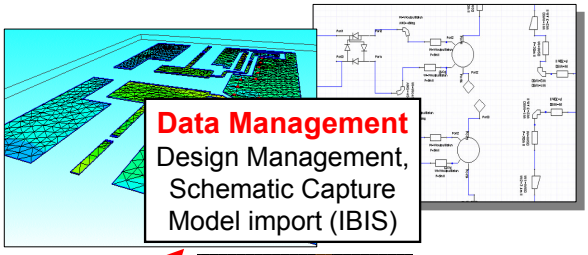
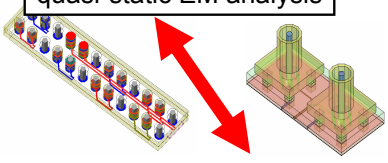
Electromagnetic modeling for Multi-gigabit Channel Design



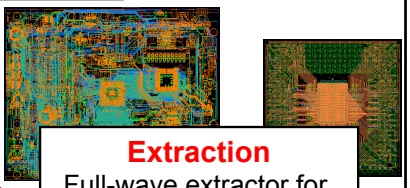
Extraction
3D Full-wave and quasi-static EM analysis



Data Management
Design Management, Schematic Capture Model import (IBIS)



Circuit Simulation
High capacity and accuracy, Time and frequency domains



Extraction
Full-wave extractor for entire package and PCB

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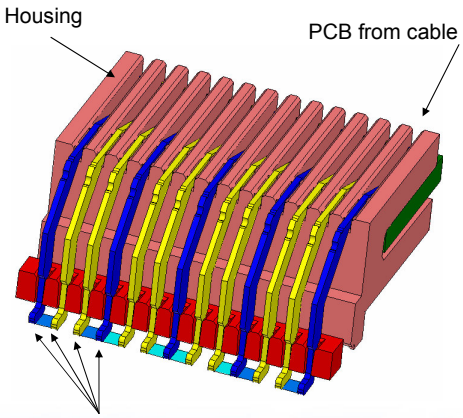
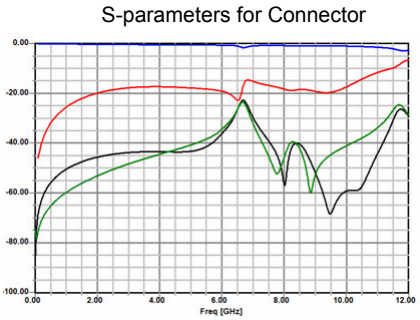
Simulation Requirements

- 3D interconnect components should be modeled using full-wave electromagnetic solvers that produce S-parameters.





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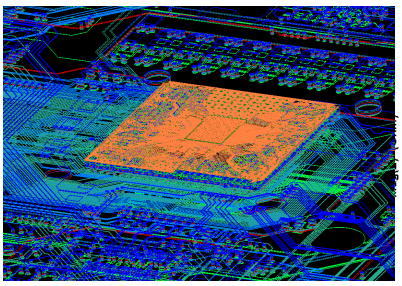
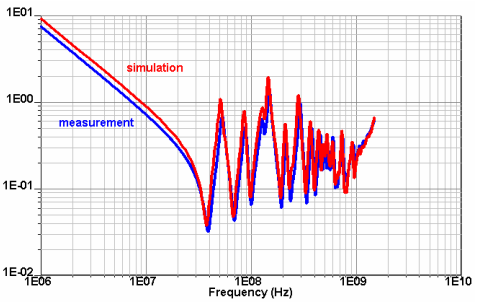
Simulation Requirements

- Multi-gigabit backplanes must meet complex power-delivery requirements, and simulation tools are needed to verify designs before tapeout.





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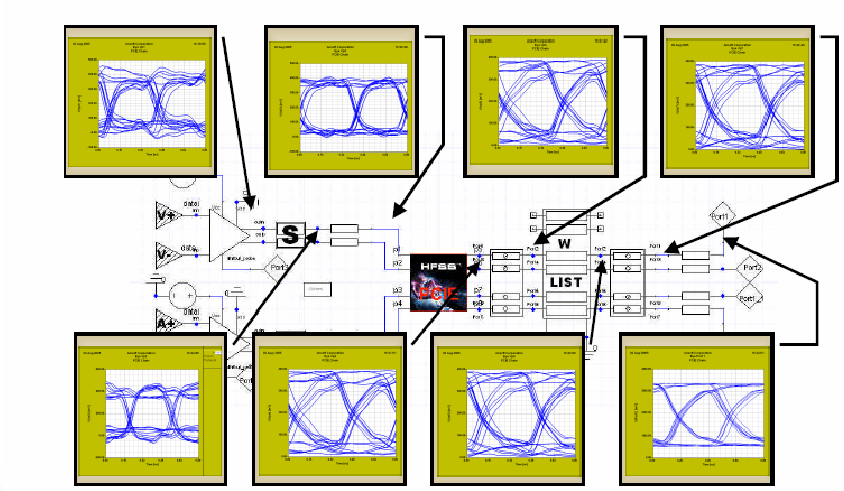
Simulation Requirements

- Simulator must provide reliability and capacity by correctly including S-parameters along with other model types in transient simulations of channel.



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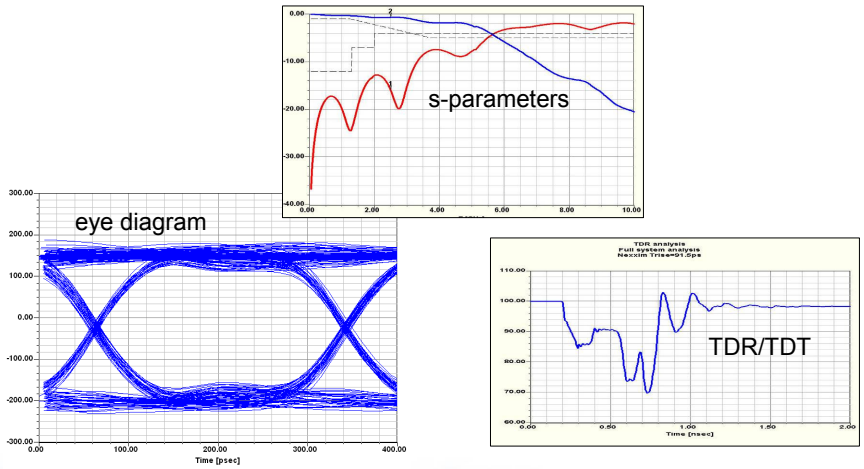
Simulation Requirements

- Multi-gigabit channel designs require both frequency- and time-domain simulations to meet required specifications.



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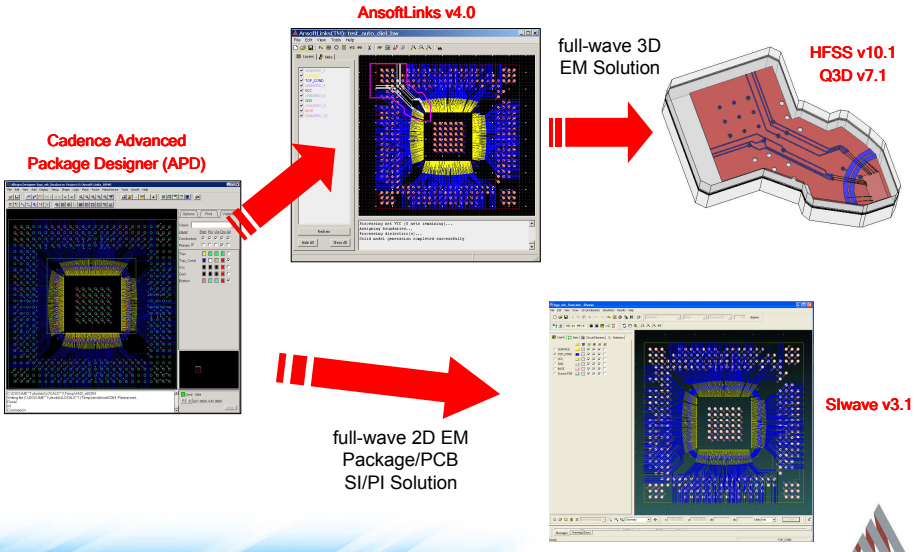
Simulation Requirements

- Ability to transfer data from layout programs to EM extraction tool.



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Phases of Interconnect Design

Phase 1: Feasibility
Which technologies to use?
First-pass SI and PI designs

Phase 2: Design
SI and PI optimization
Refinements to interconnect channel
Detailed simulations with IBIS buffer models

Phase 3: Validation
Layouts completed
Extract critical nets – validate SI and PI
SSO simulations to check jitter specs

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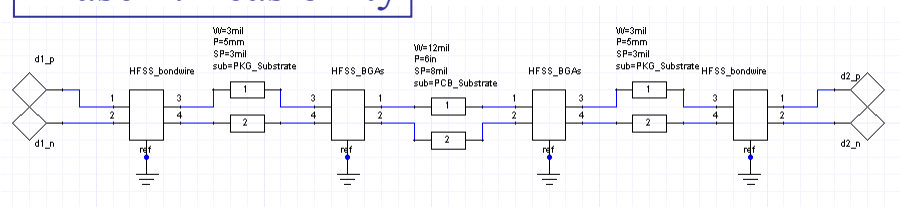
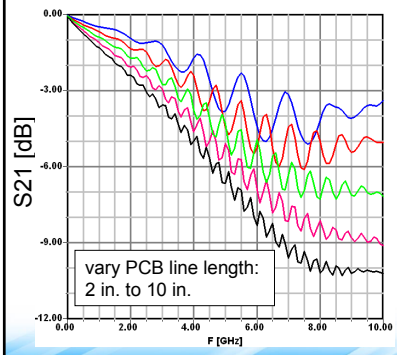
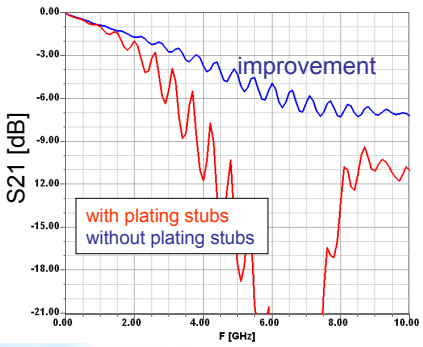
Phase 1: Feasibility



Explore Design Space



Investigate Technology Choices



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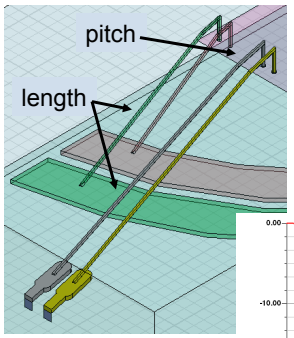
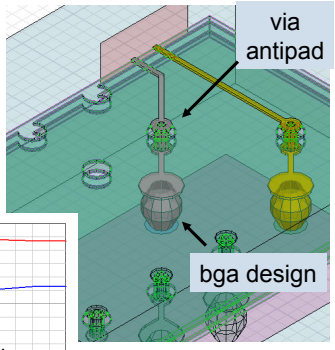
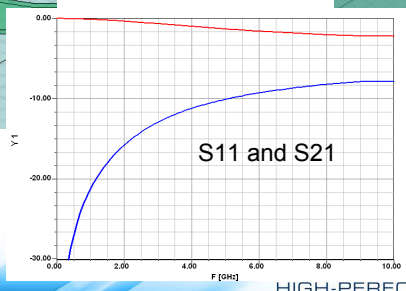
Phase 2: Design

Optimize designs of the interconnect components of the multi-gigabit channel.



"virtual prototyping"





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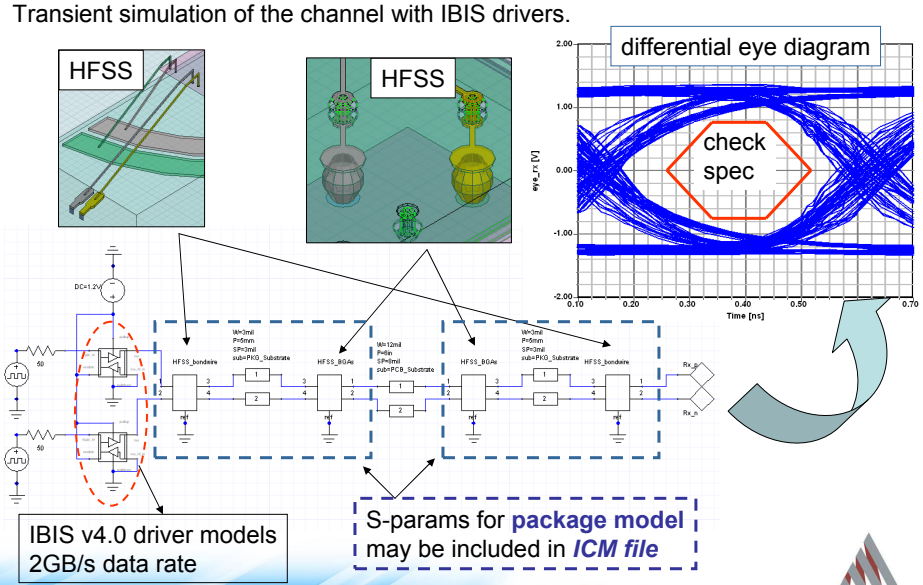
Phase 2: Design

Transient simulation of the channel with IBIS drivers.



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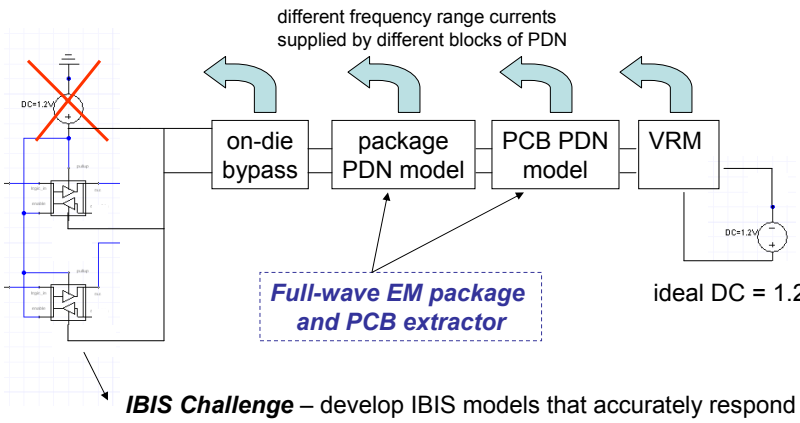
Phase 2: Design

For more detailed simulation – also include ***Power Distribution Network (PDN)***



IBIS Challenge – develop IBIS models that accurately respond to noise on power/gnd rails caused by dI/dt effect.

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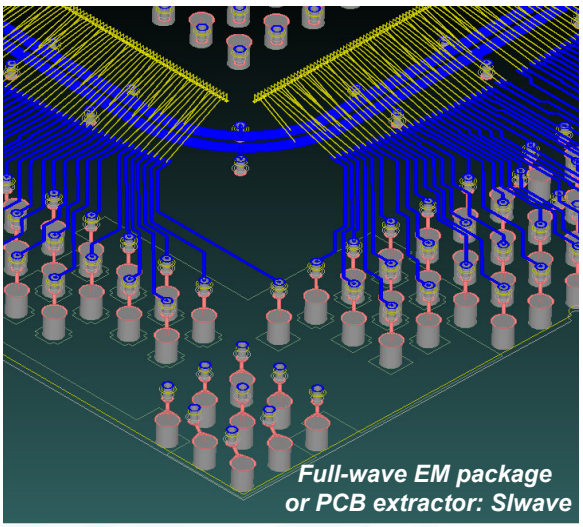
Phase 3: Validation



Include more nets to simulate any impact of crosstalk and other post-layout design issues.

16-channel, 32-port S-parameter File

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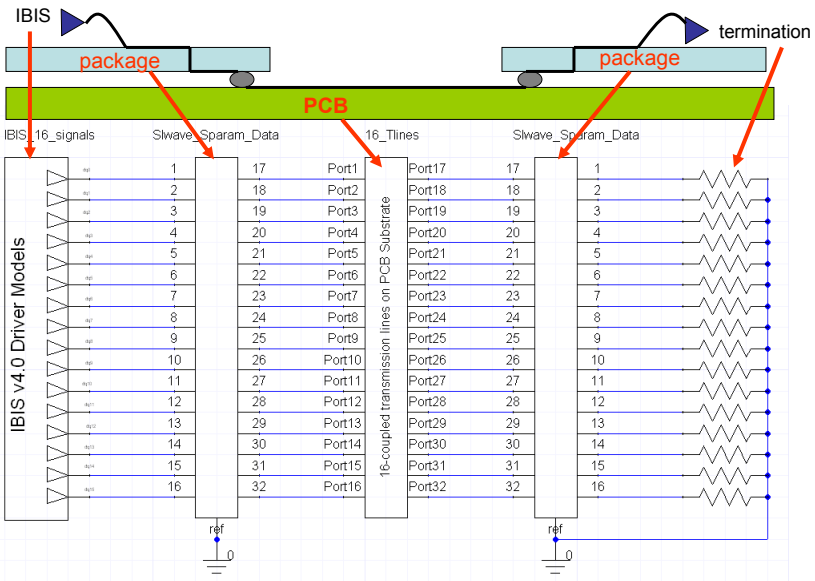
Phase 3: Validation



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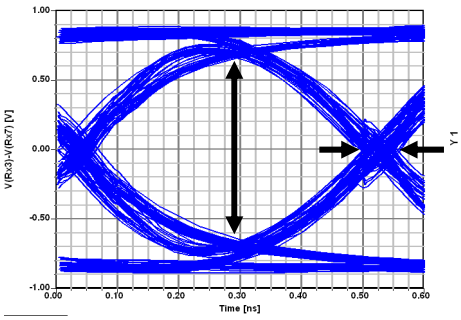
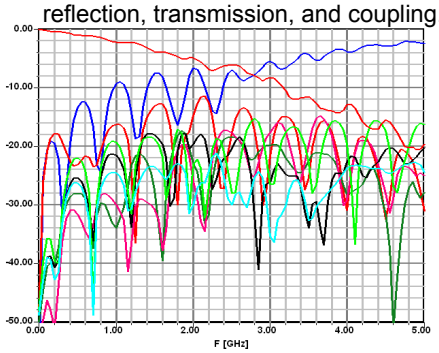
Phase 3: Validation

Time-domain:
Inspect eye opening for spec qualification, jitter, fidelity.



Frequency-domain:
inspect channel s-parameters for reflection, transmission, and coupling.



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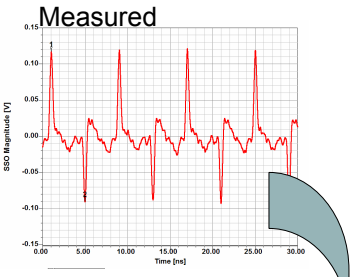
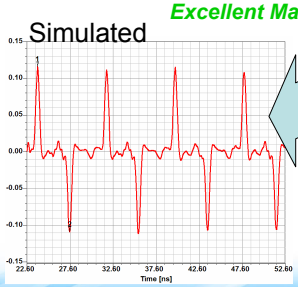
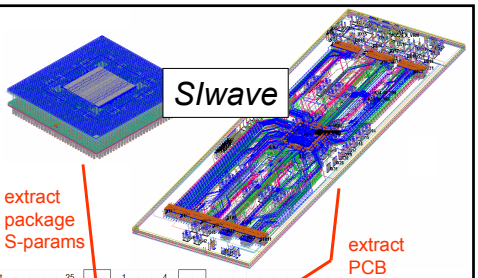
Customer Case Study



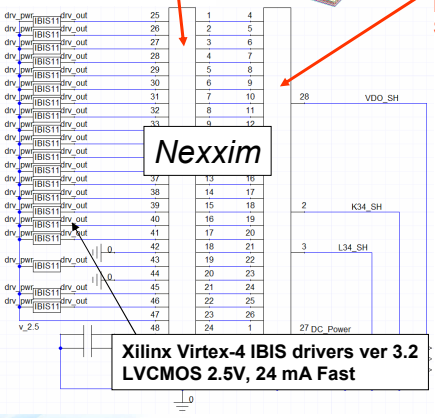
Excellent Match





extract package S-params

extract PCB S-params



Xilinx Virtex-4 IBIS drivers ver 3.2
LVCMOS 2.5V, 24 mA Fast

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Summary

- Electromagnetic-based modeling tools play a critical role in multi-gigabit channel design.
- The inclusion of S-parameters in IBIS models will open up higher bandwidths for signal integrity and augment complete SSN analyses for power integrity.
- Thank you very much!

HIGH-PERFORMANCE EDA

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System-Level SSO Simulation Techniques with Various IBIS Package Models

Asia IBIS Summit (China)

Sam Chitwood, samchitwood@sigrity.com
Jack W. C. Lin, jackwclin@sigrity.com
Raymond Y. Chen, chen@sigrity.com

October 27, 2006, Shanghai

SIGRITY

Presentation Outline

Simultaneous Switching Output Noise Analysis – a.k.a SSO/SSN

- Fundamentals of SSO Mechanisms
- Typical SSO Simulation Setup
- IBIS Package Modeling Choices
- Case study to compare the package models
- Summary

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The SSO / SSN Problem

- SSO, SSN, Power/Ground Bounce, Delta-I Noise, …
  - Simultaneous Switching Output, Simultaneous Switching Noise, di/dt, power and ground voltage fluctuations, etc.
- Two types: I/O switching and Core logic switching
  - This presentation focuses on I/O SSO analysis

3

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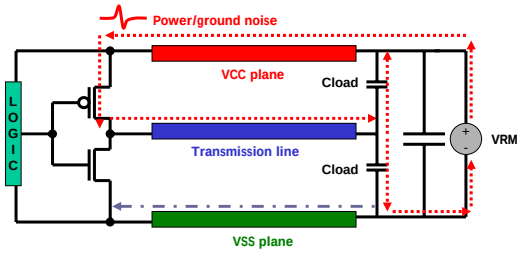
Fundamentals of I/O SSO Mechanisms



When the output is driven high, the transmission line is connected to the PWR net at the driver. When the output is driven low, the transmission line is connected to the GND net at the driver. This connection forms one end of the sig/gnd or sig/pwr loop.

The capacitive loads (for typical CMOS technologies) complete the sig/gnd and sig/pwr loops. Return current takes the path of least impedance, so PDS performance is key.

All three loops are important factors for optimizing signal quality and reducing PDS noise.

4

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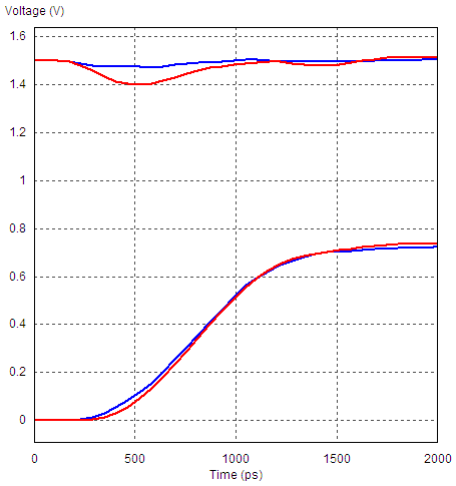
Fundamentals of I/O SSO Mechanisms

- SSO is a combination of signal and power integrity issues
- Affects signal edge rate, timing and voltage margins
- System-level issue involving both packages and PCBs
- Multiple signal net crosstalk mechanisms – trace / via / pin
- Two components of PDS noise
  - PDS current supplied to devices
  - Return currents from I/Os
- BGA inductance presents a fundamental limitation on the PCB's PDS freq. range; the package is responsible for decoupling above that freq. region
- PCB layout can only do so much – it cannot solve package design problems



Blue – Single I/O switching results
Red – Two I/Os switching results

5

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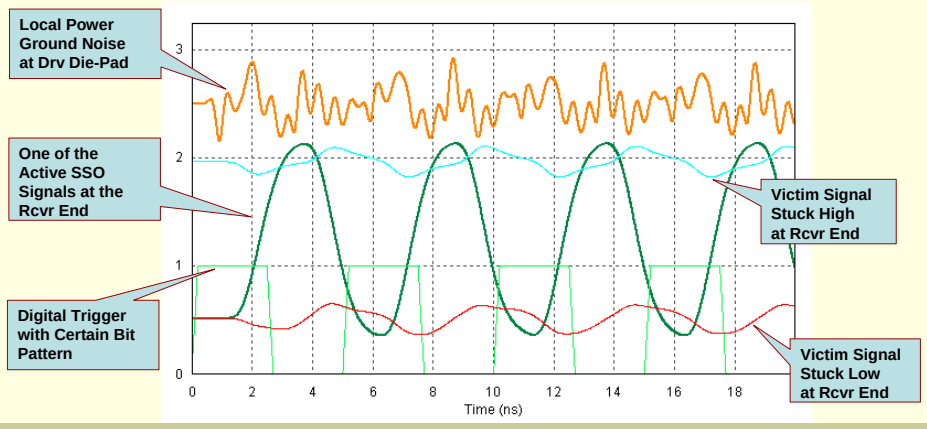
Typical SSO Analysis Results



Set two of the data bits as stuck high and stuck low victims. These results can assist with more in-depth analysis of the power and ground rail fluctuations.

6

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Typical IBIS-based SSO Analysis Setup

- PCB layout (including dielectric information)
- VRM location and model
- Decoupling capacitor locations and models
- Power, ground, and signal nets of interest
- Any interconnect terminations
- Switching patterns
  - PRBS recommended to find eye diagram and max PDS noise (simple 1010 repeating patters do not always yield worst-case)
- IBIS models
  - Drivers and receivers
  - On-die models highly recommended
  - Split c_comp and [Pin Mapping] should be requested from vendors for improved accuracy, otherwise make assumptions
  - IBIS supports multiple package models – which one to use?

7

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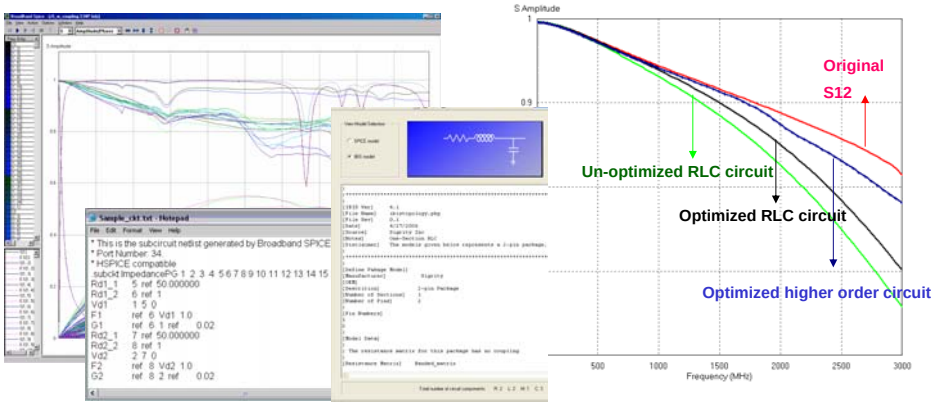
Frequency Response and Accuracy of Various SPICE Equivalent Circuits for a Pkg I/O's S[1,2]



S-parameters are typically the most accurate modeling technique, but practically they can be difficult to use in system-level SSO simulations: more difficult to extract than RLCs, increased SSO simulation complexity, causality/passivity issues, and no formal integration with the IBIS specification makes simulation setup difficult in some tools.

8

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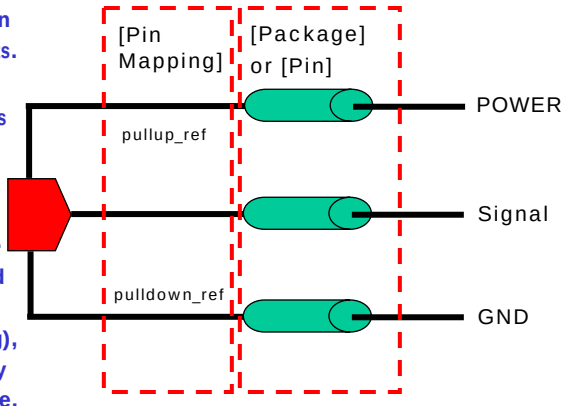
Confusion with [Package] and [Pin] in IBIS

- The [Package] and [Pin] constructs do not allow any coupling between the power, signal, and ground nets.
- Therefore, these package models are only appropriate for two types of situations: ideal pwr/gnd simulations or packages that truly have negligible coupling between these three nets (e.g. leadframe).
- For packages that have power and ground planes (pins are inter-connected and nets have coupling), a per-pin RLC PDS model is usually not appropriate without great care.
- If RLCs for POWER and GND pins are present, how should they be interpreted / connected?



9

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[Package Model] Can Include Coupling

- [Model Data] allows self and mutual inductances, capacitances, and resistances to be included
- The mutual terms are necessary to include all SSO mechanisms
- Power and ground pins can be lumped together to account for their interconnected nature on the package (one RLC for entire PDS)
- RLCs for individual power and ground pins are still not appropriate in general cases

```
[IBIS Ver]          4.1
[Comment Char]      !_char
[File Name]         ibis_wirebond.pkg
[File Rev]          1.0
[Date]              8/9/2006
[Source]            Sigrity Extractor
[Notes]             One-Section RLC
[Disclaimer]        178-pin package
[Copyright]
!
!*************************************
!
[Define Package Model]  ibis_wirebond
[Manufacturer]          Sigrity
[OEM]                   Sigrity
[Description]           178-pin Package
!
[Model Data]
!
[Inductance Matrix]     Sparse_matrix
[Row]     B19
B19      1.66704e-009
D3       3.71638e-010
W17      3.60196e-010
U16      3.90649e-010
```

10

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Case Study: PCB DDRII Analysis to Compare the Three Package Choices

Analysis Methodology

- DDRII 800 interface (typical configuration)
- Three package choices were compared
  - [Pin] RLC model for signals only (no per-pin RLCs for PDS)
  - [Package Model] with full power/signal/ground coupling
  - Broadband S-parameter model
- Analyze PDS noise at the PCB, I/O waveforms at the receivers, and quiet nets (stuck high and low)
- 6 and 14 switching nets (8 and 16 I/Os total)
- On-die models were not included to enhance the waveform differences between the configurations

11

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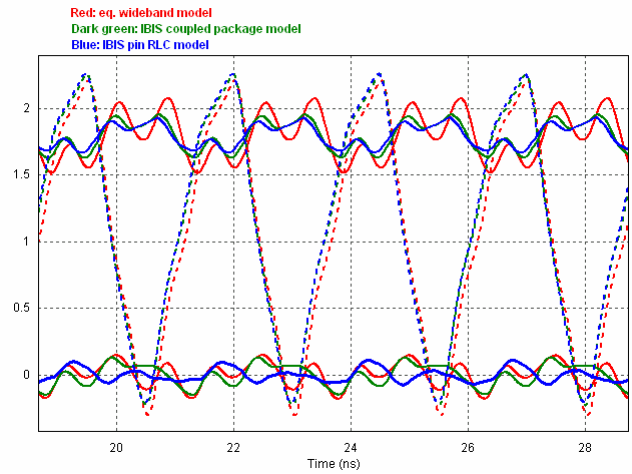
DDRII800 results – SSO signal noise 8 bits with 2 victims (stuck high and low)



The three package models show their fundamental differences in capabilities.

The two IBIS package models show similar results for the stuck high line. This is because the stuck high noise will quite often follow the overall PDS noise when signals are only referenced to GND.

The stuck low results are quite different because signal-signal crosstalk can be a significant source of noise (not in the [Pin] model).

Broadband model yields the largest victim net SSO noise.

12

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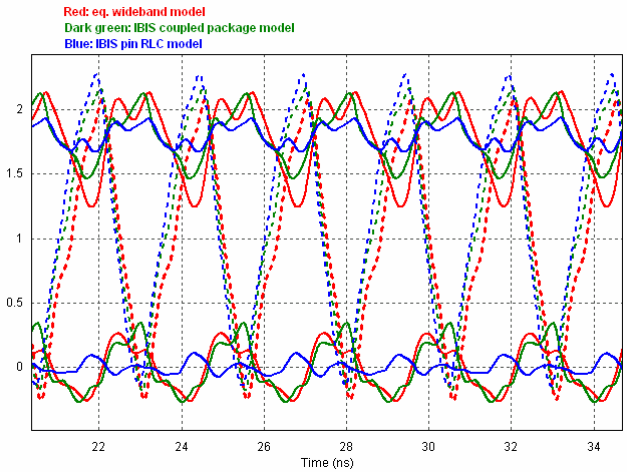
DDRII800 results – SSO signal noise 16 bits with 2 victims (stuck high and low)



For the 16 driver case, the three package models show significant differences in the results. This is because the package PDS impedance and crosstalk are dominant factors in the overall simulation.

In the simulation results shown thus far, the PCB had excellent characteristics regarding PDS impedance and signal-signal crosstalk. This was purposely done in order to highlight the differences between the package models.

Broadband model yields the largest stuck high noise only.

13

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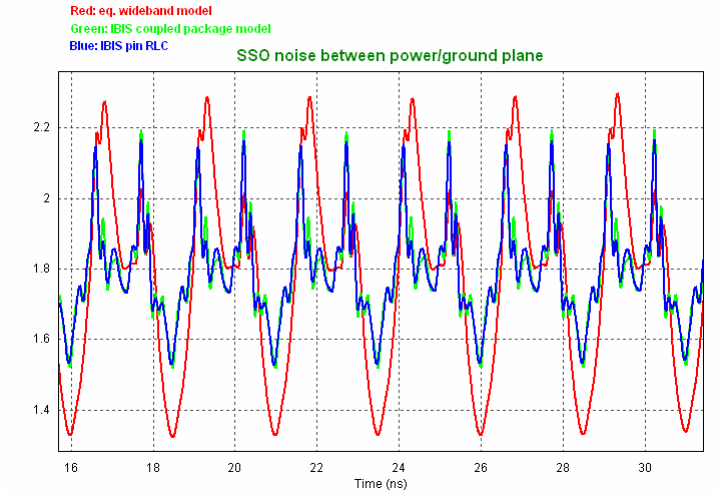
DDRII800 results – PDS Noise for 16 bits Package Impedance is dominant factor



For this case, the package is the dominant factor in the system's PDS impedance (the PCB PDS design is excellent).

Because the IBIS package PDS models are not as accurate as the S-parameter model, the results will typically be quite different in this scenario.

14

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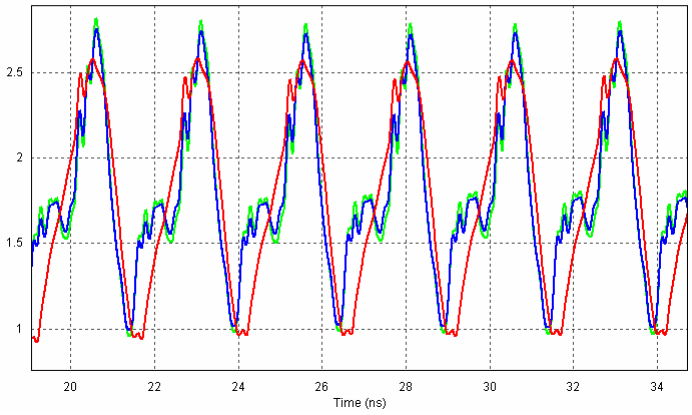
DDRII800 results – PDS Noise for 16 bits
PCB Impedance is dominant factor

Red: eq. wideband model
Green: IBIS coupled package model
Blue: pin RLC model

SSO noise between power/ground plane



For this case, the PCB is now the dominant factor in the system's PDS impedance.
(The PCB impedance was intentionally degraded by removing some decaps.)

Therefore the choice between the three package models is not as critical and may yield similar results. This facilitates relative study optimization.

15

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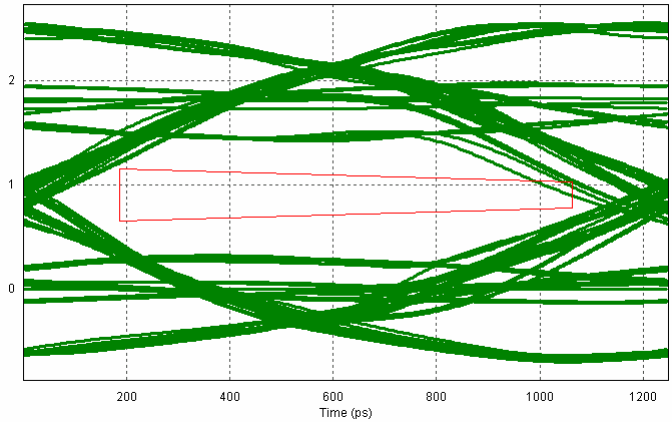
Eye Diagram for DDRII800
IBIS [Pin] RLC model

Data eye for IBIS pin RLC case



16

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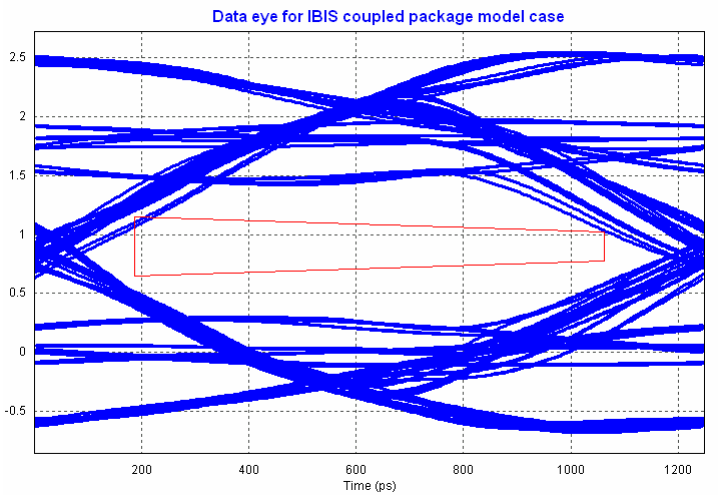
Eye Diagram for DDRII800
IBIS [Package Model] with coupled RLCs



17

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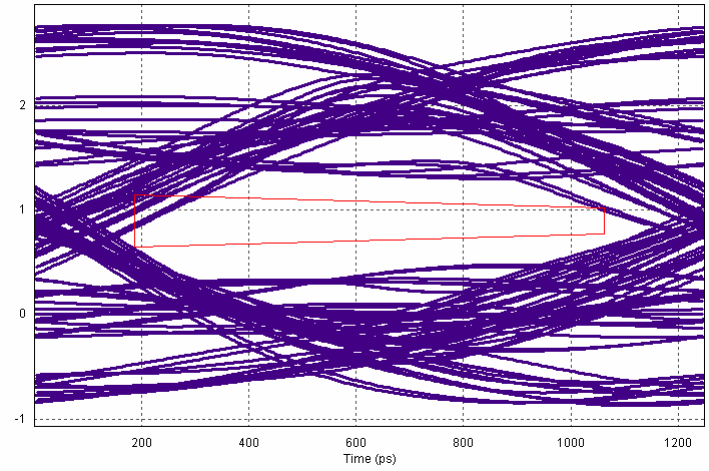
Eye Diagram for DDRII800
Broadband S-parameter package model



18

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Conclusions and Summary

- SSO noise is generated in circuits through many mechanisms. The primary contributors are 1) the many forms of crosstalk and 2) the impedance and interactions of the package and PCB power distribution systems.
- In full SSO simulations, it is difficult to separate the contribution of these two factors. However, the components can be separated with specially designed simulations that isolate particular effects.
- RLC models can over- or under-estimate the true behavior of the package. The RLC model should be sufficiently accurate over the necessary signal bandwidth.
- [Pin] package models have limited use in SSO simulations since they lack the coupling between the PDS and the signals. They are most appropriate for ideal PDS simulations.
- [Package Model] is very appropriate for SSO trend studies and "what-if" analysis.
- S-parameter package models are most appropriate for highly accurate SSO sign-off.
- The package may or may not be the dominant factor in system-level SSO analysis. If the package [Pin] model is the only model available, relative PCB optimization studies can still be performed.

19

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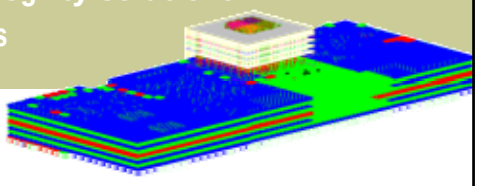
Thank You!

Advanced Power and Signal Integrity Solutions
for Chips, Packages and Boards



20

Using S-parameters for behavioral interconnect modeling

Asian IBIS Summit

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High-Speed System Lab, EDA Dept. ZTE Corporation
Zhu.shunlin@zte.com.cn

October 27, 2006

ZTE中兴

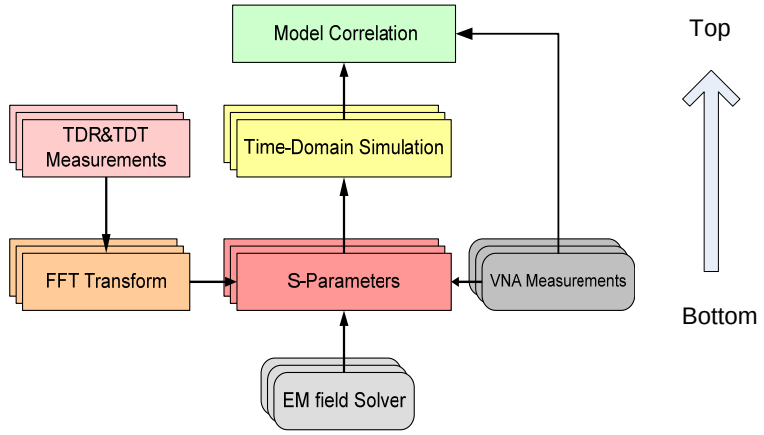
Agenda

- Using S-parameters for high-Speed digital design
- Describing passive interconnects in ICM
- ICM&IBIS
- A solution for package modeling using S-parameters
- Summary

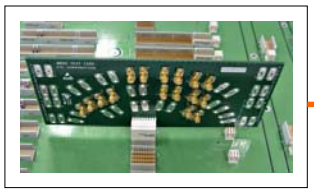
Using S-parameters for high-Speed Digital Design

- The signal integrity simulation of high-speed digital design requires that the interconnect modeling must be valid over a wide bandwidth.
- S-parameters can be generated by 3D EM field solver or by VNA and TDR/TDT measurements.
- S-parameters can be used to generate distributed models for transmission line and vias.
- S-parameters model can be easily correlated with VNA measurements.
- Circuit simulators can run both S-parameters and RLGC models together in time-domain.

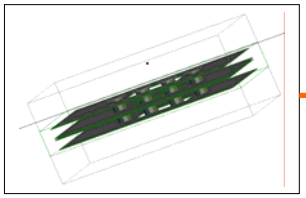
S-parameters Extraction and Correlation



Measurement and 3D EM Solver Modeling



Measurement setup



3D EM Solver Modeling

S-Parameter

S-Parameter touchstone file

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! CORRECTED  DATA
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 0.010000000 3.217487E-02  25.539 1.433922E-02  73.163 7.022051E-04 -164.797 9.721752E-01 -14.501
         1.437112E-02  73.522 8.342298E-02  21.247 9.721735E-01 -14.643 1.031352E-03 152.923
         6.869677E-04 -166.566 9.750083E-01 -14.799 3.180707E-02  24.806 1.426077E-02  73.110
         9.757603E-01 -14.762 1.043164E-03 148.597 1.442420E-02  73.191 3.261170E-02  27.190
 0.019987500 4.338055E-02  24.741 2.759167E-02  60.757 1.264493E-03 172.773 9.619784E-01 -28.320
         2.753260E-02  60.598 5.663544E-02  -7.471 9.629115E-01 -28.078 8.262120E-04 130.485
         1.252529E-03 171.672 9.652648E-01 -28.414 4.342042E-02  20.989 2.762920E-02  60.190
         9.660442E-01 -28.600 8.369133E-04 130.697 2.751868E-02  59.706 4.591656E-02  22.958
 0.029975000 5.279364E-02  19.352 3.940318E-02  47.550 1.777378E-03 145.369 9.554404E-01 -42.013
         3.933148E-02  47.604 3.671105E-02  -9.347 9.577851E-01 -41.765 7.441007E-04 136.632
         1.751164E-03 143.245 9.584093E-01 -42.077 5.350023E-02  13.120 3.941780E-02  46.306
         9.575923E-01 -42.330 7.423362E-04 133.941 3.934892E-02  46.433 5.596628E-02  14.271
 0.039962500 6.059968E-02  11.269 4.905304E-02  34.608 2.323297E-03 117.191 9.492754E-01 -55.661
         4.906615E-02  34.594 3.431321E-02  15.544 9.519293E-01 -55.371 1.174888E-03 136.972
         2.295646E-03 114.989 9.529339E-01 -55.758 6.189575E-02   3.980 4.901626E-02  33.024
         9.517830E-01 -55.968 1.161010E-03 136.920 4.896336E-02  33.055 6.299231E-02   3.407
 0.049950000 6.662585E-02   1.555 5.628981E-02  21.659 2.841726E-03  90.468 9.434645E-01 -69.209
         5.633547E-02  21.883 5.111281E-02  22.288 9.453543E-01 -68.928 1.940923E-03 116.840
         2.788556E-03  88.049 9.454238E-01 -69.373 6.795117E-02  -5.423 5.627455E-02  19.599
         9.449649E-01 -69.579 1.899390E-03 117.875 5.611407E-02  19.671 6.618402E-02  -7.747
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         6.093212E-02   8.964 6.989614E-02  11.224 9.395743E-01 -82.342 2.770354E-03  88.655
         3.227467E-03  61.858 9.384965E-01 -82.888 7.212381E-02 -15.124 6.077348E-02   6.385
         9.384112E-01 -83.188 2.774367E-03  89.391 6.085816E-02   6.319 6.634015E-02 -18.404
 0.069925000 7.160252E-02 -22.097 6.273439E-02  -3.632 3.720456E-03  37.930 9.326985E-01 -96.370
         6.272058E-02  -3.522 8.357295E-02  -6.331 9.355087E-01 -95.783 3.570472E-03  57.951
         3.599259E-03  36.141 9.323274E-01 -96.278 7.376438E-02 -24.634 6.278425E-02  -6.705
         9.336231E-01 -96.646 3.602008E-03  58.589 6.281382E-02  -6.657 6.448640E-02 -28.081
 0.079912500 7.081175E-02 -34.685 6.182219E-02 -16.100 4.040125E-03  12.437 9.270003E-01 -109.843
         6.178188E-02 -15.966 8.959131E-02 -26.534 9.309905E-01 -109.271 4.262746E-03  27.041
         3.903036E-03  11.300 9.269238E-01 -109.574 7.376363E-02 -34.289 6.182057E-02 -19.660
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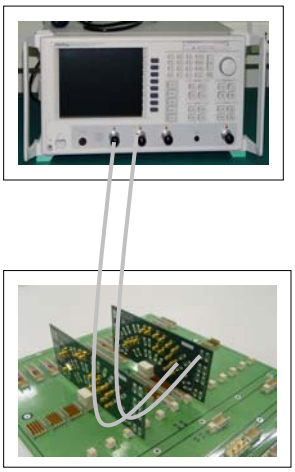
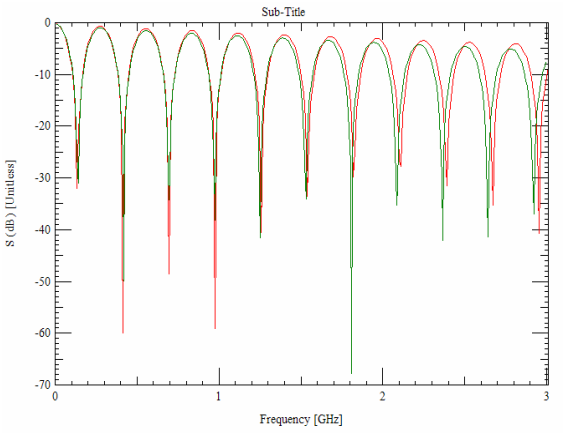
Lab Correlation for S-parameters

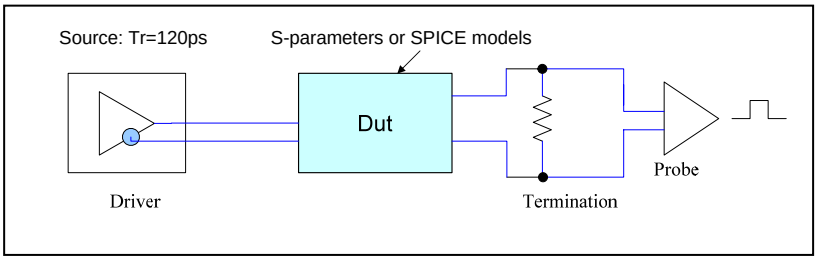




S21 data comparison between VNA measurement and Simulation

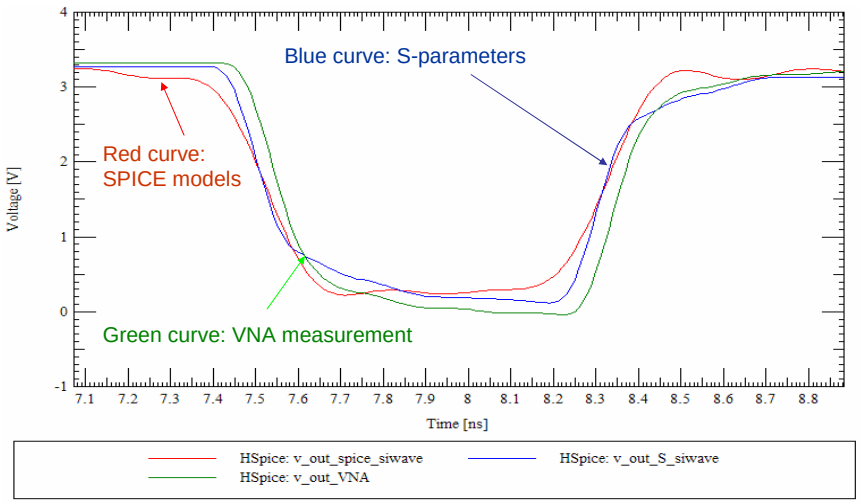
Simulation using S-parameters and SPICE models

1 Simulation using S-parameters extracted by EM field solver
2 Simulation using RLGC models
3 Correlate with laboratory measurements



Measurement versus Simulation

Lab Correlation for S-parameters and SPICE models

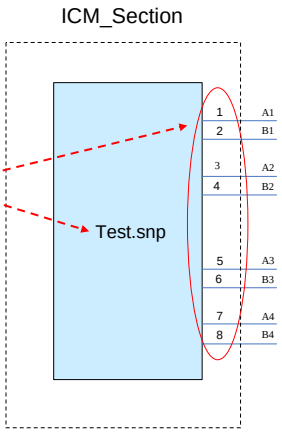


ICM&IBIS

- IBIS Interconnect Modeling Specification (ICM) permits model authors to describe passive interconnects in a tool-neutral, behavioral, human-readable way similar to IBIS.
- ICM supports S-parameter data.
- ICM supports RLGC frequency-dependent matricies.
- ICM does not include connections between IBIS [Model], IBIS [Pin] and ICM ports today.

Describing passive interconnects in ICM

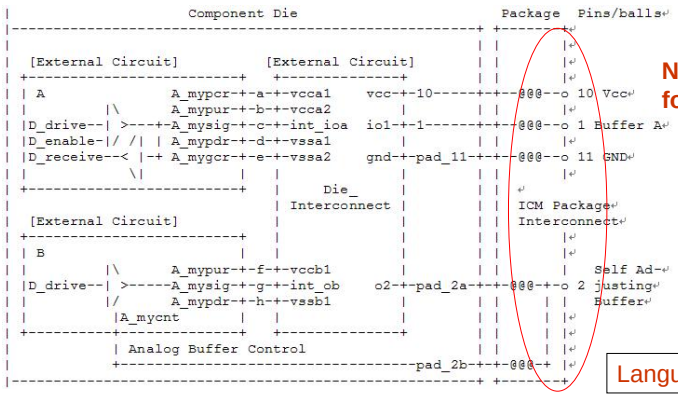
```
[Begin_ICM_Section]  S_para_example
[Derivation Method] Lumped
[ICM S-parameter]
File_name  test.snp
Port_assignment
|Port    Node
 1       A1
 2       B1
 3       A2
 4       B2
 5       A3
 6       B3
 7       A4
 8       B4
[End ICM Section] S_para_example
```



How do we link ICM to IBIS?

[External Circuit] in IBIS ver4.2

- Accepting SPICE, VHDL-AMS, Verilog-AMS, VHDL-A(MS) or Verilog-A(MS) as arguments.



New syntax required for arbitrary ports

Language→Touchstone ?

A proposal for IBIS package modeling using S-parameters

Linking ICM to IBIS

[Node Declarations]
|Die pads or pin names
A1, A2, A3, A4
pad1, pad2, pad3, pad4
[End Node Declarations]

IBIS

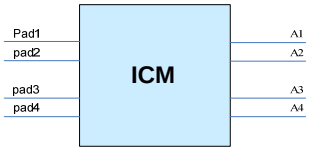
[ICM Pin Map] sample_int
Pin_order Row_ordered
Num_of_columns = 4
Num_of_rows = 1
Pin_list
|Pin Name
pad1 D1
pad2 D2
pad3 D3
pad4 D4

ICM

[ICM Pin Map] sample_ext
Pin_order Row_ordered
Num_of_columns = 4
Num_of_rows = 1
Pin_list
|Pin Name
A1 D1
A2 D2
A3 D3
A4 D3

ICM

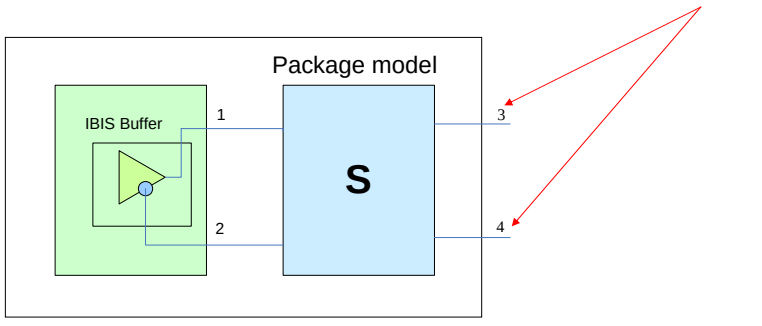
To Buffer



How do we use S-parameters for package modeling now?

Package modeling using S-parameters

- Many EDA tools support S-parameter simulation.
- Using subcircuits to describe S-parameter model.
- Replacing IBIS [Package Model] by S-parameter model.



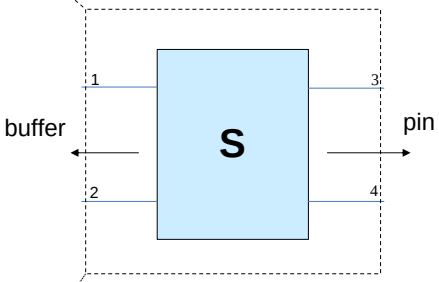
A solution for package modeling using S-parameters

```
("../../../Pkg_models/s_para_pkg.dml"
 (PackagedDevice
  (s_para_pkg
   (ESpice ".subckt s_para_pkg 1 2 3 4
Xs_para_pkg_4Port 1 3 2 4

.subckt s_para_pkg_4Port_Data 1 2 3 4
S1 1 2 3 4 algorithm=default
DATAPOINTS SPARAM
R=50.000000
DATAUNIT=HZ
FREQUENCY=0.000000e+000
.
. END SPARAM
.ends s_para_pkg_4Port_Data

.ends s_para_pkg_4Port" )
   (PinConnections
.
      (NumberOfPorts 4 )
   (SubType SPARAM ) ) )
 (LibraryVersion 136.2 ) )
```

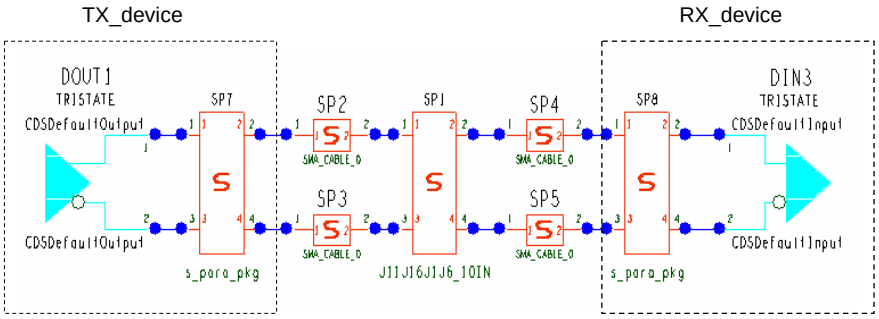
Package modeling using DML model



S-parameters can be added to Cadence DML file.

A solution for package modeling using S-parameters

- IBIS IO buffer modeling
- S-parameter package models of transceiver
- Connecting buffer models to package models in topology.



Summary

- S parameter features:
  - Behavioral modeling method compatible with IBIS style.
  - Much shorter simulation time compared with RLC connector models..
- Benefit IBIS ICM with S parameter:
  - "One model, one platform, one simulator" for both active and passive components.
  - Pave the way for behavioral, yet accurate enough IBIS simulation for very high speed circuit well beyond gigahertz.

References

- Michael Mirmak,"IBIS & ICM Interfacing: A New Proposal".
- IBIS Interconnect Modeling Specification (ICM) Version 1.0 (Sept. 12, 2003)
- I/O Buffer Information Specification (IBIS) Version 4.2 (June 2, 2006)


ZTE中兴
Global Connections Universal Solutions
Thank You
http://www.zte.com.cn

JEITA EDA -WG Activity and Study of Interconnect Model Part-3

Oct 27, 2006
IBIS SUMMIT in China
JEITA EDA-WG
Takeshi Watanabe (NEC Electronics)
takeshi.watanabe@necel.com
Hiroaki Ikeda (Japan Aviation Electronics)

JEITA ; Japan Electronics and Information Technology Industries Association

 1

Outlines

1. JEITA EDA-WG Activities
2. Short Term Direction of JEITA EDA WG
3. Study of Interconnect Model
4. Progress Report

 2

1. JEITA EDA-WG Activities

Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics

Cellular Phone, LCD /PDP TV,
Digital Camera/Video, DVD Recorder

(Digital , RF, and Analog circuits)

Auto Mobile Electronics ?

(Motor Drive, EMC)

< Applicability of IBIS V4.1 >

3

EMI, SI and PI for Digital Consumer Electronics

<Background>

EMI **High-speed Clock Frequency**

SI **DDR, PCI, PCI-Express**

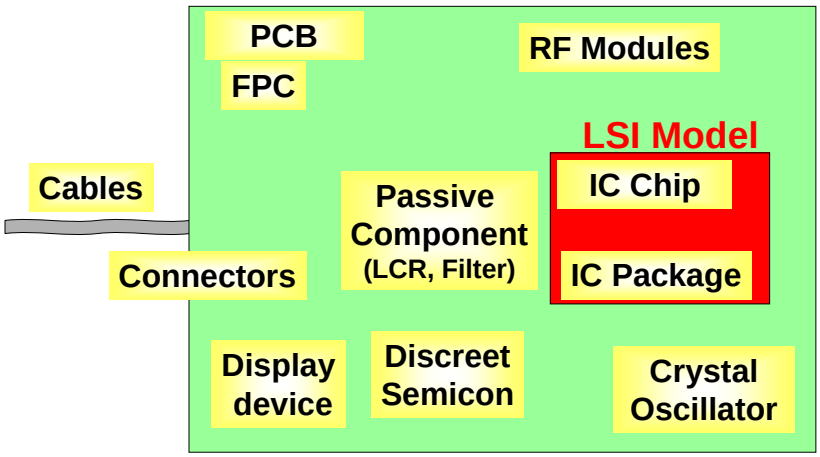
PI **High density and Large scale IC**

SiP and Module, PCB level

EMI, SI and PI Simulation Technology

4

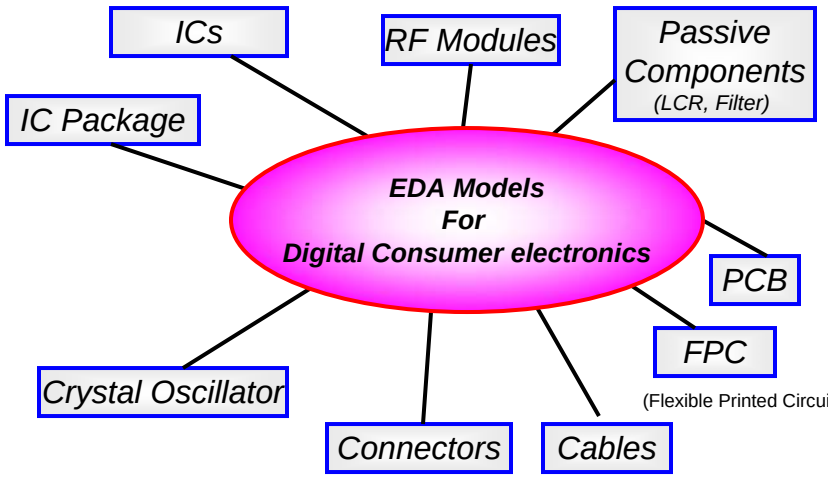
EDA Model for EMI, SI and PI Simulation



5

Focus of EDA Model for Simulation

9 components

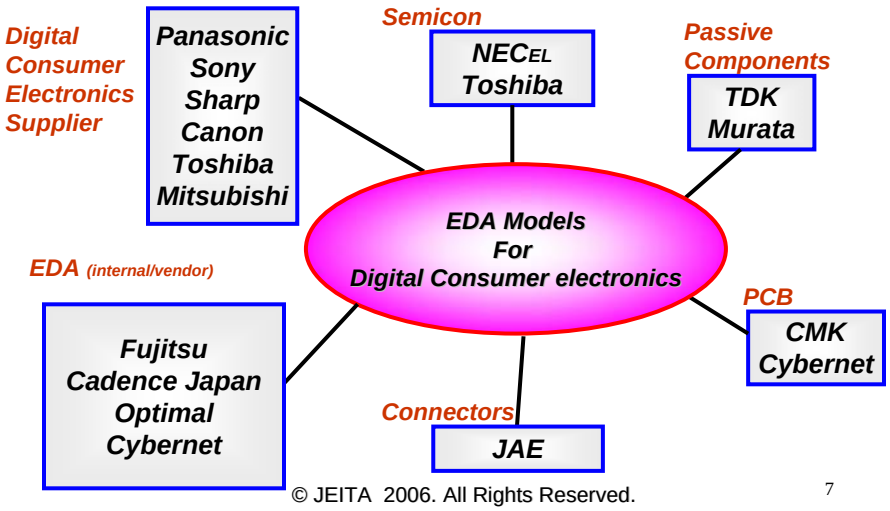


(Flexible Printed Circuit Board)

6

JEITA EDA-WG Member

16 Major Companies

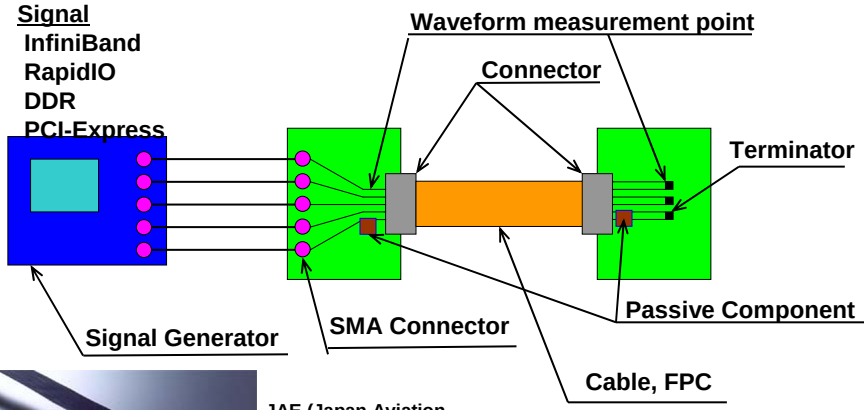


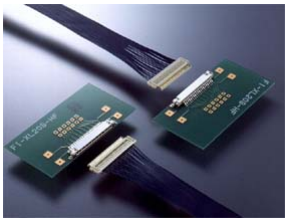
2. Short Term Direction of JEITA EDA WG

- Study of Interconnect Model
- EDA Models of Passive Components and Connector and other Components
- JEITA IBIS Model WEB
- Discussion about Case study of Simulation for Digital Consumer Electronics and JEITA-IBIS Joint meeting periodically

3. Study of Interconnect Model

SI Model (Connector, PCB, Cable)



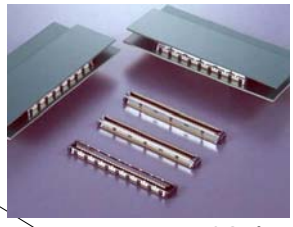


JAE (Japan Aviation Electronics Industry)
FI-X Series

Study of Interconnect Model for Signal Integrity

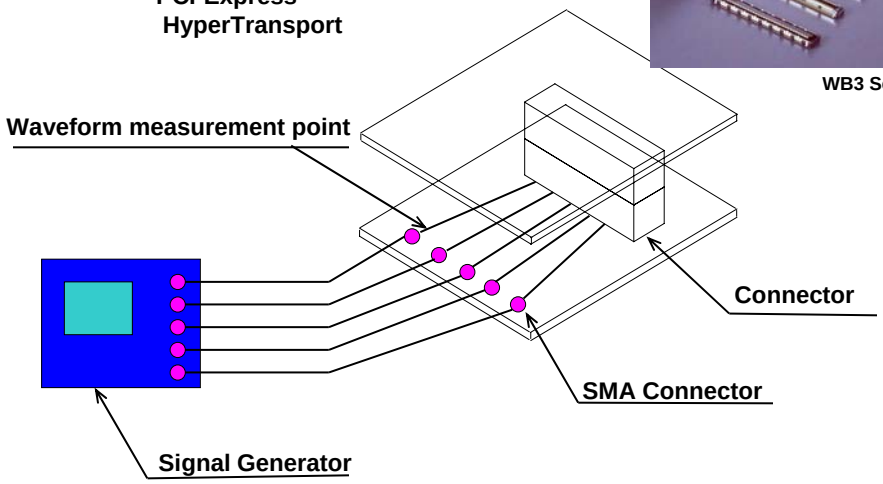
- ◆Target Application; DDR, PCI-Express etc.
- ◆EDA Model; Connectors,
  Passive Components,
  PCB (Via, Pattern),
  (LSI)
- ◆Simulation Tool; Cadence etc.

SI Model (Connector- Type B; stacked module, PCB, Cable)



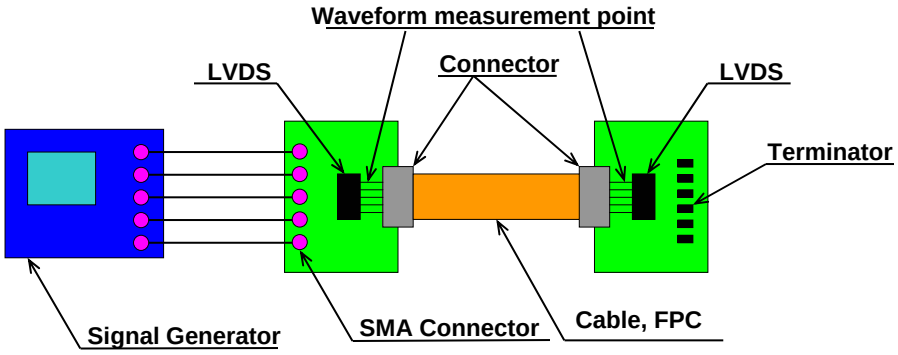
WB3 Series

Signal
PCI-Express
HyperTransport



11

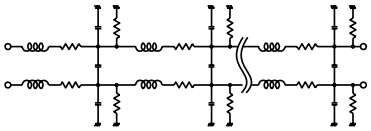
SI Model (Connector, PCB, Cable, LVDS)



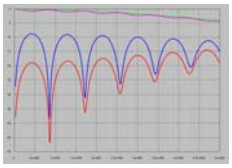
12

Simulation Model

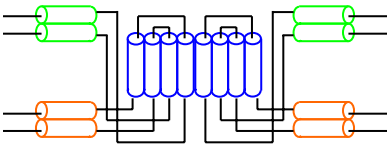
Equivalent circuit



Simulation



TML

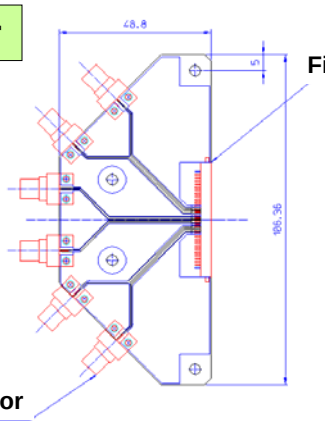


Measurement

13

Evaluation Board

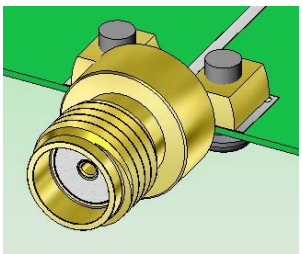
Connector



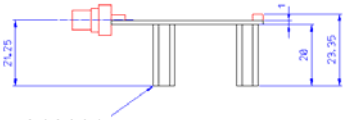
Fi-X Connector

SMA Connector

SMAR006D00



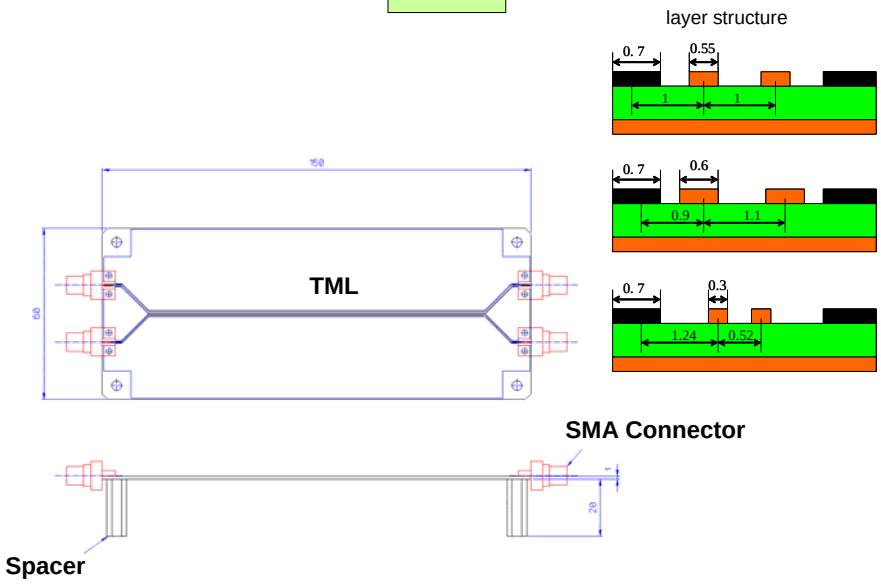
SMA Connector



spacer

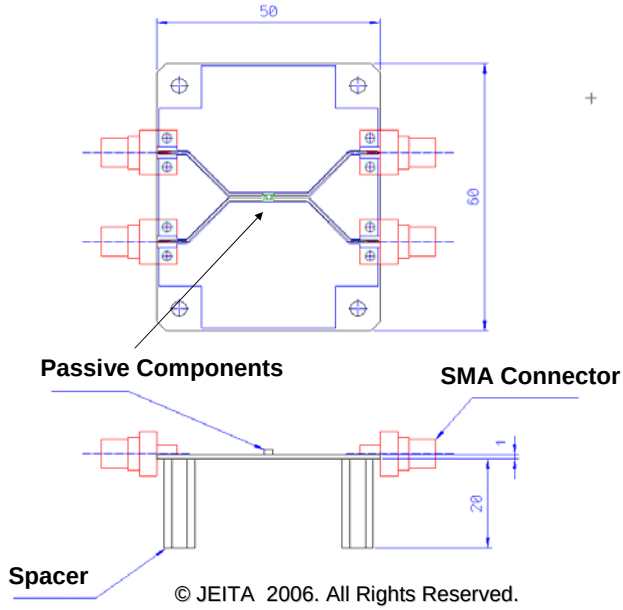
14

TML



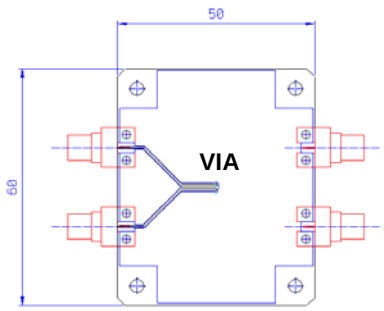
15

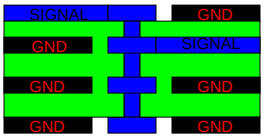
Passive Components

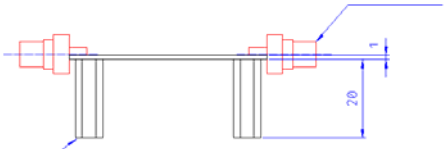


16

VIA



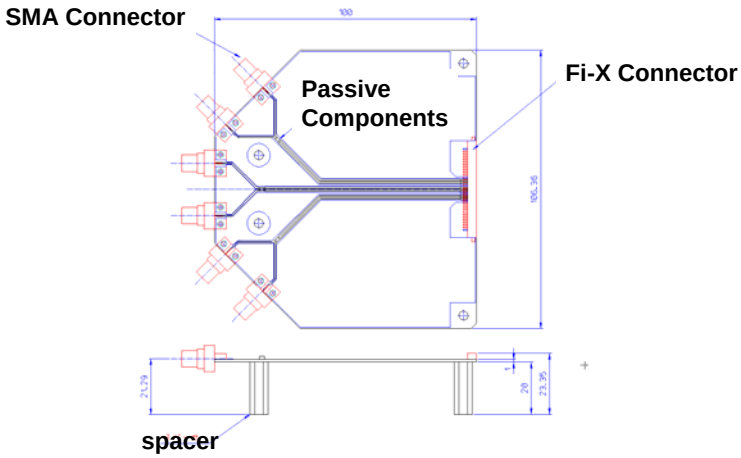




Spacer

17

All Component
(TML, Passive Components, VIA, Connector)



18

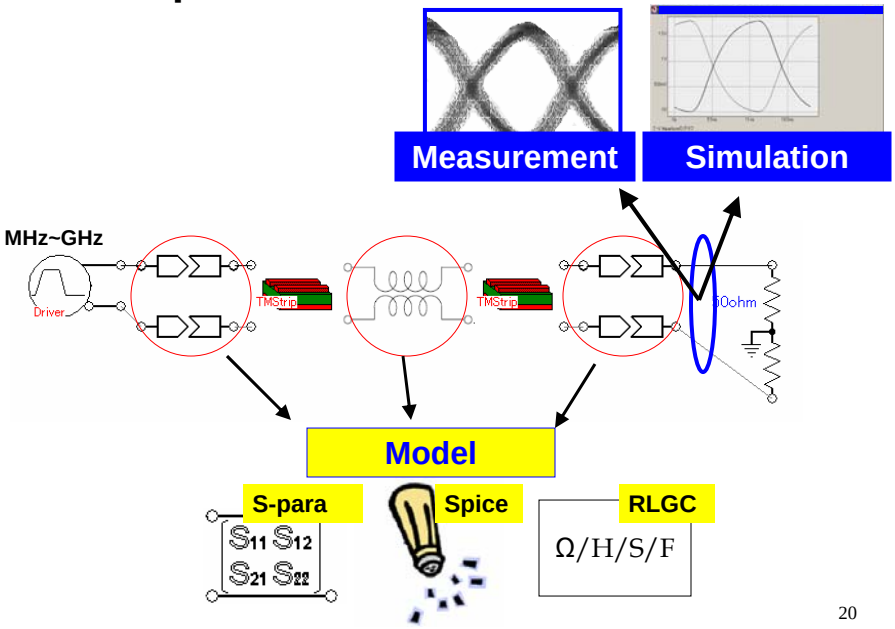
4. JEITA EDA-WG Progress Report

- **Study of Interconnect Model**

~October of 2006

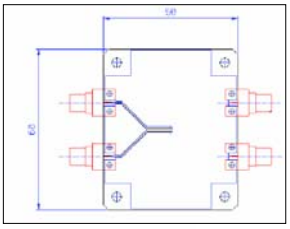
19

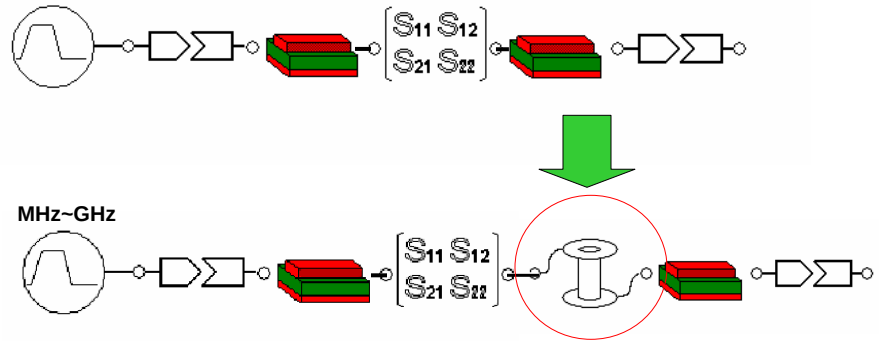
Compare Measurement with Simulation



20

Testing the VIA effect





And more

21

Study of Interconnect Model Outlines

0. Measurement and Simulation Environment
   - 0.1 Measurement equipment and simulation tools
1. Detail of Measurement and simulation
   - 1.1 Measurement
   - 1.2 Simulation
2. Comparison between Measurement and Simulation
   - 2.1 Eye-Diagram and Discrete Waveform
3. Simulation with Measured EDA models
   - 3.1 Eye-Diagram
4. Accuracy of EDA models
   - 4.1 TDR waveform for PCB trace
   - 4.2 S-parameters of device models (Filters,Via,Connector,Cable)
5. Conclusion

22

0.1. Measurement equipment and simulation tools

0.1.1 Equipment of Measurement

Time Domain Reflectmetory (TDR)

86100C +54754A(TDR module)

Vector Network Analyzer (VNA)

N5230A PNA-L

Signal Generator (GS) with Real Time Osi

81134A ,DSO81204B

0.1.2 Simulation tools and Venders

Company A, B, C,D

23

1. Detail of Measurement and simulation

24

1.1. Detail of Measurement

1.1.1 Measurement of Eye-diagram

Signal generator (GS) and real time oscilloscope (OSC) were used to compare measurement with simulation of Eye-Diagram.

GS was used to inject differential signal which were pseudo random bit sequence. (PRBS) PRBS pattern were 256bits.

OSC was used to record transient waveform.

DUT of three types were provided, which simulate PCBs of digital consumer electronics. One of them contains only filter and connector, the others contain filter, connector and also through hole via and slit.

25

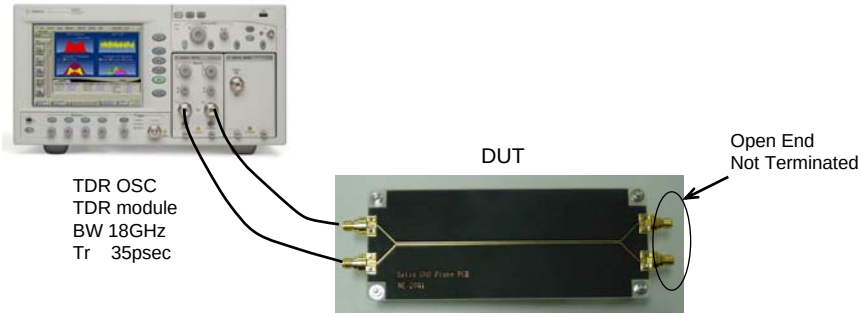
1.1. Detail of Measurement

1.1.2 Measurement of TDR

To verify characteristic Impedance of PCB, TDR was used.

The TDR injected differential step pulse and measured reflection waveform, then characteristic Impedance was calculated by the reflection waveform.

One side of DUT were left open in order to measure DUT of electric length which is propagation time to the end ports.



26

1.2. Detail of simulation
EDA models

1. EDA models were provided by component manufacturer.
2. PCB models were extracted from CAD data by simulation tools.
   PCB manufacturer does not provide EDA model.
   They provide only layer structure, wire width, space between wires and dielectric constant.
3. EDA models were S-parameters or Equivalent Circuits.

1.2. Detail of simulation
Simulation Items

1. Eye-Diagram

Only EDA model provided by the manufacturer.

To verify Whether the experiment agrees with the simulation

Measured S-parameters

To verify whether each simulator accept S-parameters.

2.TDR Waveform

Only wire of PCB

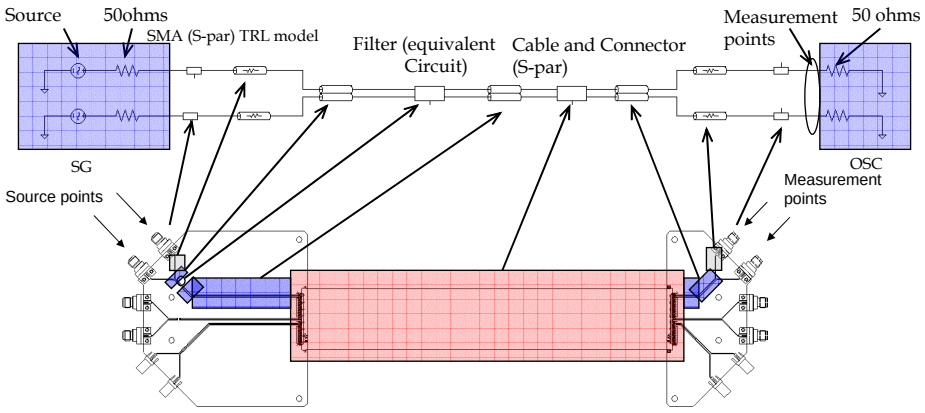
To verify whether EDA model of PCB which is extracted by each simulator is correct.

3.S-parameters

Each EDA models

To verify accuracy of each EDA models

1.2. Detail of simulation
#53 DUT and Simulation model



29

Gratitude to cooperation in measurement and simulation

Mr. Takeshi Watanabe	NEC Electronics
Mr. Shigeharu Shimada	CMK
Mr. Seiji Hayashi	CANON
Mr. Yogi Yamashita	Agilent Technologies
Mr. Yukio Masuko	Cadence Design Systems
Mr. Hirotsugu Ueno	Cadence Design Systems
Mr. Kazuhiko Kusunoki	CYBNET
Mr. Masatoshi Kobayashi	CYBNET
Mr. Nobuhiko Kawai	Murata Manufacturing
Mr. Jun-ichi Wakasa	TDK
Mr. Yasumasa Kondo	Toshiba
Mr. Testuo Iwaki	Sharpe

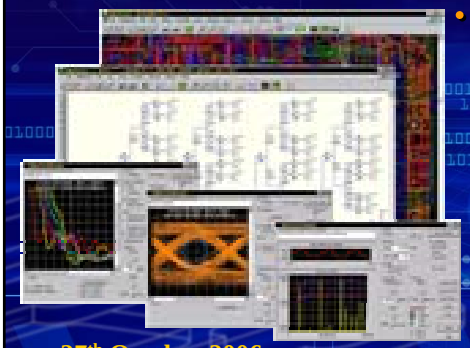
30

We hope to discuss case study of IBIS with you periodically

Thank you for all the help EIA/IBIS Committee!

31

IBIS4.2 and VHDL-AMS for SERDES and DDR2 Analysis



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Architect, High Speed Tools
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Gary Pratt
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Mentor Graphics®

27th October 2006

IBIS 4.2 Multi-lingual Extensions

- **Traditional IBIS lacks the ability to adequately model the behavior of devices used in state of the art communication channels:**
  - **Drivers with pre-compensation**
  - **Receivers with input slew rate sensitivity.**
  - **Phase locked loop clock and data recovery**
  - **Simple and adaptive equalization**
  - **Multi-level signaling**
- **Traditional IBIS also lacks the ability to adequately specify new measurements:**
  - **Differential overshoot**
  - **Eye masks**
- **IBIS 4.2 Multi-lingual Extensions can address both of these limitations**

SPICE as an IBIS 4.2 Multi-lingual option

- Good supply of transistor level models for older devices
  - May be encrypted and therefore not portable between tools
- Poor standardization
  - Lots of proprietary primitives
- Extremely slow simulation
  - Particularly when using transistor level models
- Missing a high level view
  - Needed to effectively model complex digital logic
  - Needed to make complex measurements.

AMS as an IBIS 4.2 Multi-lingual option

- VHDL-AMS and Verilog-AMS International standards
  - IEEE and Accellera
- Fast.
  - Models are compiled to machine code just like built in primitives.
  - Digital content is handled in event driven kernel
- Flexible
  - Can provide both behavior and measurement.
- Accurate
  - Uses the same analog non-linear solver as SPICE

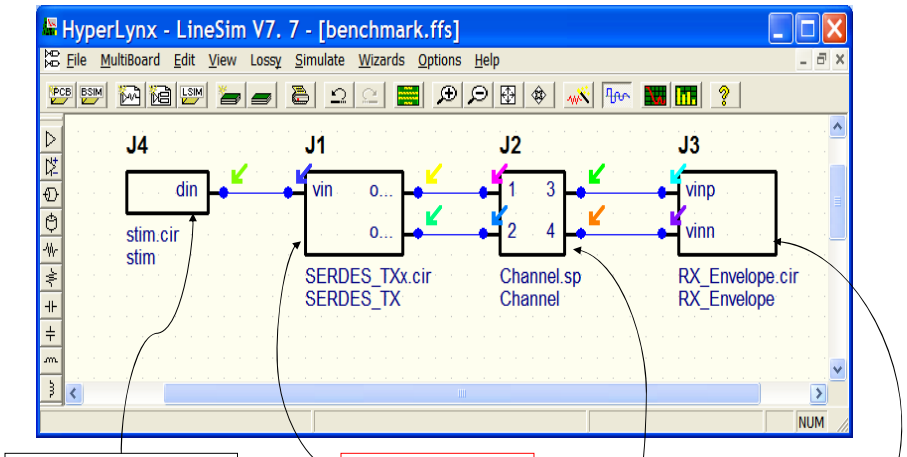
IBIS 4.2 Multi-lingual Case Studies

- The model maker and user can best decide whether it is best to create models using the IBIS 4.2 multi-lingual extensions utilizing SPICE or AMS
- The best solution for the SI Engineer may well be a tool that supports the mixing of both
- AMS provides some unique features so this presentation is going to provide two case studies that highlight these features.

AMS Case Study One
Full non-linear analysis of a SERDES channel

- Simulate to 10 million data bits
- Custom data pattern
- VHDL-AMS Driver with non-linear drive characteristics and pre-compensation
- Realistic S-Parameter model for packages, two connectors and backplane*
- VHDL-AMS receiver model with built in envelope recorder
- Simulations to be done on an average single processor notebook computer running Microsoft Windows
- Appropriate simulation time-step for accurate results

* As with previous examples used in presentations, this S-parameter model was provided by an independent third party and not optimized for simulation speed



The VHDL-AMS SERDES Transmitter Model

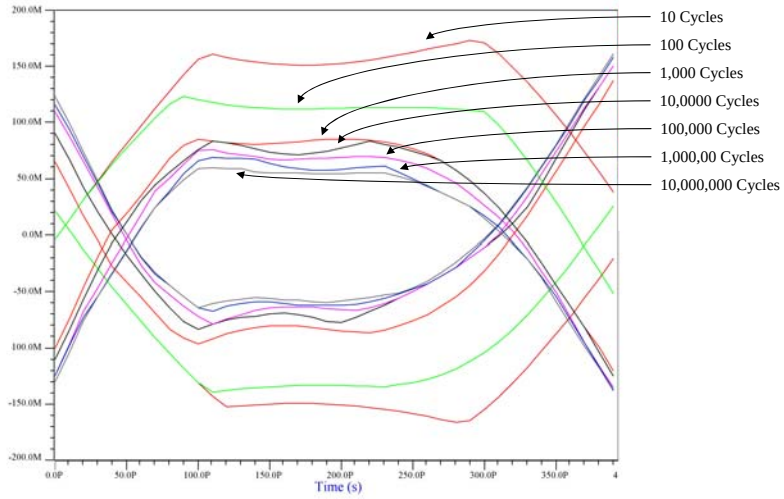
```
begin
  -- output the proper current based on the state of signal din,
  -- and values of constants Ipe and Imain
  if domain = quiescent_domain use  – if DC then
    itxp == Ipe/2.0; itxn == Ipe/2.0;     -- set both outputs to half
  elsif din='1' and din'delayed(bit) = '0' use
    itxp == Ipe; itxn == 0.0;             -- first pulse (txp positive)
  elsif din='1' and din'delayed(bit) = '1' use
    itxp == Imain; itxn == Ipe-Imain; -- normal pulse (txp positive)
  elsif din='0' and din'delayed(bit) = '1' use
    itxp == 0.0; itxn == Ipe;             -- first pulse (txn positive)
  elsif din='0' and din'delayed(bit) = '0' use
    itxp == Ipe-Imain; itxn == Imain; -- normal pulse (txn positive)
  end use;
  break on din, din'delayed(bit) ;   -- deal with the discontinuities

  -- P and N-side C_comp, R_term, Vdd
  i_r_term_p == (vtxp - Vdd)/R_term; i_c_comp_p == c_comp * vtxp'dot;
  i_r_term_n == (vtxn - Vdd)/R_term; i_c_comp_n == c_comp * vtxn'dot;

end architecture;
```

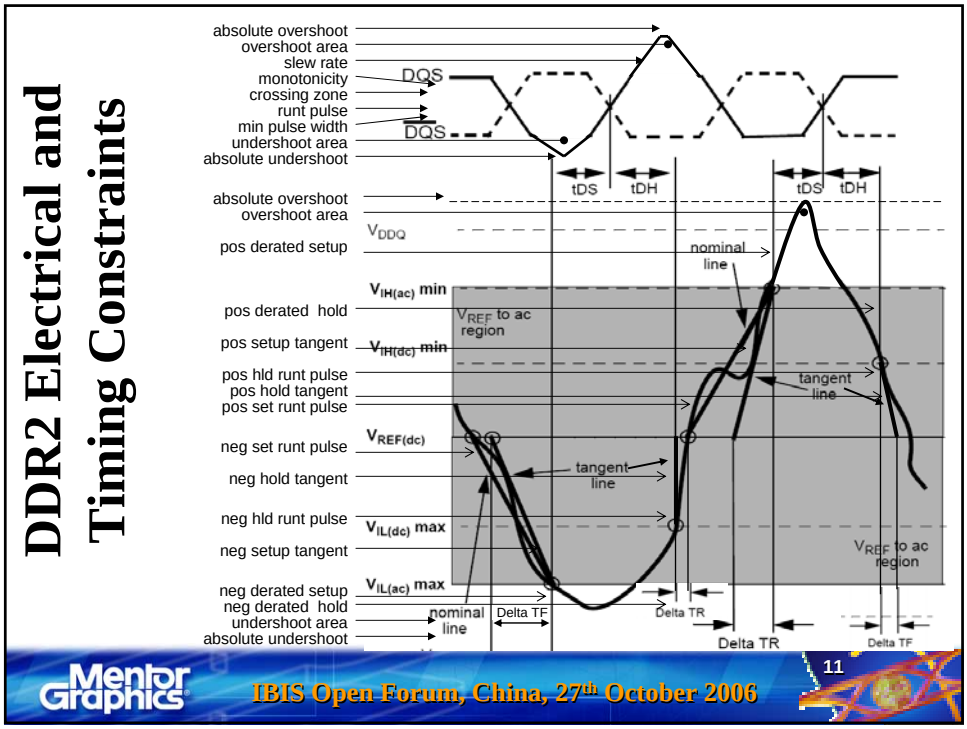
Results: Simulation to 10 Million Data Cycles

(All simulations completed overnight)



AMS Case Study Two
Automated DDR2 Measurements

- Implement all measurements specified in the DDR2 datasheet in a VHDL-AMS model
- Utilize standard IBIS 3.2 driver and receiver models


DDR2 Electrical and Timing Constraints
absolute overshoot
overshoot area
slew rate
monotonicity
crossing zone
runt pulse
min pulse width
undershoot area
absolute undershoot
DQS
DQS
tDS
tDH
tDS
tDH
absolute overshoot
overshoot area
pos derated setup
VDDQ
nominal line
VIH(ac) min
pos derated hold
VREF to ac region
pos setup tangent
VIH(dc) min
pos hld runt pulse
pos hold tangent
pos set runt pulse
tangent line
VREF(dc)
neg set runt pulse
neg hold tangent
tangent line
neg hld runt pulse
VIL(dc) max
neg setup tangent
VREF to ac region
neg derated setup
VIL(ac) max
neg derated hold
undershoot area
absolute undershoot
nominal line
Delta TF
Delta TR
Delta TR
Delta TF
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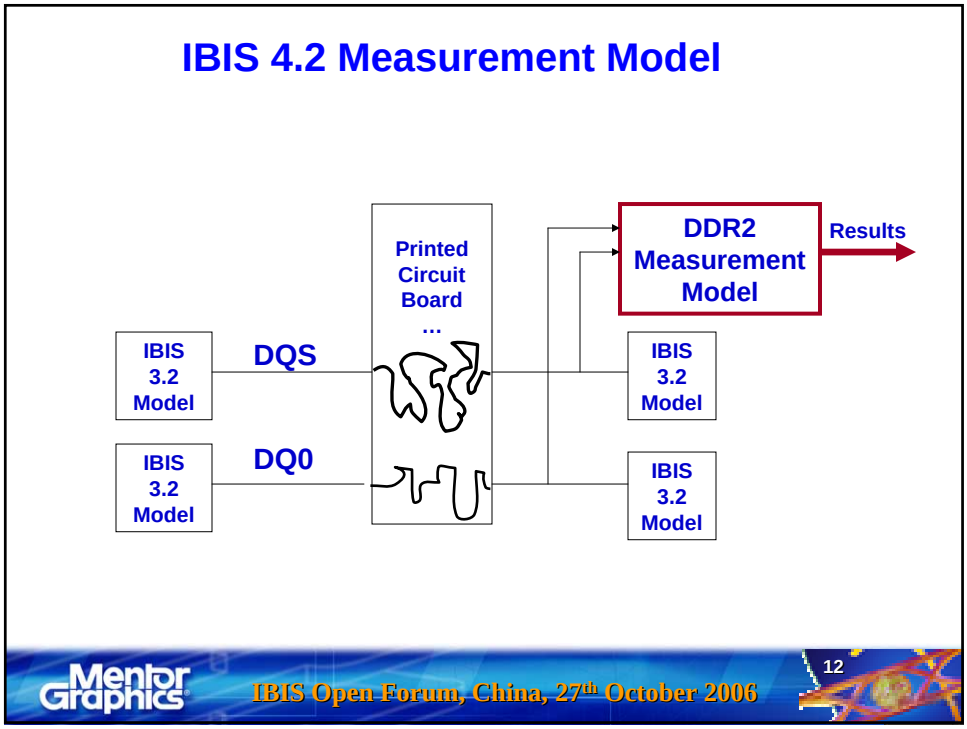
11


IBIS 4.2 Measurement Model
Printed Circuit Board ...
DDR2 Measurement Model
Results
IBIS 3.2 Model
DQS
IBIS 3.2 Model
IBIS 3.2 Model
DQ0
IBIS 3.2 Model
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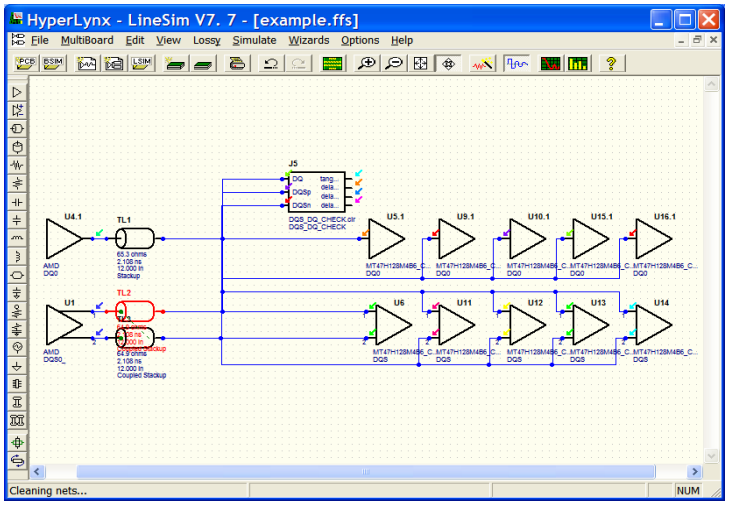
12

Pre-layout analysis using the IBIS 4.2 Measurement Model

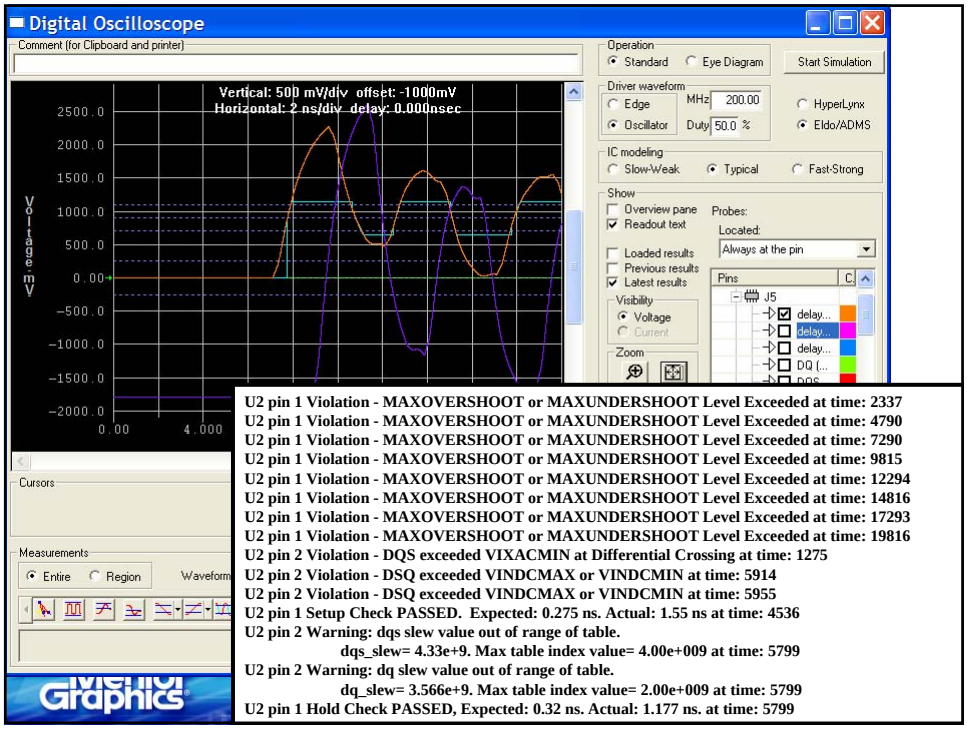


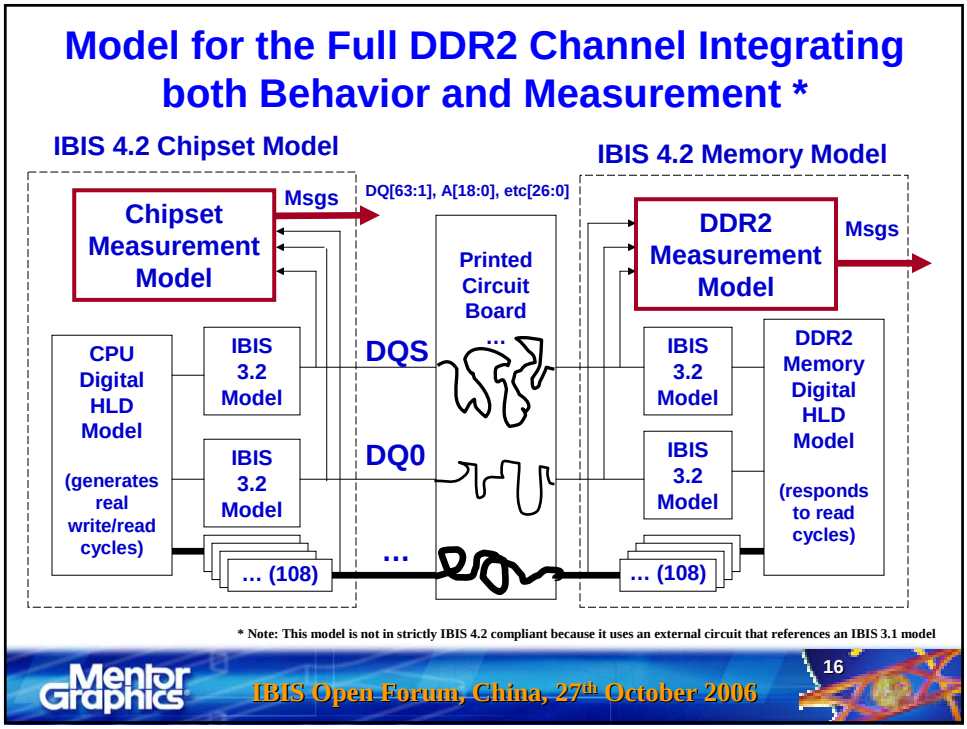
TANGENT MEASUREMENT

- Wait for vref crossing
- Store data points
- Wait for vix_ac cross
- Calculate the slope from each point to the vix_ac crossing point
- Return the maximum slope
- Wait for vix_dc crossing
- Calculate the slope from each subsequent point back to the vix_dc crossing
- Wait for vref crossing
- Return the max slope

```
begin
   ------------------------------------------------------------------------------
   -- measure the setup time tangent
   ------------------------------------------------------------------------------
   wait until VREFDC; -- wait for a crossing of correct direction
   max_slope:=0.0; data_point_cntr:=0;  setup_crossing <= 0.0*sec;
   while not vix_ac'event loop -- store all the data points until vix_ac crossing
      data_point_v(data_point_cntr) := Vin'reference;
      data_point_t(data_point_cntr) := now;
      wait on vix_ac, ASP; -- wait for next event
      data_point_cntr := data_point_cntr + 1;
   end loop;  -- go on to find the maximum slope
   setup_crossing <= now;
   for i in min_slope to data_point_cntr-1 loop
      slope := (crossing_point_v - data_point_v(i)) /
               (crossing_point_t - data_point_t(i));
      if slope > max_slope then max_slope:=slope; end if;
   end loop;
   setup_slope <= max_slope;
   ------------------------------------------------------------------------------
   -- measure the hold tangent
   ------------------------------------------------------------------------------
   wait until not vix_dc;  -- wait for opposite crossing of vix_dc
   max_slope := 0.0;
   crossing_point_v := Vin'reference; crossing_point_t:=now;
   -- calculate slope of each point until vix_dc, or max_points
   while not VREFDC'event loop
      wait on VREFDC, ASP ;
      slope := -(Vin'reference - crossing_point_v) /
               (now - crossing_point_t);
      if slope > max_slope then max_slope := slope; end if;
   end loop;
   hold_slope <= max_slope; -- in v/s
end process;
```

(error and exception handling removed for clarity)


Digital Oscilloscope
Comment (for Clipboard and printer)
Vertical: 500 mV/div offset: -1000mV
Horizontal: 2 ns/div delay: 0.000nsec
Voltage-mV
2500.0
2000.0
1500.0
1000.0
500.0
0.00
-500.0
-1000.0
-1500.0
-2000.0
0.00
4.000
Operation
Standard
Eye Diagram
Start Simulation
Driver waveform
Edge
Oscillator
MHz 200.00
Duty 50.0 %
HyperLynx
Eldo/ADMS
IC modeling
Slow-Weak
Typical
Fast-Strong
Show
Overview pane
Readout text
Probes:
Located:
Always at the pin
Loaded results
Previous results
Latest results
Visibility
Voltage
Current
Zoom
Pins
J5
delay...
DQ (...
Cursors
Measurements
Entire
Region
Waveform
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 2337
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 4790
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 7290
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 9815
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 12294
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 14816
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 17293
U2 pin 1 Violation - MAXOVERSHOOT or MAXUNDERSHOOT Level Exceeded at time: 19816
U2 pin 2 Violation - DQS exceeded VIXACMIN at Differential Crossing at time: 1275
U2 pin 2 Violation - DSQ exceeded VINDCMAX or VINDCMIN at time: 5914
U2 pin 2 Violation - DSQ exceeded VINDCMAX or VINDCMIN at time: 5955
U2 pin 1 Setup Check PASSED. Expected: 0.275 ns. Actual: 1.55 ns at time: 4536
U2 pin 2 Warning: dqs slew value out of range of table.
dqs_slew= 4.33e+9. Max table index value= 4.00e+009 at time: 5799
U2 pin 2 Warning: dq slew value out of range of table.
dq_slew= 3.566e+9. Max table index value= 2.00e+009 at time: 5799
U2 pin 1 Hold Check PASSED, Expected: 0.32 ns. Actual: 1.177 ns. at time: 5799


Model for the Full DDR2 Channel Integrating both Behavior and Measurement *
IBIS 4.2 Chipset Model
IBIS 4.2 Memory Model
Chipset Measurement Model
Msgs
DQ[63:1], A[18:0], etc[26:0]
DDR2 Measurement Model
Msgs
Printed Circuit Board
CPU Digital HLD Model
(generates real write/read cycles)
IBIS 3.2 Model
IBIS 3.2 Model
DQS
DQ0
...
IBIS 3.2 Model
IBIS 3.2 Model
DDR2 Memory Digital HLD Model
(responds to read cycles)
... (108)
... (108)
* Note: This model is not in strictly IBIS 4.2 compliant because it uses an external circuit that references an IBIS 3.1 model
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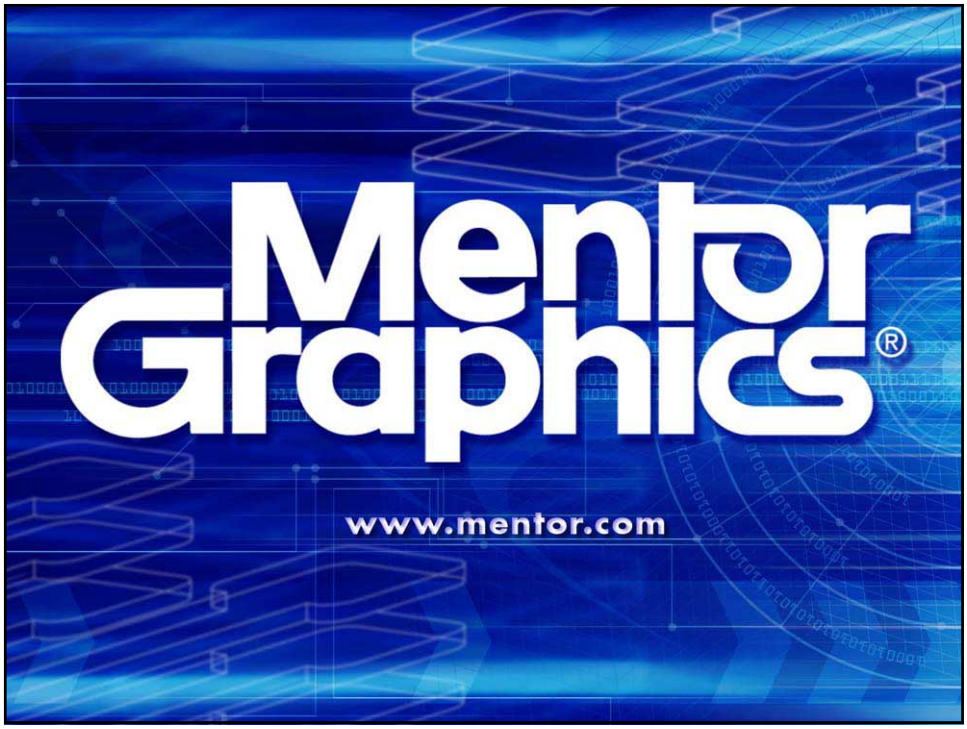
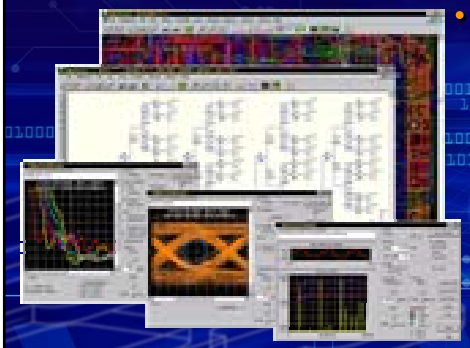
16

Special thanks to

Randy Wolff and his associates at Micron for assistance in developing DDR2 simulation and measurement models.



IBIS modeling of DDR2 in conjunction with linear channel analysis



Ian Dodd
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27th October 2006

Mentor Graphics®

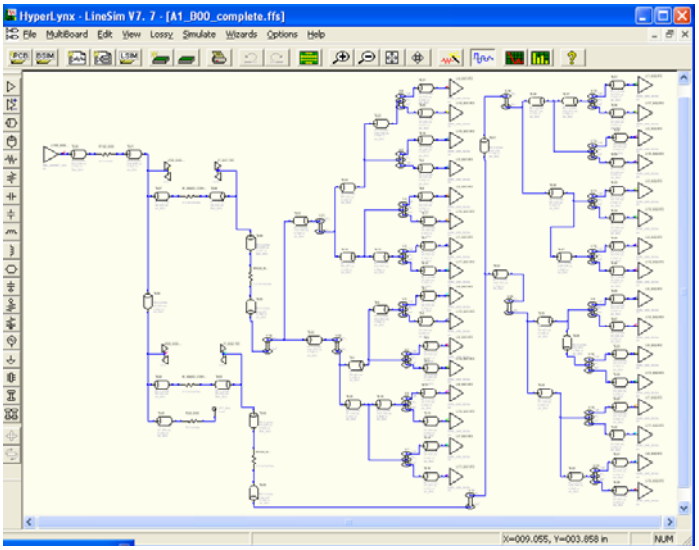
Overview

- High performance source synchronous buses, including DDR2 are known to be susceptible to resonances
  - Established solution is to add compensation capacitors
- It is difficult to demonstrate these resonances in traditional time domain SI simulators
  - Resonance only occurs with specific repeated bit sequences
- Linear channel analysis can identify the resonances but has limitations in its ability to determine if they are harmful
  - DDR2 drivers exhibit non-linearity's which may affect characteristics such as overshoot
- This paper describes the early results of our analysis of resonances in DDR2 buses using of both tradition circuit simulation using IBIS 4.2 models and linear channel analysis

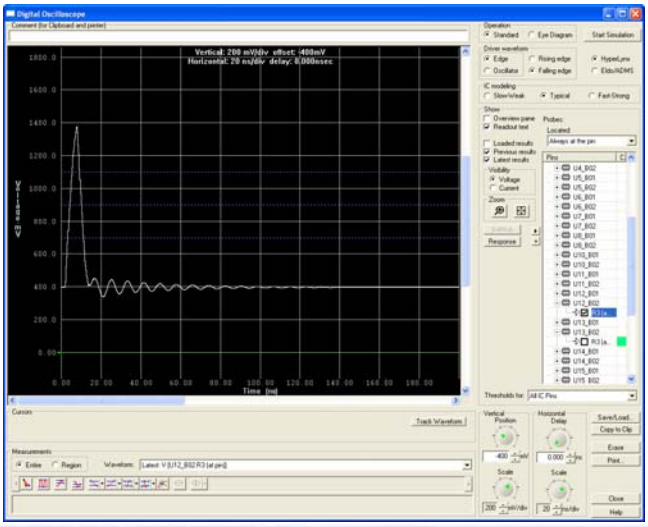
Analysis Steps

1. **Extract DDR2 Address net from layout**
   - Example has motherboard, 2 DDR2 modules and connectors
2. **Measure pulse response of the net using standard circuit simulation**
   - IBIS 4.2 driver and receiver models
   - Simulating multiple pulses allows the degree of non-linearity to be determined
3. **Linear channel analysis**
   - Determine worst case bit sequence
   - Create eye diagram with linearized drivers and receivers
4. **Standard circuit simulation using worst case bit sequence**
   - Create eye diagram without linearization

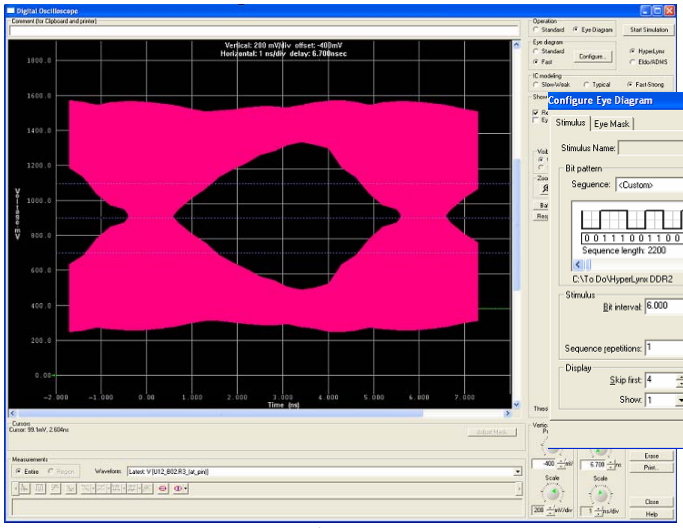
1. DDR2 address net extracted from layout



2. Full non-linear simulation to establish pulse response

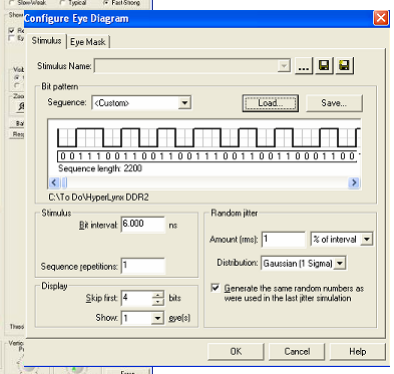


3. Linear Channel Analysis



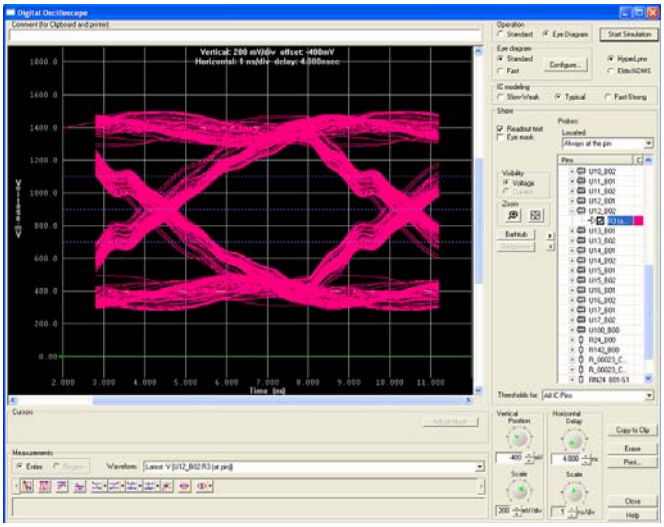
Eye Diagram

6% Non-linearity



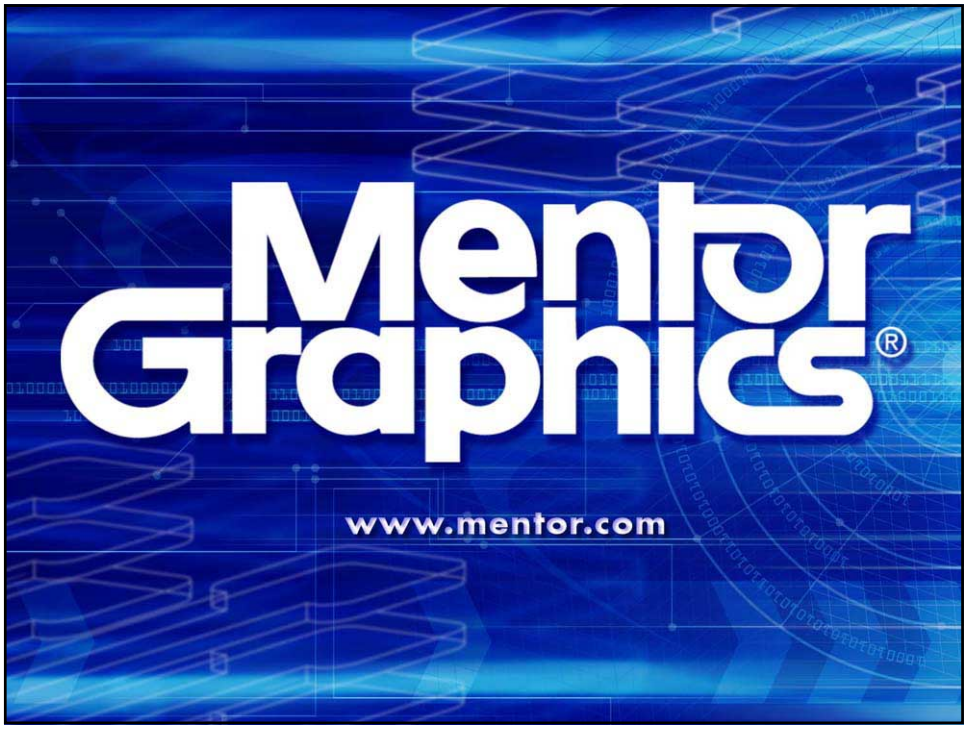
Worst Case Stimulus

4. Full Non-linear simulation using Worst Case Stimulus



Further Work

- This paper is based on the early results of this investigation into resonances on DDR2 buses
- We plan to further examine the detailed affects of channel layouts, connector characteristics and the optimization of compensation capacitors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ODT, Pre-Emphasis, and Speed

Bob Ross
Asian IBIS Summit
Shanghai, CHINA
October 27, 2006

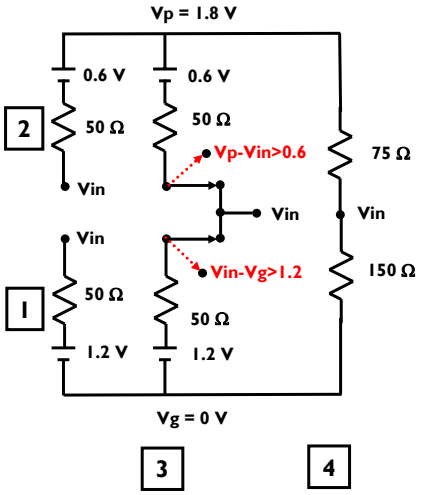
鲍伯若什
亚洲 IBIS 技术研讨会
中国上海
2006年10月27日

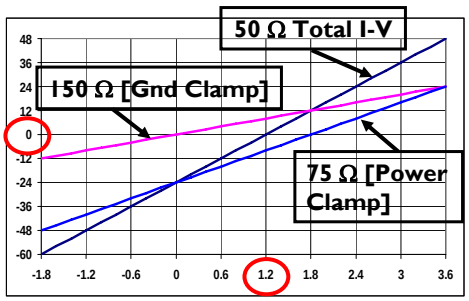
bob@teraspeed.com

On-Die Terminations (ODT)

- Model the device structure
- More details on "DEC" (Deviate, Extrapolate, Calculate) process:
  - http://www.eda.org/pub/ibis/summits/sep05/ross2.pdf

Four ODTs With Same Total I-V





1. [Gnd Clamp] (1.2 V, 50 Ω)
2. [Power Clamp] (0.6 V, 50 Ω)
3. "Clip and Extend" (both clamps clipped)
4. "DEC" (75 Ω, 150 Ω)

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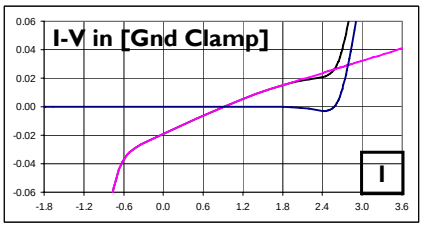
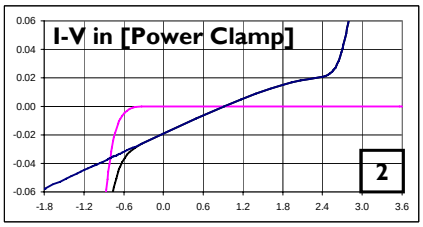
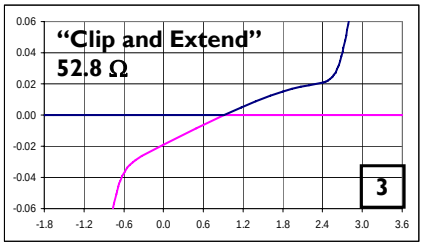
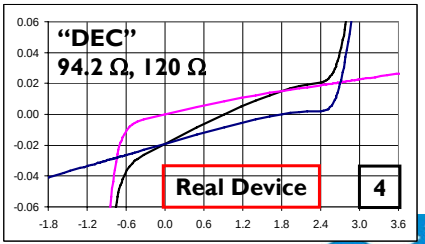
Real "50 Ω" ODT Choices









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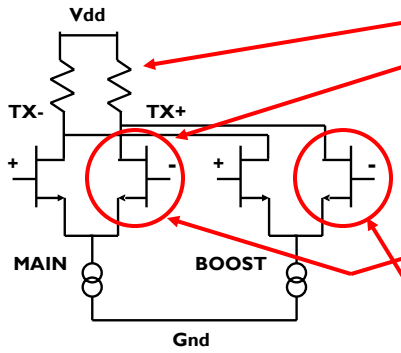
Pre-emphasis

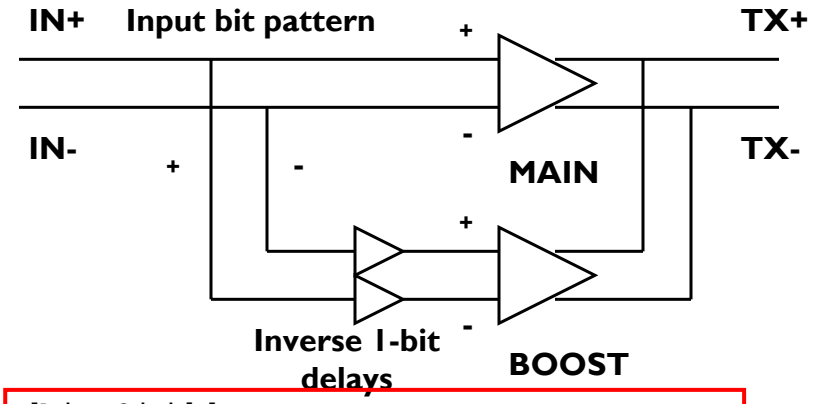
- Add [Driver Schedule] to match the device structure
- Examples:
  - 2-tap current mode logic (CML) 1-bit delay (de-emphasis) structure
  - Kickers for internal logic controlled boosts (and adjusted waveform delays)

CML Structure using IBIS Open_drain Models and Connected by [Diff Pin]



- Top-level
  - ODT [Power Clamp]
  - MAIN [Pulldown]
    - Extracted waveforms with ODT & 50 Ω
    - Pre-emphasis = 0
  - [Driver Schedule]
- MAIN [Pulldown]
  - Scaled waveforms
- BOOST [Pulldown]
  - Scaled waveforms

Actual SPICE Configuration with Differential Control




```
[Driver Schedule]
| Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly
MAIN         0           NA           0           NA
BOOST        NA          0.47059ns    NA          0.47059ns
```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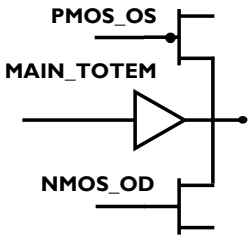
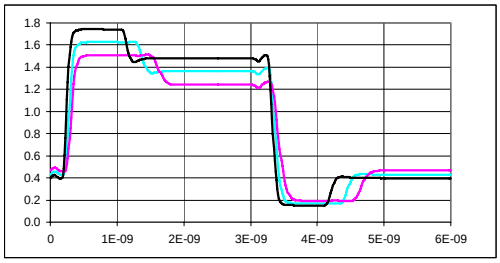
Different Typ-Min-Max Kicker Times (Internal Logic Control Kickers)

```
[Driver Schedule]
| Model_name     Rise_on_dly  Rise_off_dly  Fall_on_dly  Fall_off_dly
|
MAIN_TOTEM       0            NA            0            NA
PMOS_OS          0            1.05n         NA           NA
NMOS_OD          NA           NA            0            1.05n
```





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Speed – How Fast Is IBIS?

- World's fastest published IBIS model:

```
[IBIS Ver]      1.1
[File Name]     fastest.ibs
[File Rev]      0
[Date]          October 27, 2006
[Component]     Worlds_Fastest_Model
[Manufacturer]  Teraspeed Consulting Group
[Package]
R_pkg           0                   NA NA
L_pkg           0                   NA NA
C_pkg           0                   NA NA
[Pin]           signal_name         model_name
  1             Open_Drain          FAST_OD
[Model]         FAST_OD
Model_type      Open_drain
C_comp          0                   NA NA
[Voltage Range] 1E-100              NA NA
[Pulldown]
-1e-100         -20E-103            NA NA
2e-100          40E-103             NA NA
[Ramp]
dV/dt_r         0.3e-100/0.6E-109   NA NA
dV/dt_f         0.3e-100/0.6E-109   NA NA
[End]
```

1.0E-100 V, 50 Ω driver

1.0E-109 s ramps

Conclusion

- How fast is IBIS?
  - "As fast as you are smart"
- How accurate is IBIS?
  - Configure IBIS to match device structure for best accuracy
  - IBIS is as accurate as you are smart