Performance Evaluation Approach for 112G Serdes

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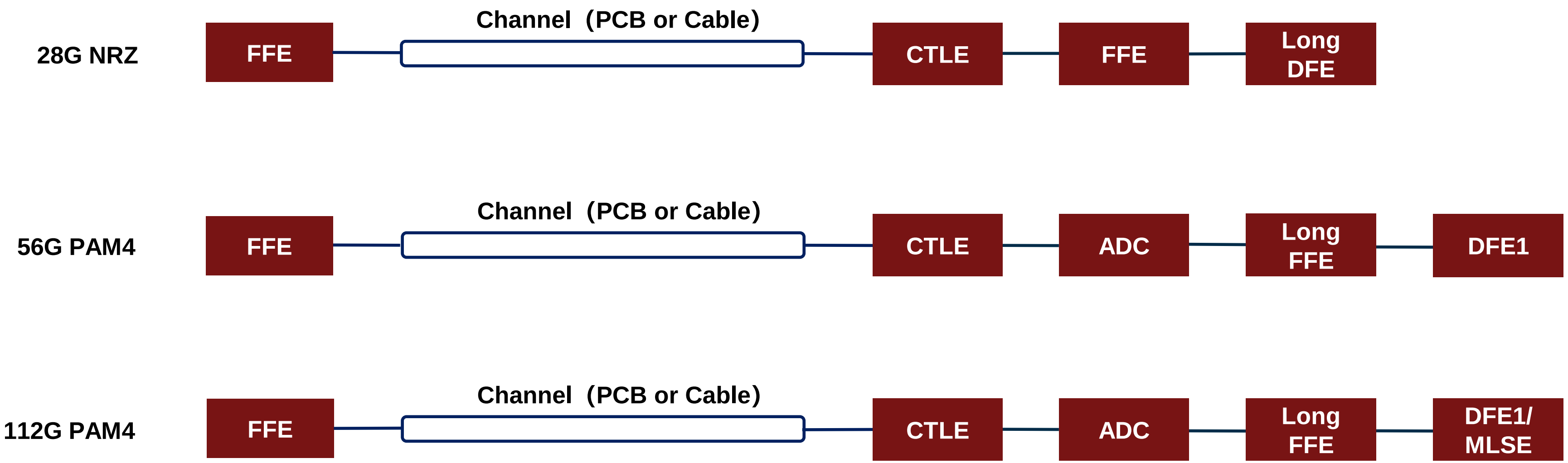
Outline

- High-Speed Serdes Channel Architecture and System Design
- 112G Serdes Signal Simulation and Test Verification
- 112G Serdes Error Distribution Histogram Simulation and Test Verification
- Conclusion

High-Speed Serdes Channel Architecture

- Typical architecture



112G Serdes System Design Technology

- Passive Design

Item	Approach
Base Material	ultra low loss (M7/M8 level)
Skew	reasonable stackup, board rotation(>3°)
Via	smaller size, backdrill error control, stub(<8mil)
Antipad	change the size and shape of antipad, reduce capacitive load
Ball Pitch	1.0mm or less
Crosstalk	control wiring layer and distance between wires, avoid cross-via-wiring, add isolation ground via
Connector	select high-performance high-bandwidth connector

- Active Design
  - ✓ Serdes architecture
  - ✓ FEC encoding: RS(544,514)/RS(544,514)-int

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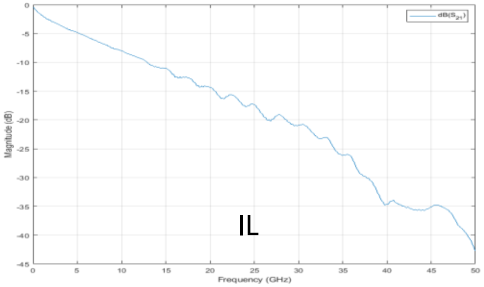
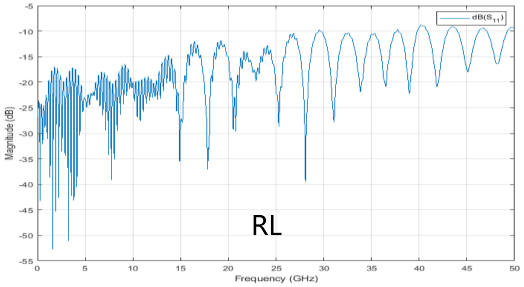
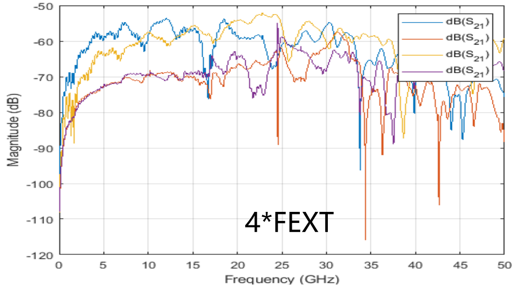
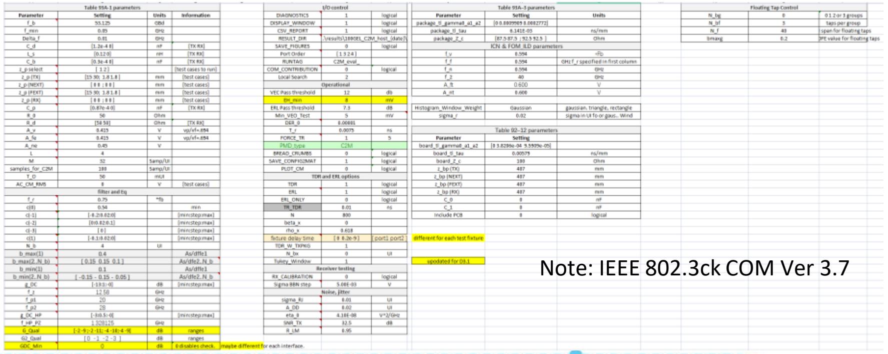
112G Serdes Passive Channel Simulation with XTALK (1)

Use Default COM Sheet Configuration









Note: IEEE 802.3ck COM Ver 3.7

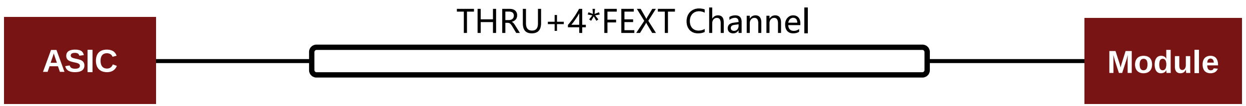
COM	ERL	ICN (mV)	FOM_{ILD} (dB)	VEC (dB)	VEO (mV)
1.914	8.268	1.072	0.239	17.035	3.84

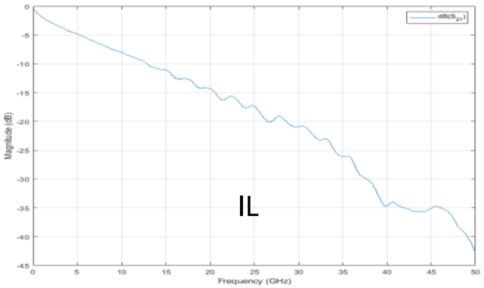
COM = channel operating margin
ERL = effective return loss
ICN = integrated crosstalk noise
FOM_{ILD} = RMS value of the insertion loss deviation
VEC = vertical eye closure

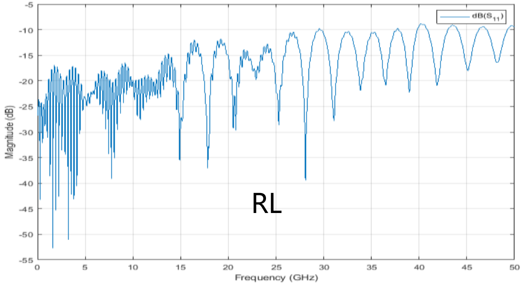
112G Serdes Passive Channel Simulation with XTALK (2)

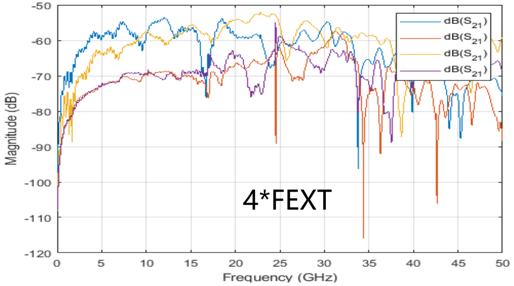
Use Modified COM Sheet Configuration

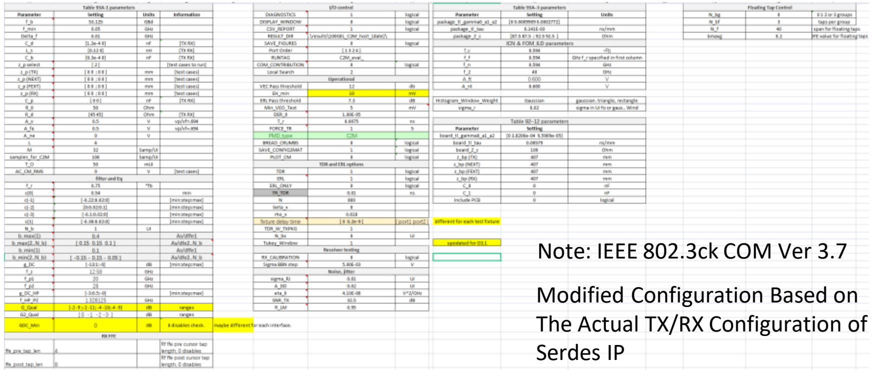
112G C2M











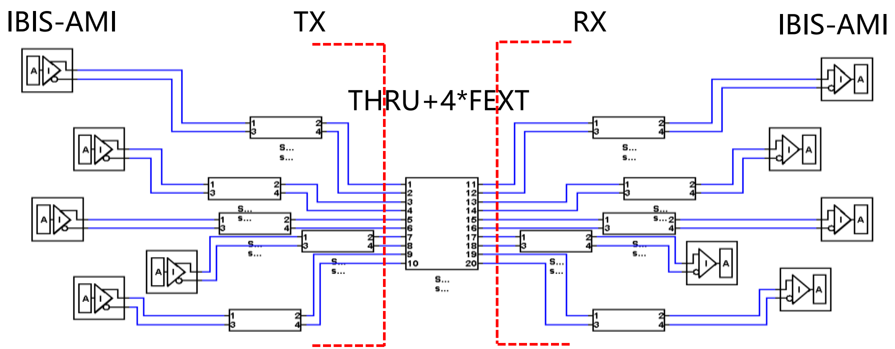
Note: IEEE 802.3ck COM Ver 3.7

Modified Configuration Based on The Actual TX/RX Configuration of Serdes IP

COM	ERL	ICN (mV)	FOM_{ILD} (dB)	VEC (dB)	VEO (mV)
3.233	8.388	1.072	0.239	10.149	14.28

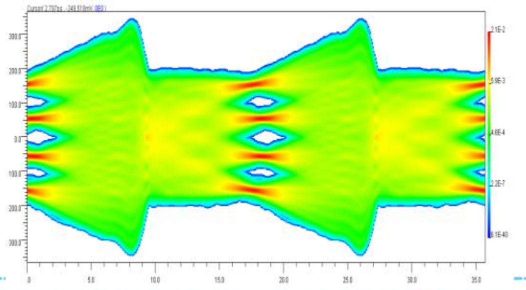
COM = channel operating margin
ERL = effective return loss
ICN = integrated crosstalk noise
FOM_{ILD} = RMS value of the insertion loss deviation
VEC = vertical eye closure

IBIS-AMI Simulation and Test Verification



Corner	BER	SNR (dB)	EH (mV)	EW (UI)
Typ	1.03E-15	24.9434	13.48 18.86 12.35	0.1056 0.1372 0.1046

Sim



Test

Typ	Simulation	Test
EH(mV)	13.48 18.86 12.35	22.45 23.00 20.80
EW(UI)	0.1056 0.1372 0.1046	0.2479 0.2677 0.2337

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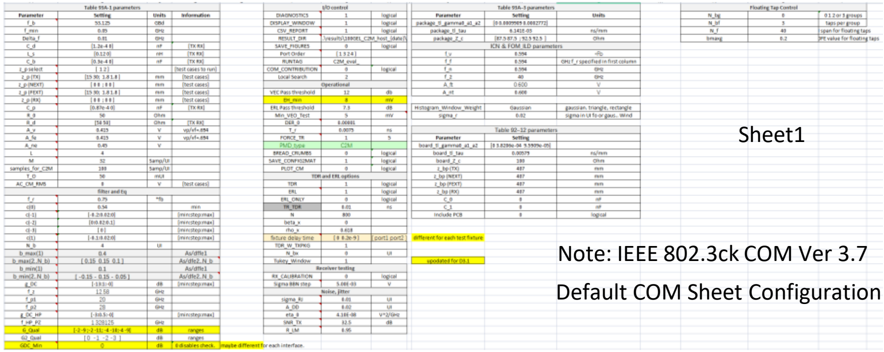
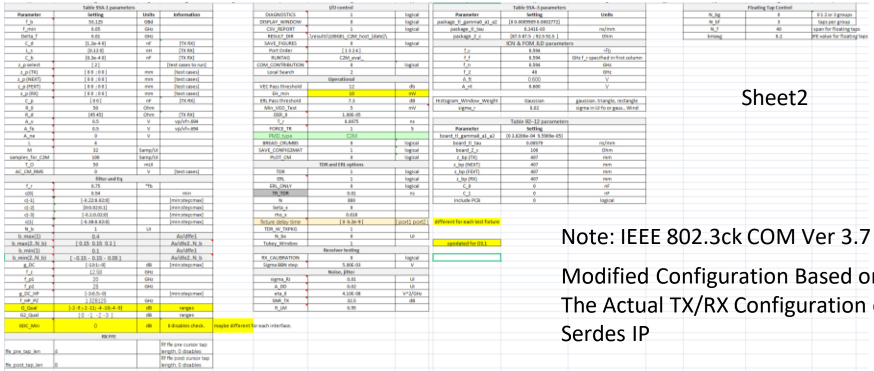
Analysis and Brief Summary



Sheet1

Note: IEEE 802.3ck COM Ver 3.7

Default COM Sheet Configuration



Sheet2

Note: IEEE 802.3ck COM Ver 3.7

Modified Configuration Based on The Actual TX/RX Configuration of Serdes IP

	VEO (mV)	VEC (dB)	COM
COM-Sheet1	3.84	17.035	1.914
COM-Sheet2	14.28	10.149	3.233
IBIS-AMI	12.35	-	-
Test	20.80	-	-

- Actual TX/RX configuration of Serdes IP recommended for COM simulation of C2M to achieve more accurate results
- Good consistency between IBIS-AMI simulation and test results, high confidence level of BER/SNR

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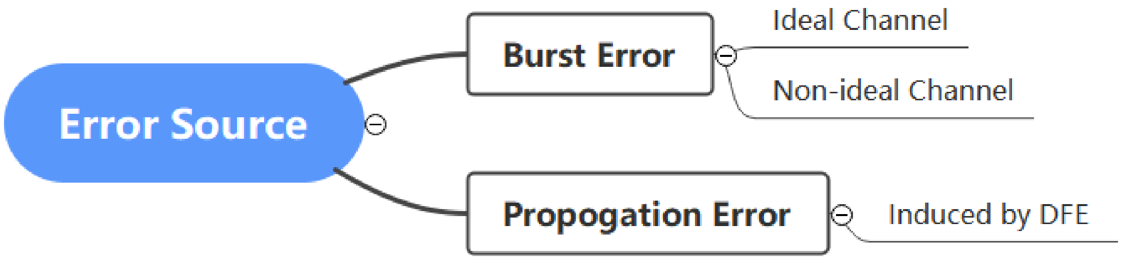
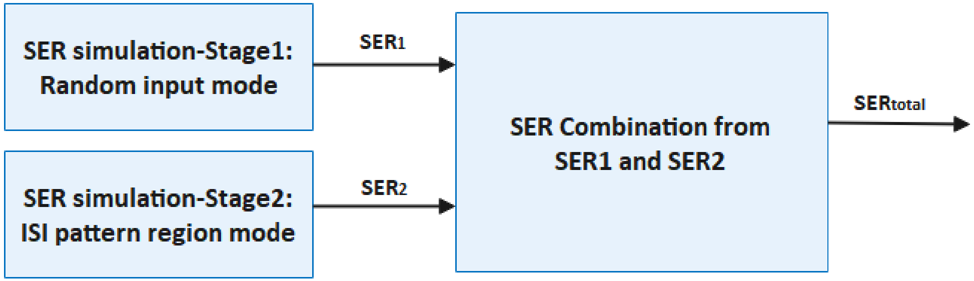
Error Distribution Simulation of 112G Serdes Channel

- During the serdes design and verification phase, the error distribution needs to be explored in order to ensure error correction by FEC at a specific BER
- Most of the 112G serdes IP vendors support the test of error distribution histogram through which it can be concluded that whether the errors can be corrected. But it takes a long time to do the test
- In order to get results more convenient and quickly, the error distribution histogram is obtained by simulation preferred



Random Error

- In general the influence of Gaussian noise is only considered for the ideal channel
- But the actual high-speed channel is non-ideal. Other factors, often ISI, need to be taken into account

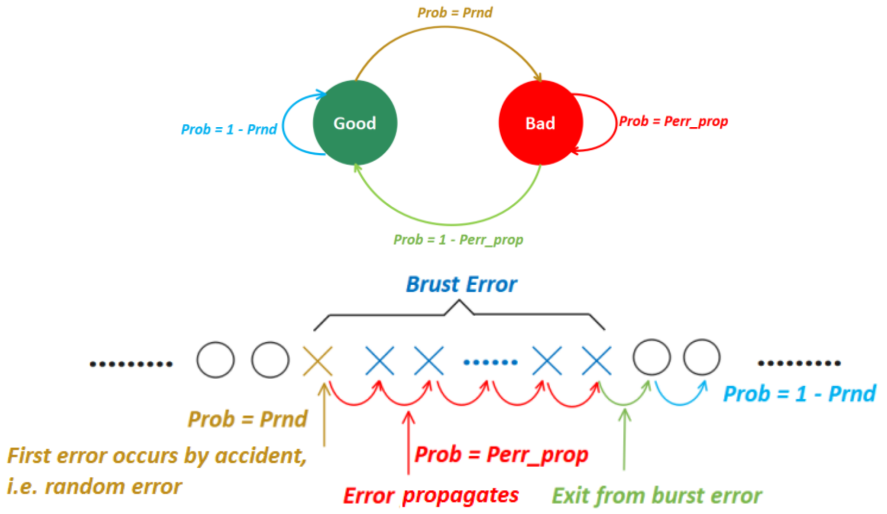


$$SER_{total}(i) = \sum_{j=0}^{i} SER_1(j) \bullet SER_2(i-j)$$

SER: symbol error rate

Propagation Error

- Many factors among which DFE is one of the most important affect propagation error. The research on DFE impact on the propagation error is widely conducted
- The propagation error induced by DFE can cause burst error. Burst error can be corrected within the capability of FEC
- The error distribution can be derived from the propagation length of burst error by simulation
- The propagation error model widely used in the industry is shown below

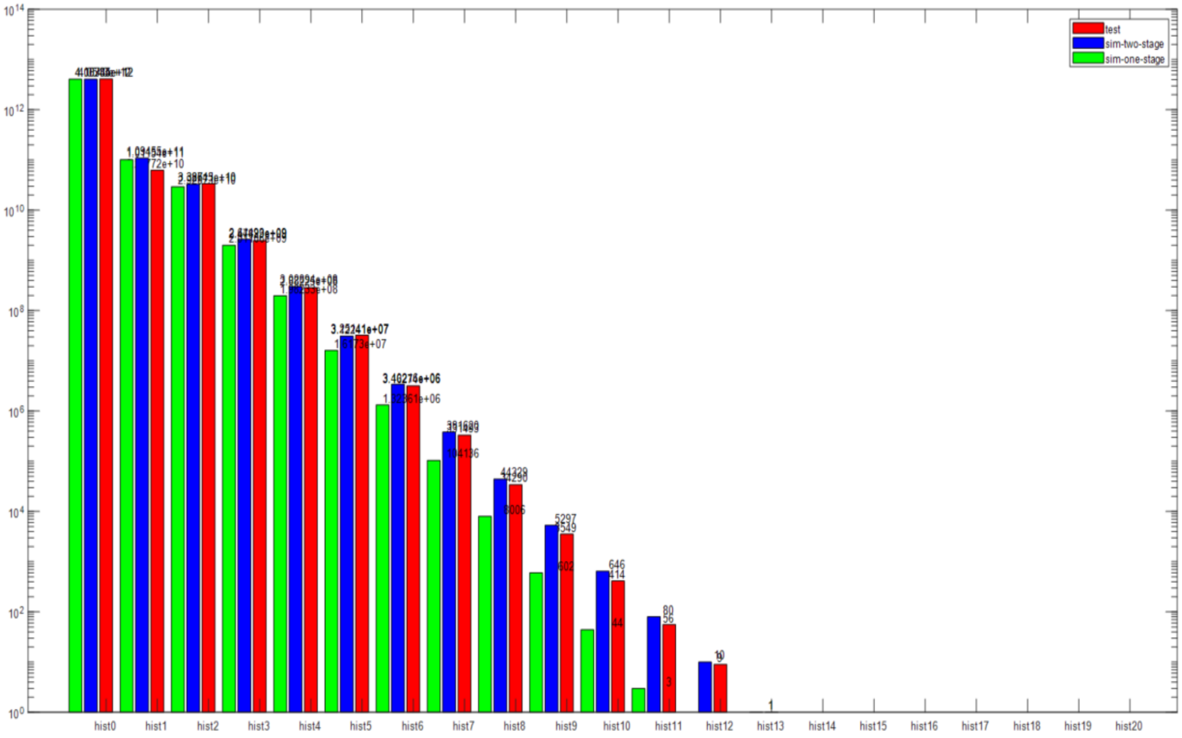


Note: This is a reference figure.

Research on Error Distribution Histogram by Simulation and Test

Input@Simulation	
Speed	106.25Gbps
Bits Flow Time	58h
Target BER	1E-5
Simulated FEC	RS(544,514)

Output @Simulation	
Blue Curve	Error Distribution Histogram (*Non-ideal channel+DFE propagation error*)
Green Curve	Error Distribution Histogram (*Ideal channel+DFE propagation error*)



Note：The red curve is the actual test result of error distribution histogram.

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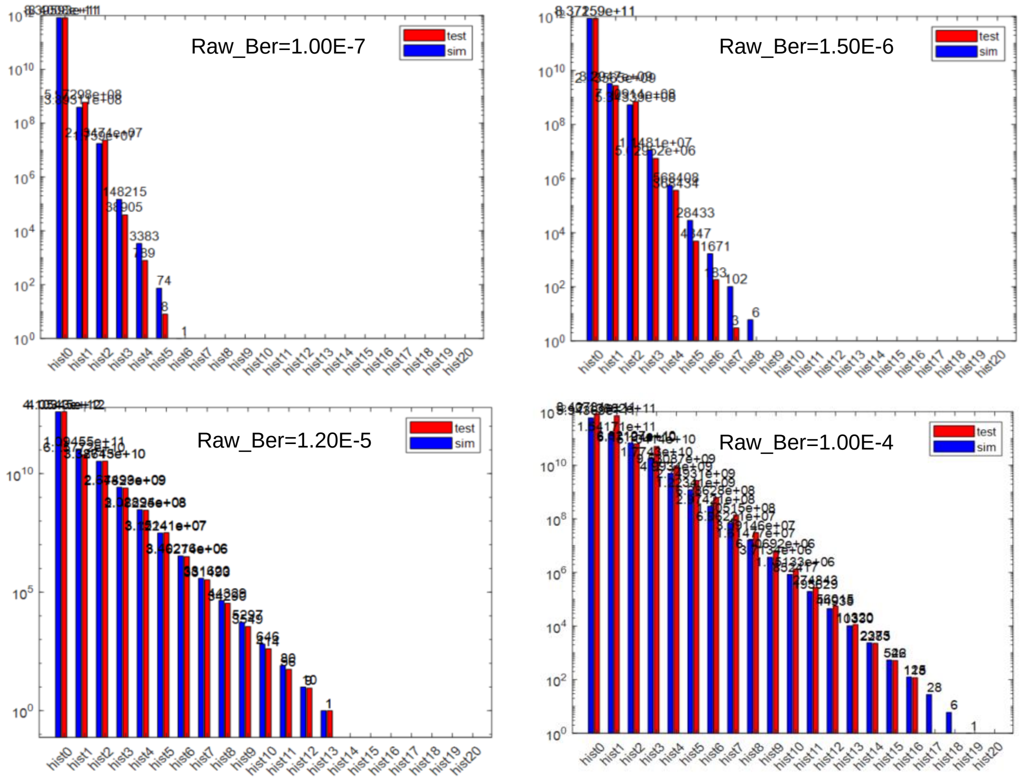
Comparison of Error Distribution Histogram under Different BER by Simulation and Test

Simulation Condition:

- ✓ Speed: 106.25Gbps
- ✓ Bits Flow Time: 12h
- ✓ Simulated FEC: RS(544,514)
- ✓ Correctable BIN Boundary: BIN<=15

Sim vs Test			
Channel	Raw_Ber	BIN@Sim	BIN@Test
36.8dB/0.45mV	1.00E-7	5	5
38.3dB/0.45mV	1.50E-6	8	7
41.3dB/0.45mV	1.20E-5	13	13
43.5dB/0.45mV	1.00E-4	>15	19



Conclusion: The simulation results consistent basically with the test results and meet the requirements.

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- Actual TX/RX configuration of Serdes IP recommended for COM Simulation of C2M to achieve more accurate results
- Good consistency between IBIS-AMI simulation and test results, high confidence level of BER/SNR
- Error distribution histogram is a useful means to evaluate the performance of 112G serdes channel

Thank you

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