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Concerns when applying Channel Simulation to DDR4 Interface

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Agenda

- Background
- About Channel Simulation
- Investigate LTI system of DDR4 Signal
- Summary

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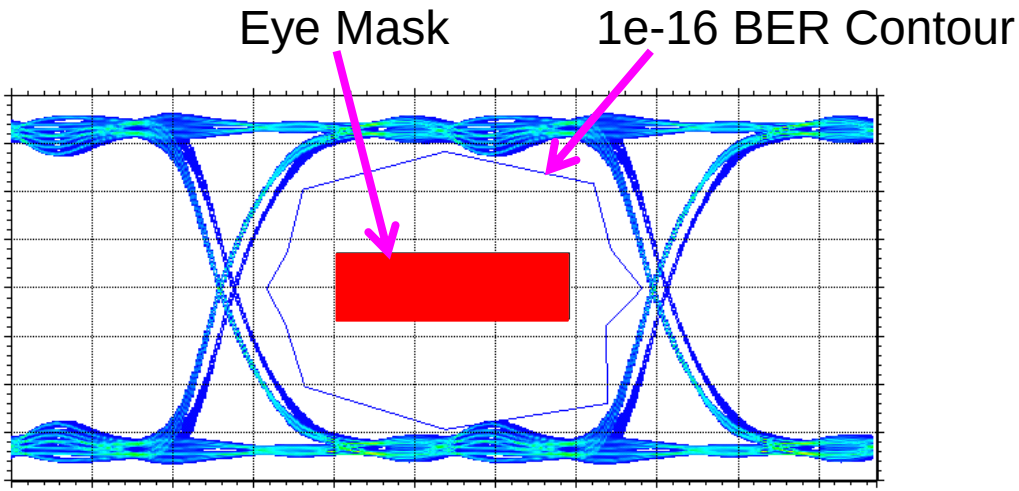
Background

Background

- DDR4 SDRAM JEDEC STANDARD: At BER=1e-16, the Eye Margin is necessary.
- Simulation of a great many bits is necessary to get a highly precise 1e-16 BER Contour.
- The conventional SPICE simulation takes time.
- Therefore high-speed Channel simulation using IBIS-AMI is necessary.
- In Channel simulation, the analog channel (include Driver, Receiver, Transmission line) must be LTI (Linear time-invariant) system.
- Therefore investigated whether DDR4 DQ Signal was LTI system this time.

DDR4-1866
Write direction
DQ Eye Diagram



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About Channel Simulation

Channel Simulation Method

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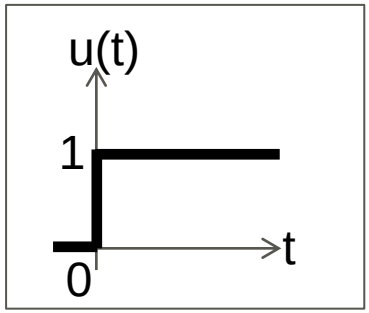
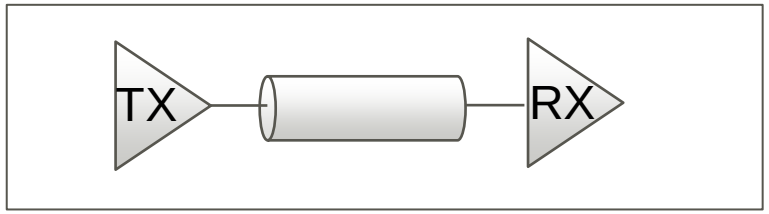
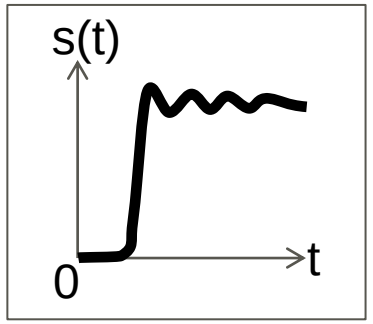
Ideal Unit Step Signal



Analog Channel
[Linear Time-Invariant (LTI) system]



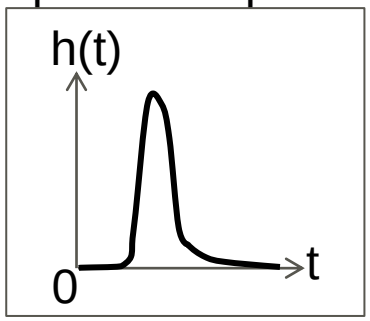
Step Response



Time Derivative

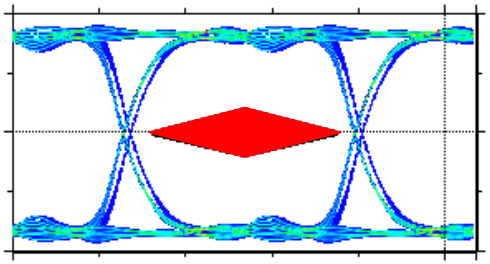
$$h(t) = \frac{ds(t)}{dt}$$

Impulse Response

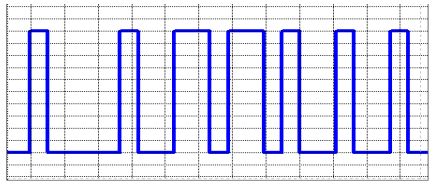


Convolution

Eye Diagram



TX Input Bit Stream



Linear Time-Invariant (LTI)

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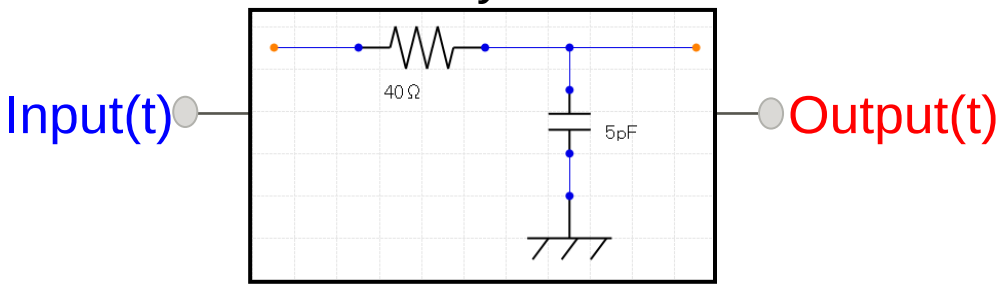
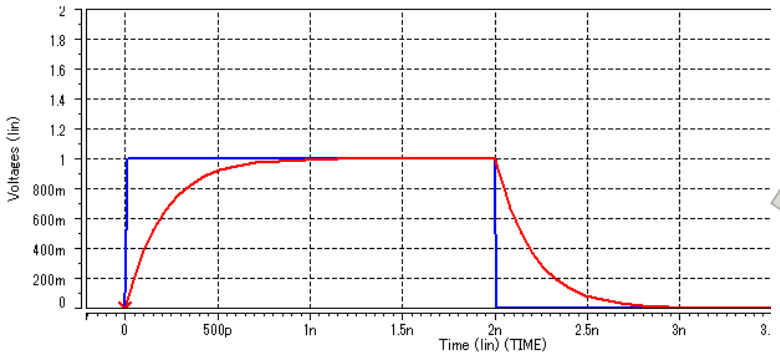
LTI System

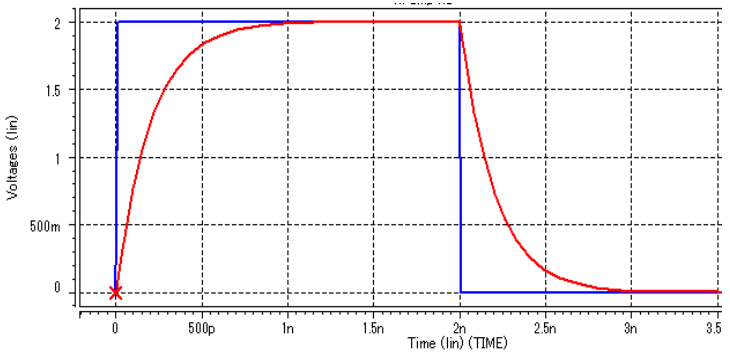


Input(t)⇒Output(t)



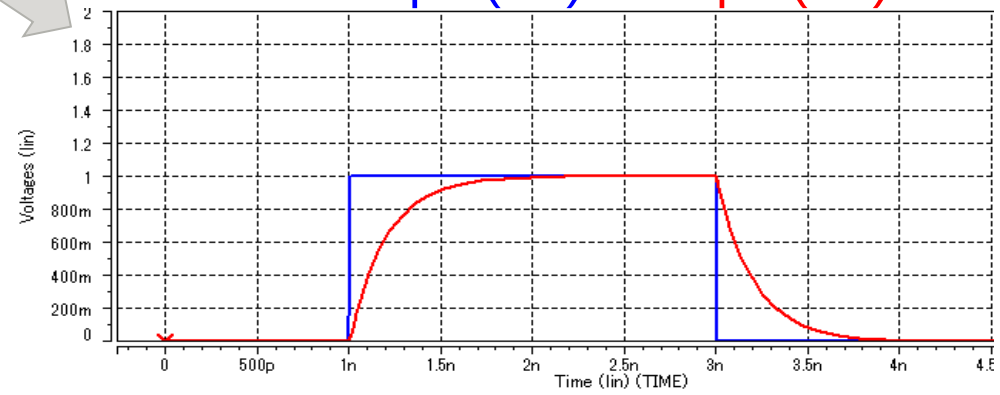
Linear

2Input(t)⇒2Output(t)



Time-Invariant

Input(t-T)⇒Output(t-T)



Linear Time-Invariant (LTI)

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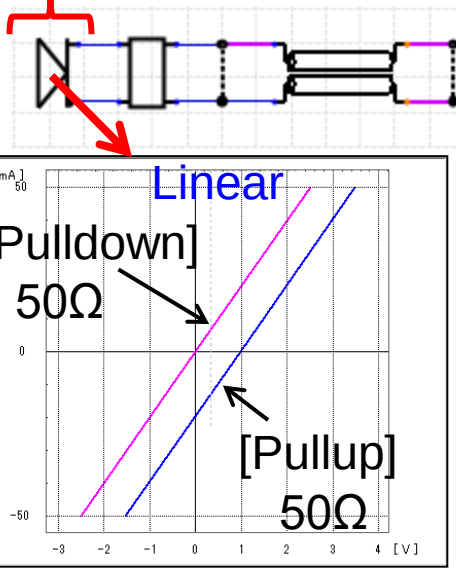
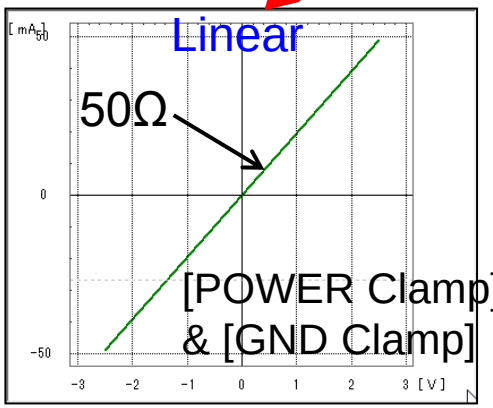
Transmitter
IBIS-AMI

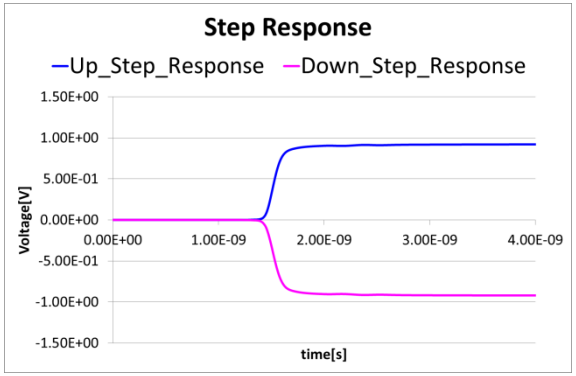
SERDES topology using IBIS-AMI

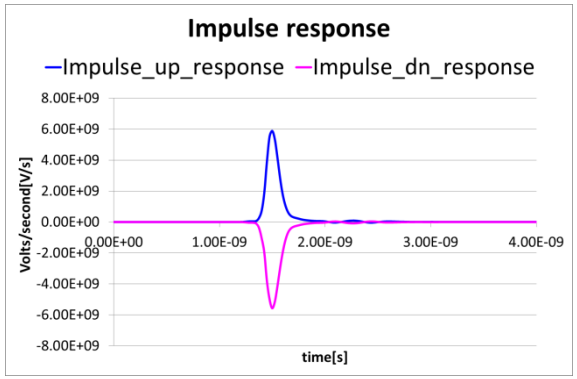
Receiver
IBIS-AMI

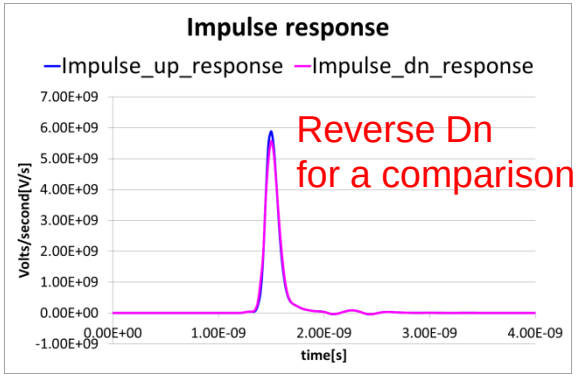


- Up Impulse response matches Down Impulse response.
- Therefore the analog channel characteristic is able to show by one Impulse response.
- And it is the LTI system.



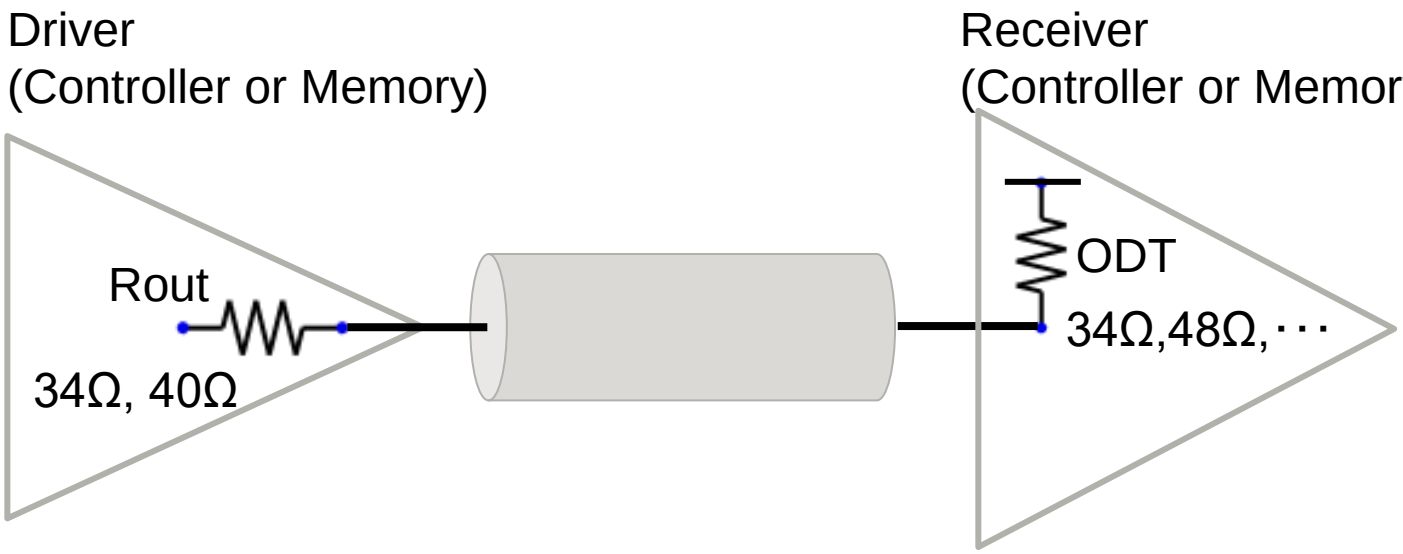






Is the DQ Signal of DDR4 LTI?

DDR4 DQ Signal topology using IBIS



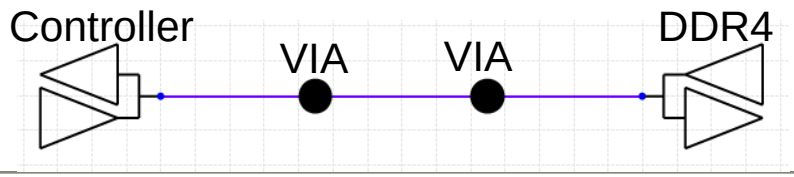
- The resistance value of Rout and ODT is shown in the IBIS model name.
  → Is it good to treat DDR4 DQ Signal as LTI system like SERDES?
- Investigated whether DDR4 DQ Signal was LTI system.

Investigate LTI system of DDR4 Signal

Investigated DDR4 Signals

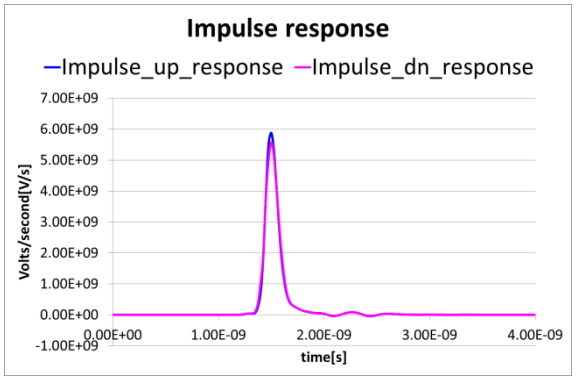
Case	Mbps	Investigated DDR4 Signal		Result
1	1866	DDR4 Signal No.1	Write	Attached
2			Read	-
3	2133	DDR4 Signal No.2	Write	Attached
4			Read	-
5	2400	DDR4 Signal No.3	Write	-
6			Read	-
7	2133	DDR4 Signal No.4	Write	-
8			Read	Attached

- Used Max model of IBIS in the Spice simulation and the Channel simulation.
- Example of the investigated topology



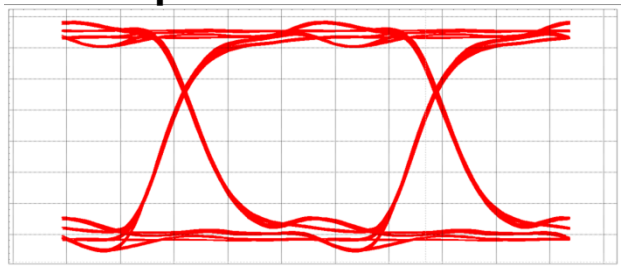
Investigation method

- Confirm the Impulse responses of rising step signal and falling step signal.
  → Are two impulse responses same?

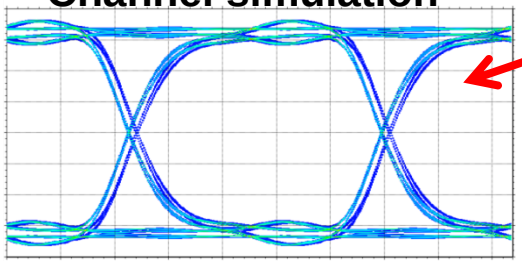


- Comparison between the Spice simulation and the Channel simulation.
  → Is the Channel simulation same as the Spice simulation?

Spice simulation

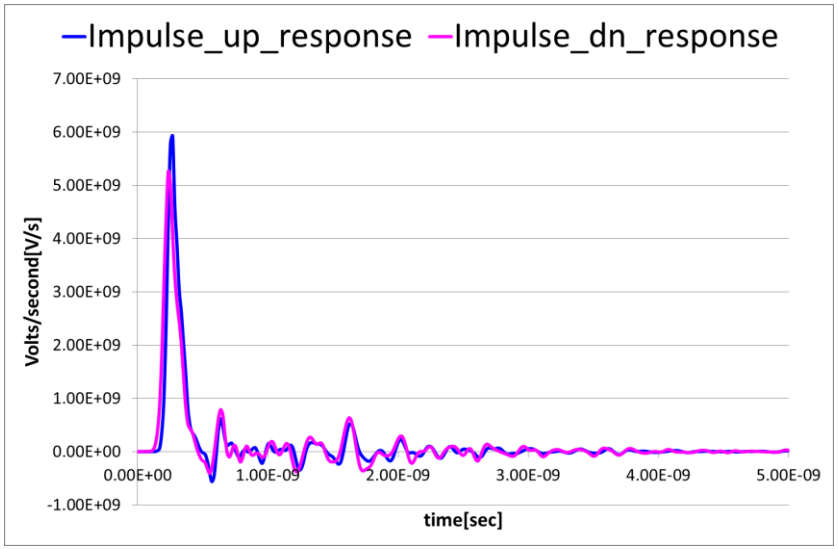


Channel simulation

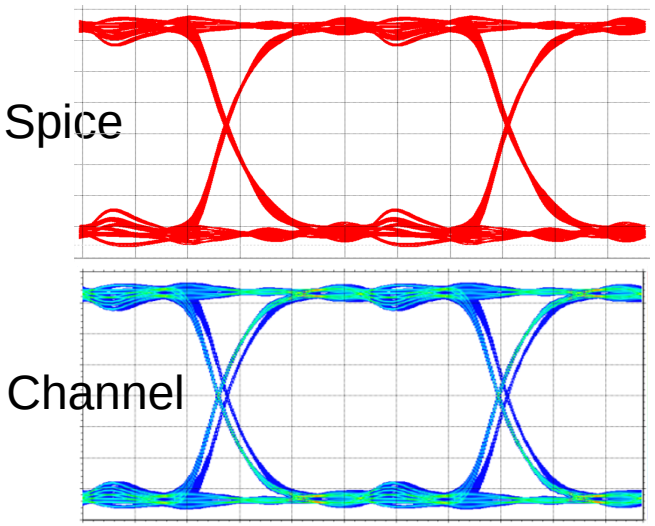


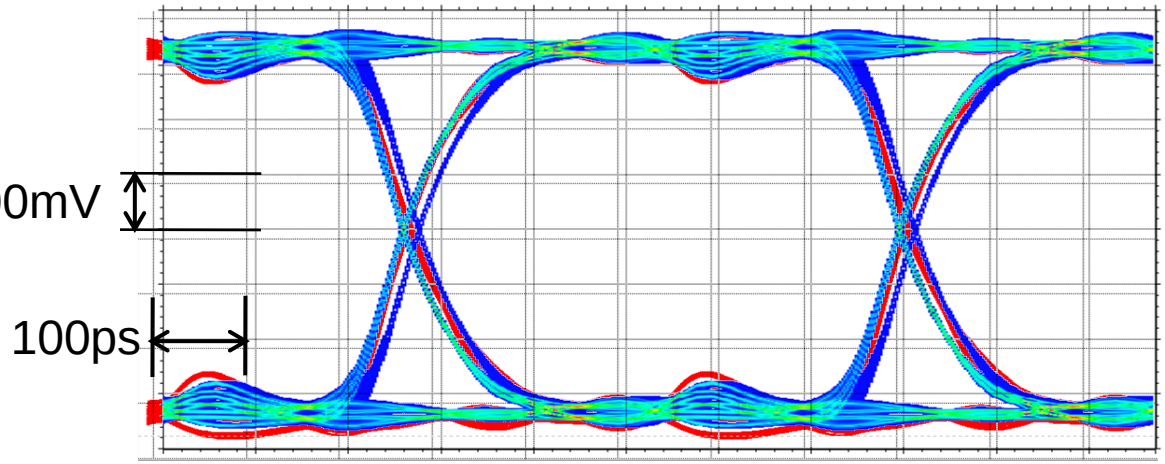
Use the Impulse response by rising step signal. (=Impulse_up_response)

[Case1] DDR4 Signal No.1 Write

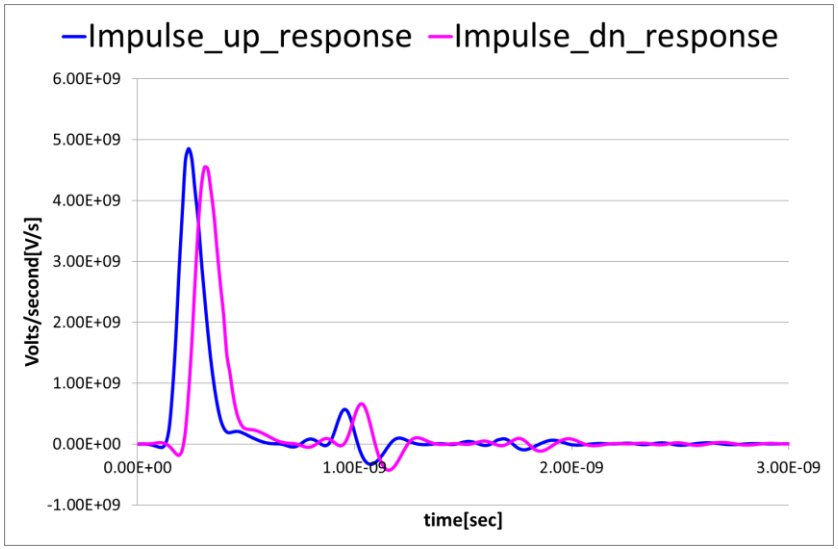


- Impulse response: up≒down
- Eye diagram: Spice≒Channel

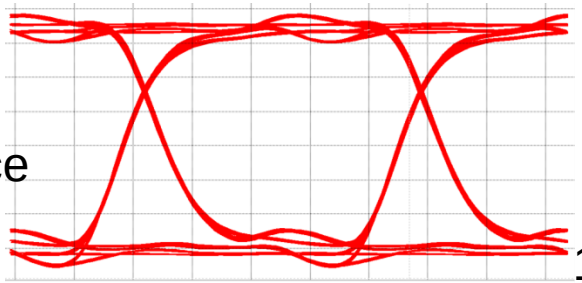




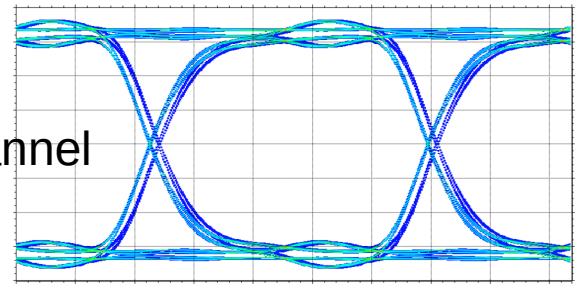
[Case3] DDR4 Signal No.2 Write



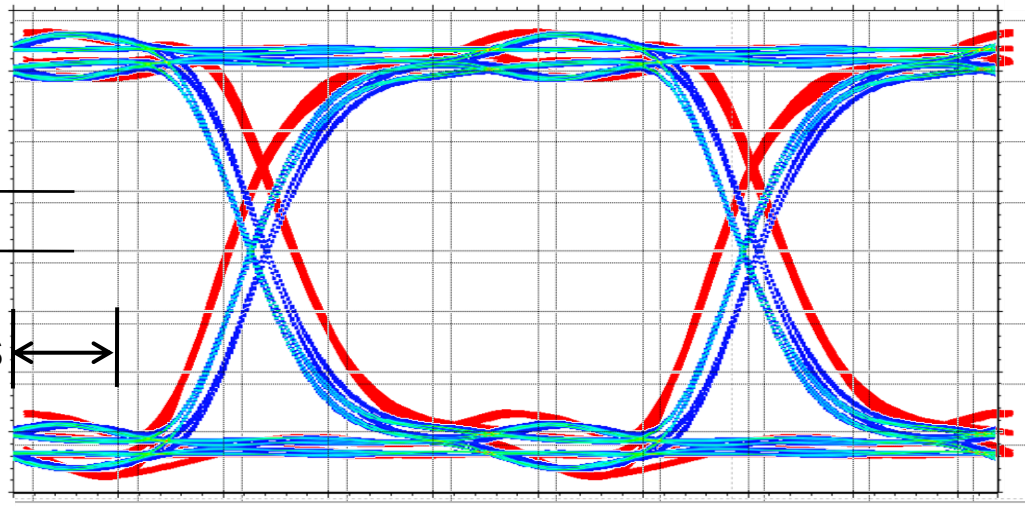
- Impulse response: up≠down
- Eye diagram: Spice≠Channel



Spice



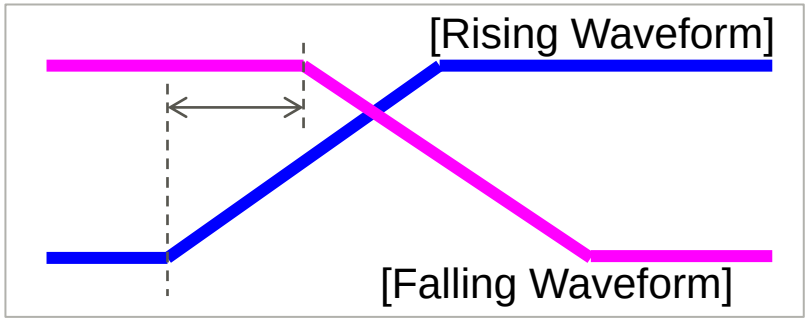
Channel



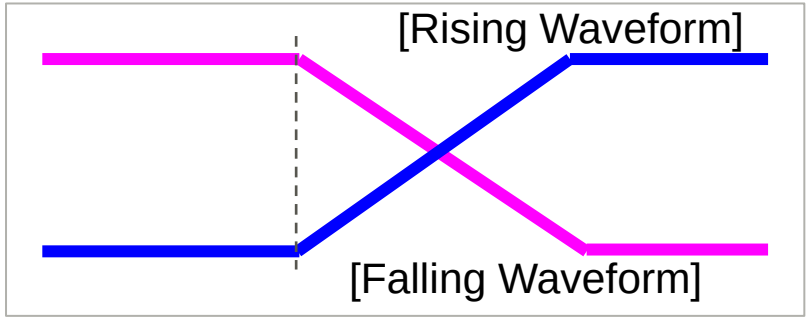
[Case3] DDR4 Signal No.2 Write

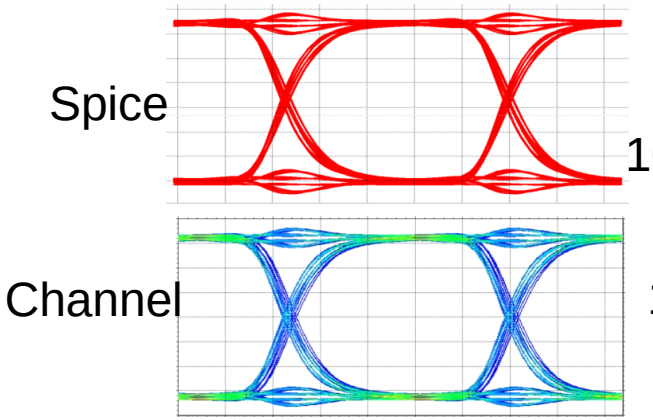
Why is it “Eye diagram: Spice≠Channel”? Checked IBIS.

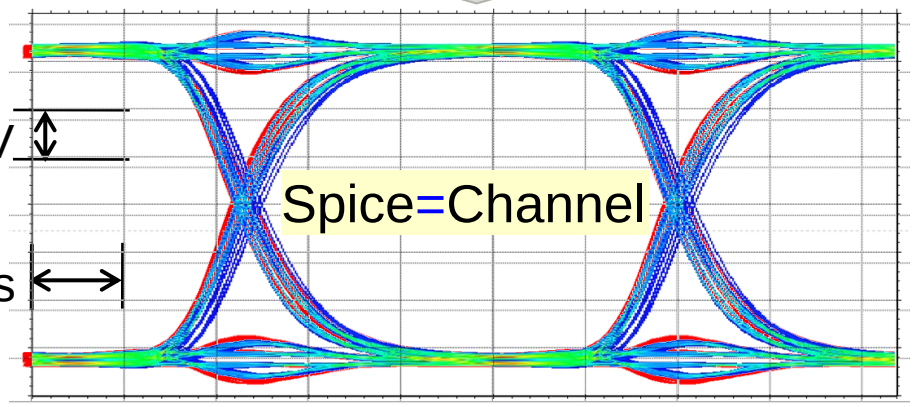
Rising and Falling Waveform of Controller (Driver)
The start of the change are greatly different.



Made the start of the change the same experimentally.

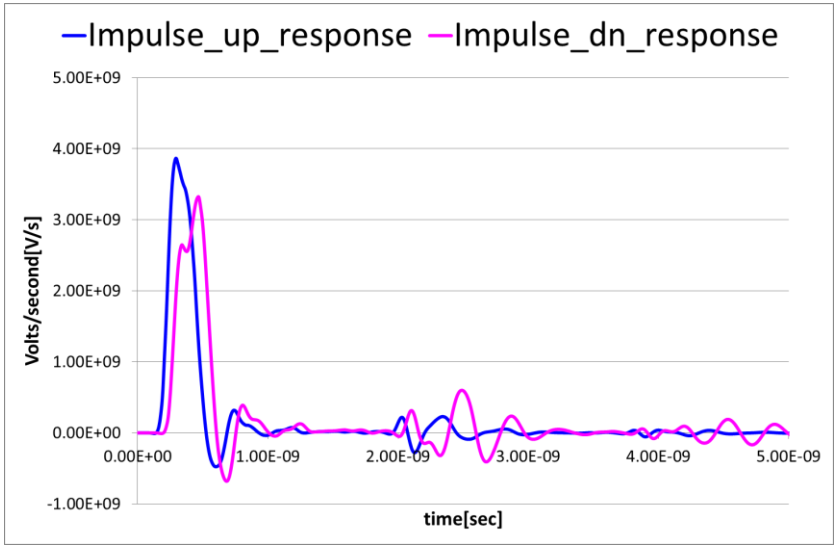




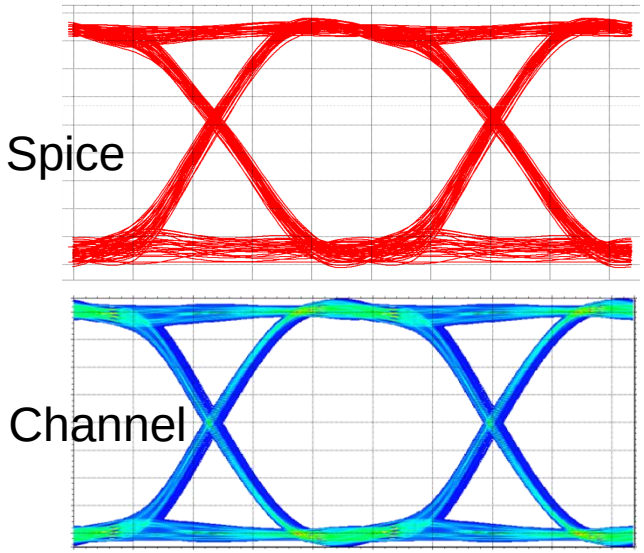


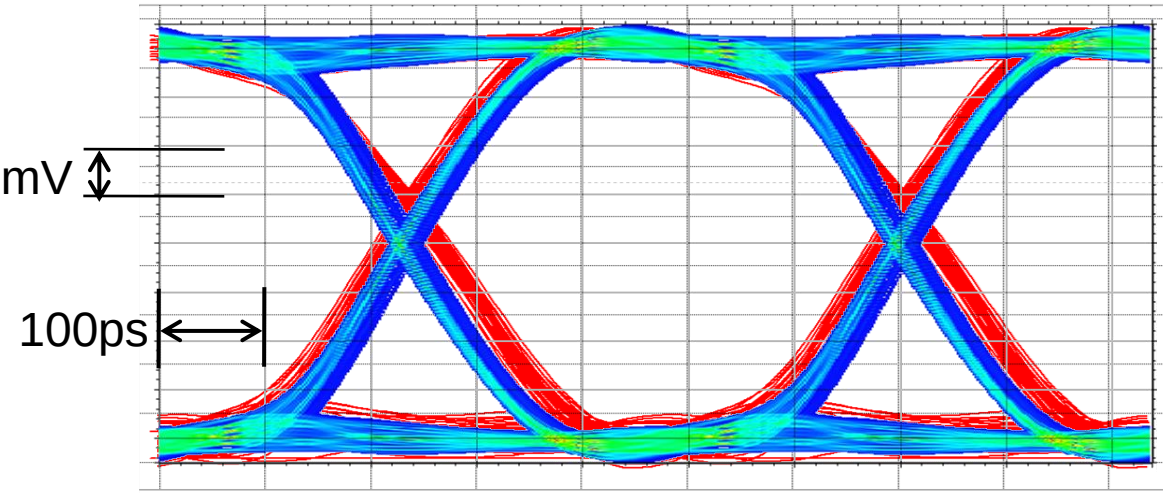
The cause is difference between rise timing and fall timing of the driver.

[Case8] DDR4 Signal No.4 Read



- Impulse response: up≠down
- Eye diagram: Spice≠Channel





[Case8] DDR4 Signal No.4 Read

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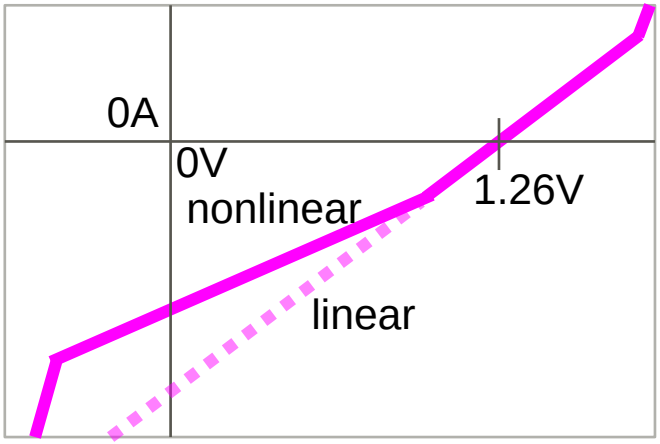
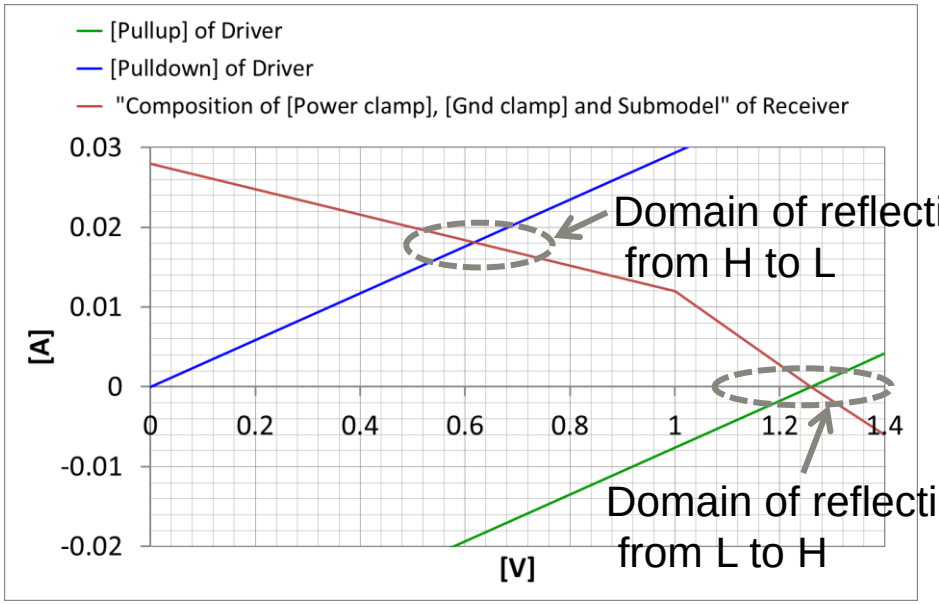
Why is it “Eye diagram: Spice≠Channel”?　Checked IBIS.

Composition of [Power clamp], [GND clamp] and [Submodel] of the Controller (Receiver) .
It is nonlinear.



Reflection from L to H (Up) ≠ Reflection from H to L (Down).
Therefore the Impulse responses are different in “Up” and “Down”.
Used the Up Impulse response in the Channel simulation.



The cause is that the ODT of Receiver is Nonlinear.
(The value of ODT is different in “Up” and “Down”.)

Investigation Results

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Case	Investigated DDR4 Signal		Impulse up=down?	Eye diagram Spice=Channel?
1	DDR4 Signal No.1	Write	close	close
2		Read	same	close
3	DDR4 Signal No.2	Write	different	different
4		Read	close	close
5	DDR4 Signal No.3	Write	close	same
6		Read	close	same
7	DDR4 Signal No.4	Write	close	close
8		Read	different	different

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Summary

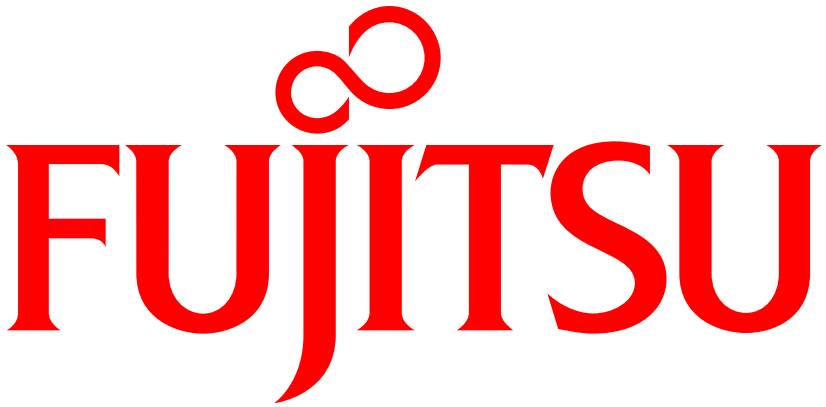
Summary

- Investigated whether DDR4 DQ Signal was LTI system.
- Most of the cases investigated were LTI system.
- However, there were two cases that were not LTI (NLTV: Non Linear Time Variant).
  The reasons why they are not LTI system are as follows.
  1. Driver IBIS: There is a difference at the start time of the Rise and the Fall of Waveform.
  2. Receiver IBIS: ODT (Composition of [Power clamp], [GND clamp] and [Submodel]) is Nonlinear.
- From the above, it is necessary to consider that there are not only LTI but also nonlinear systems (NLTV) in the DDR4 signal.
- Is IO of DDR5 LTI?

References

- “IBIS (I/O Buffer Information Specification) Version 6.1”,
  IBIS Open Forum 2015
  http://www.ibis.org/ver6.1/ for IBIS 6.1

- JEDEC STANDARD DDR4 SDRAM JESD79-4A
  Revision of JESD79-4, September 2012 for DDR4 Standard



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