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shaping tomorrow with you

Investigation of the Package Crosstalk Noise to DDR4-IF Signal by IBIS [Define Package Model]

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Agenda

- Background
- Package Modeling Method
- Crosstalk Noise by Package
- Crosstalk Noise by Package and Board
- Conclusions

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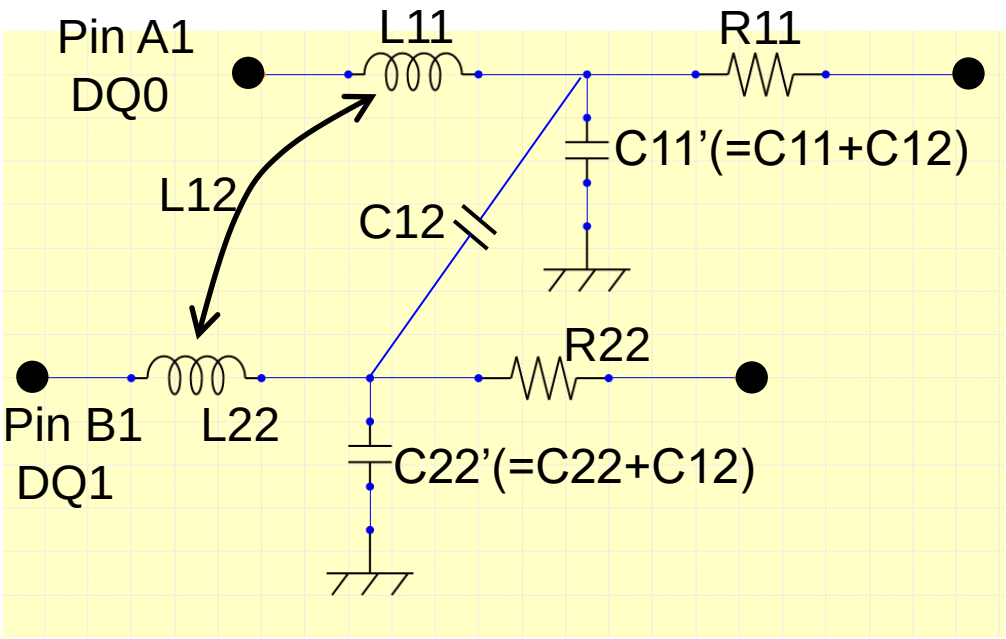
Background

Background

[Define Package Model]

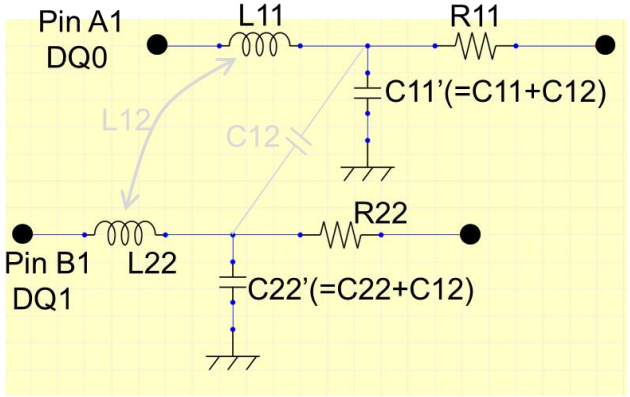
```
[Define Package Model]     FBGA-1000
[Manufacturer]             FICT
[OEM]                      FICT
[Description]              1000 pin BGA package
[Number of Pins]           2
[Pin Numbers]
A1                              |1  DQ0
B1                              |2  DQ1
[Model Data]
|[Resistance Matrix]       Banded_matrix
[Bandwidth]                0
[Row]    A1
1.000                           |R11
[Row]    B1
0.950                           |R22
[Inductance Matrix]        Sparse_matrix
[Row]    A1
A1     5.000e-009               |L11
B1     0.999e-010               |L12
[Row]    B1
B1     5.500e-009               |L22
[Capacitance Matrix]       Sparse_matrix
[Row]    A1
A1     1.500e-012               |C11
B1     -5.000e-013              |C12
[Row]    B1
B1     1.400e-012               |C22
```



Background

Coupled parameters of package are rarely used in the SI simulation.

- Because the board design period is short, own SI simulation is the first priority.
- Because Simulator does not support coupled parameter(C12, L12) modeling.



The board design rule became severe with DDR3, DDR4.
ex.《Skew Constraints》Data to DQS: ±5ps

Therefore the crosstalk noise of the board is designed to become small.

However, the influence of the crosstalk noise of package is unknown.
So investigated it by [Define Package model].

Package Modeling Method

Package Modeling Method

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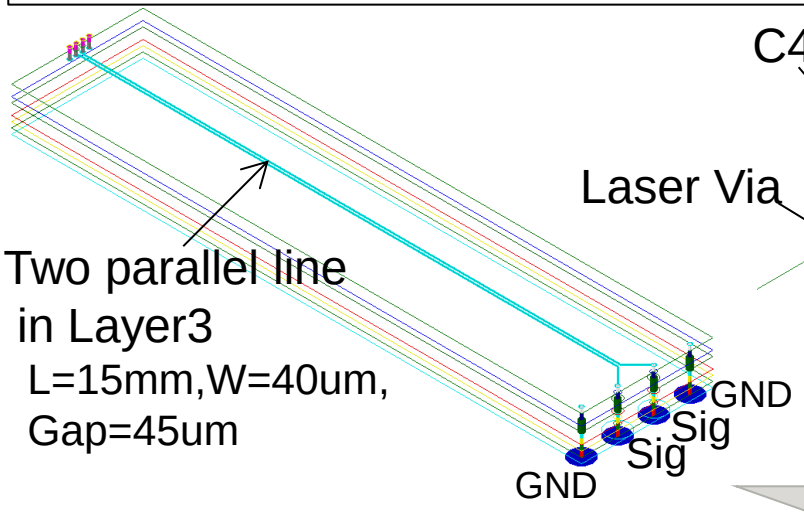
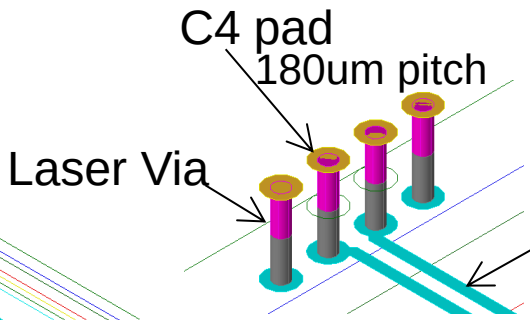
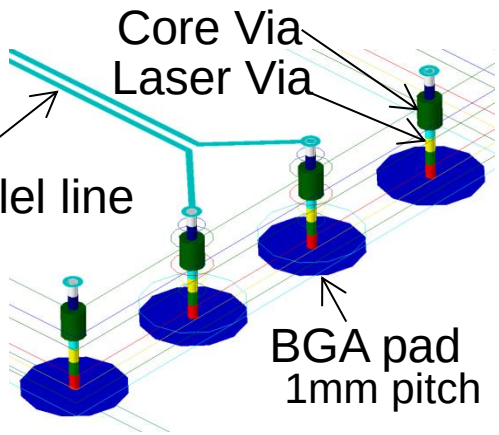
Package Substrate(4-2-4 Buildup) Model



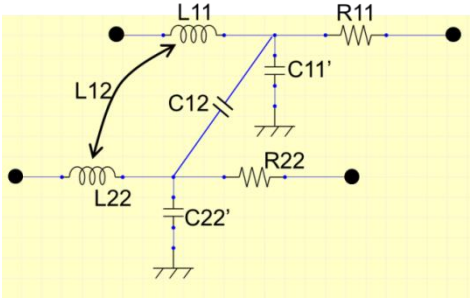




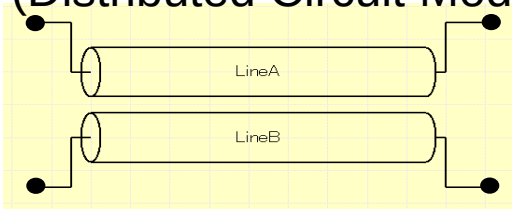
S-parameter

R, Ls, Cs, Lm, Cm

Lumped Circuit Model



W-element RLGC Model
(Distributed Circuit Model)



(Coupled Transmission Line model
in IBIS ISS Specification.)

Package Modeling Method

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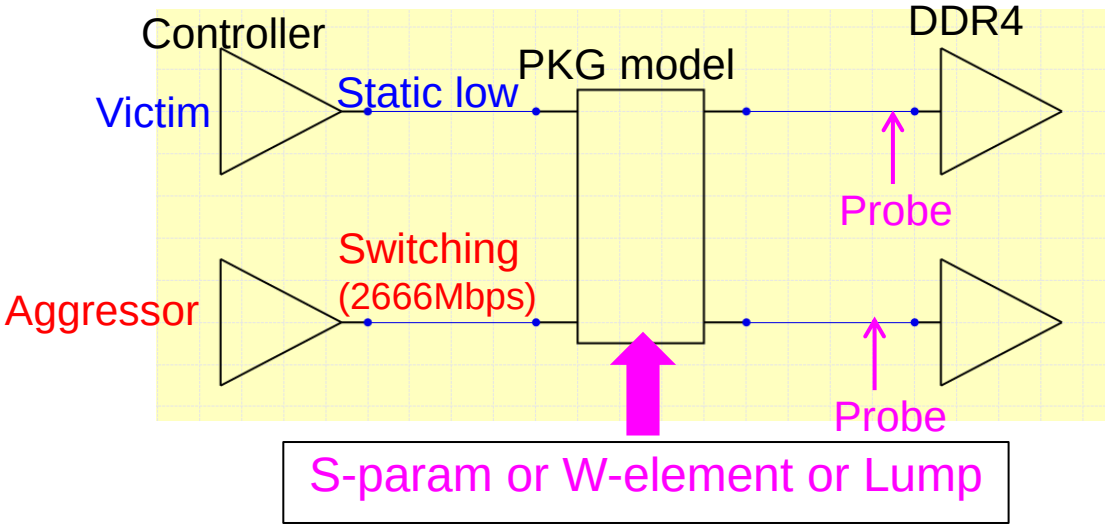
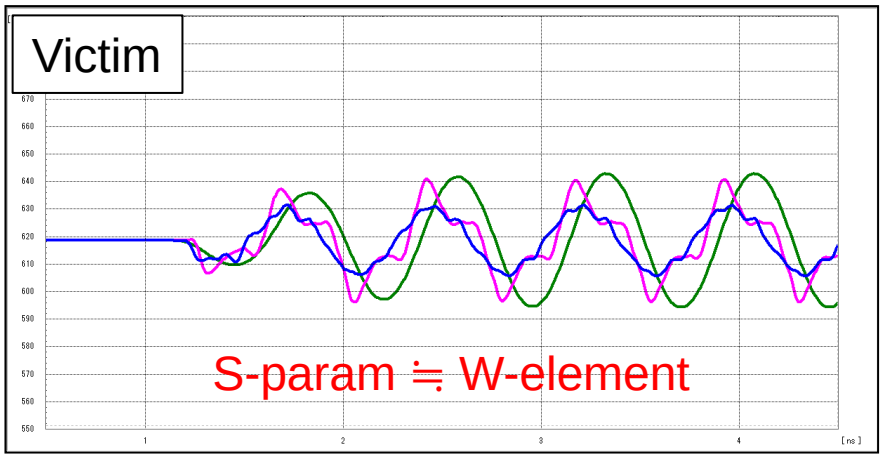
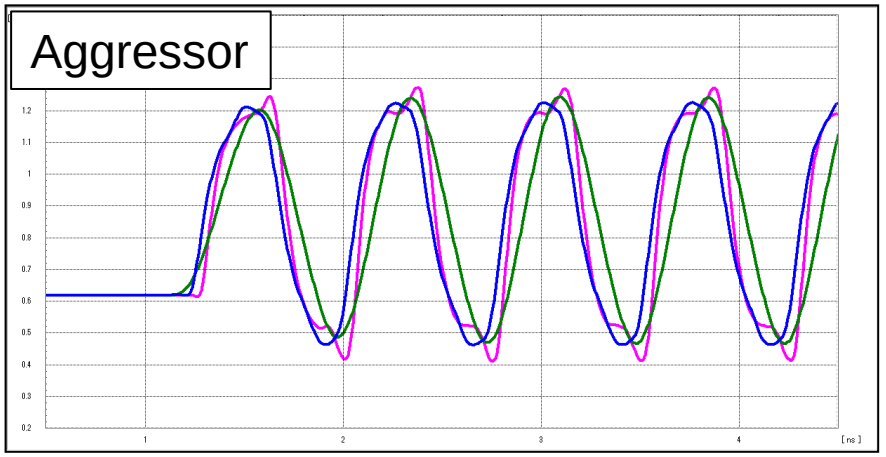
Topology



S-param
W-element
Lump





Choose W-element for package modeling.

How to make of the Coupled Package Model

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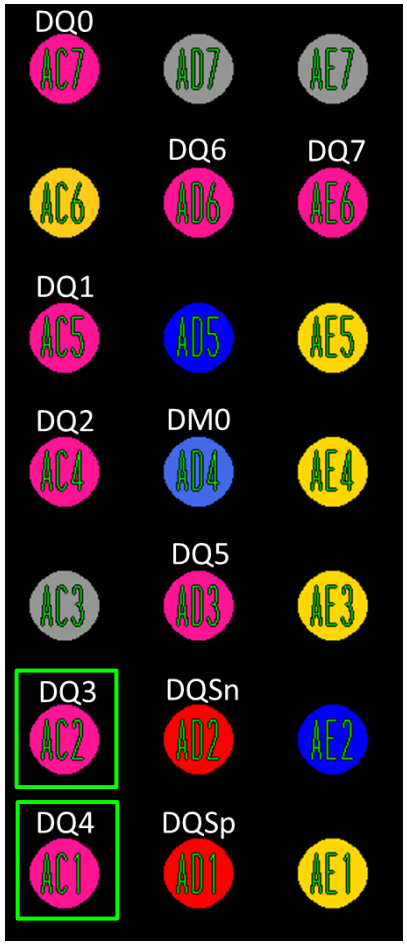
1Byte Data Signal Coupled Package Model

Controller Pin Assign



IBIS [Define Package Model]

```
[Resistance Matrix]    Banded_matrix
[Bandwidth]            0
[Row]    AC1
0.69
[Row]    AC2
0.55

[Inductance Matrix]    Sparse_matrix
[Row]    AC1
AC1      5.64e-009
AC2      0.97e-009
[Row]    AC2
AC2      4.92e-009

[Capacitance Matrix]   Sparse_matrix
[Row]    AC1
AC1      2.68e-012
AC2      -3.59e-013
[Row]    AC2
AC2      2.47e-012
```

W-element description by IBIS-ISS

```
W_controller
+ AC1_die  AC2_die ·····  0
+ AC1_bga AC2_bga ····· 0
+RLGCMODEL=rlgc_controller N=11 L=1

.MODEL rlgc_controller W
+ MODELTYPE=RLGC N=11
+ L0=
$ AC2          AC1 ·····
+ 4.92E-09                    $ AC2
+ 0.97E-09   5.64E-09         $ AC1

+ C0=
$ AC2          AC1 ·····
+ 2.47E-12                    $ AC2
+ -3.59E-13 2.68E-12          $ AC1

+ R0=
$ AC2          AC1 ·····
+ 0.55                        $ AC2
+      0      0.69           $ AC1
```

How to make of the Coupled Package Model

FUJITSU

1Byte Data Signal Coupled Package Model

Subckt description by IBIS-ISS

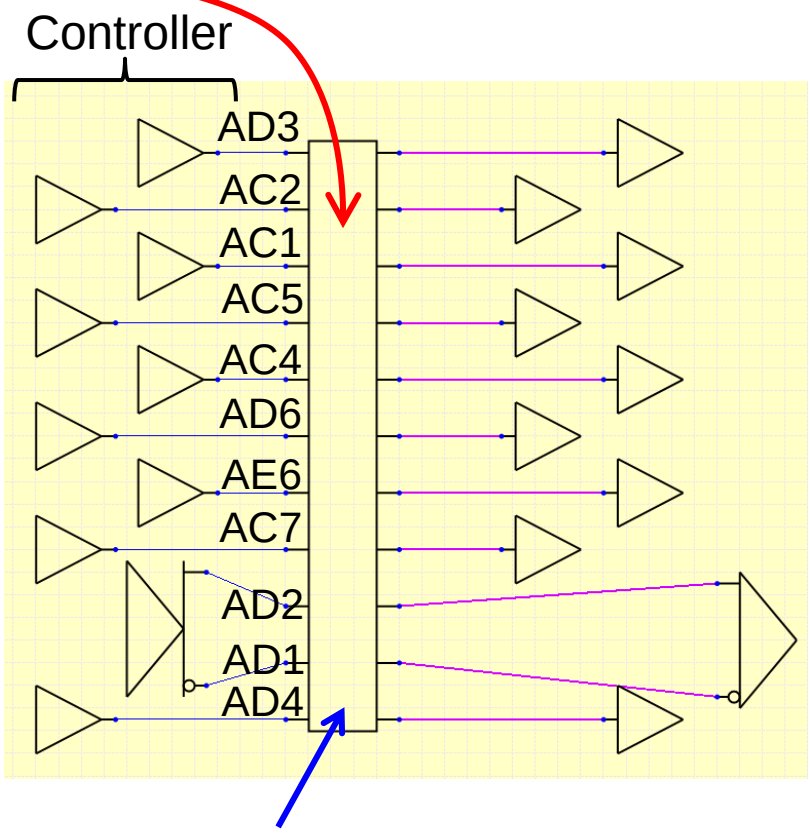
```
.subckt Controller_PKG
+  AC2_die  AC1_die ･･･ AC2_bga  AC1_bga･･･

W_controller
+  AC1_die  AC2_die ･･･････････････  0
+  AC1_bga AC2_bga ･･･････････････ 0
+RLGCMODEL=rlgc_controller N=11 L=1

.MODEL rlgc_controller W
+ MODELTYPE=RLGC N=11
+ L0=
$  AC2          AC1 ･･･････････････
+  4.92E-09                          $ AC2
                 )
+ C0=
$  AC2          AC1 ･･･････････････
+  2.47E-12                          $ AC2
                 )
+ R0=
$  AC2        AC1  ･･･････････････
+   0.55                             $ AC2
                 )

.ends Controller_PKG
```

Simulator Topology



Crosstalk Noise by Package

Crosstalk Noise Level only with a Package

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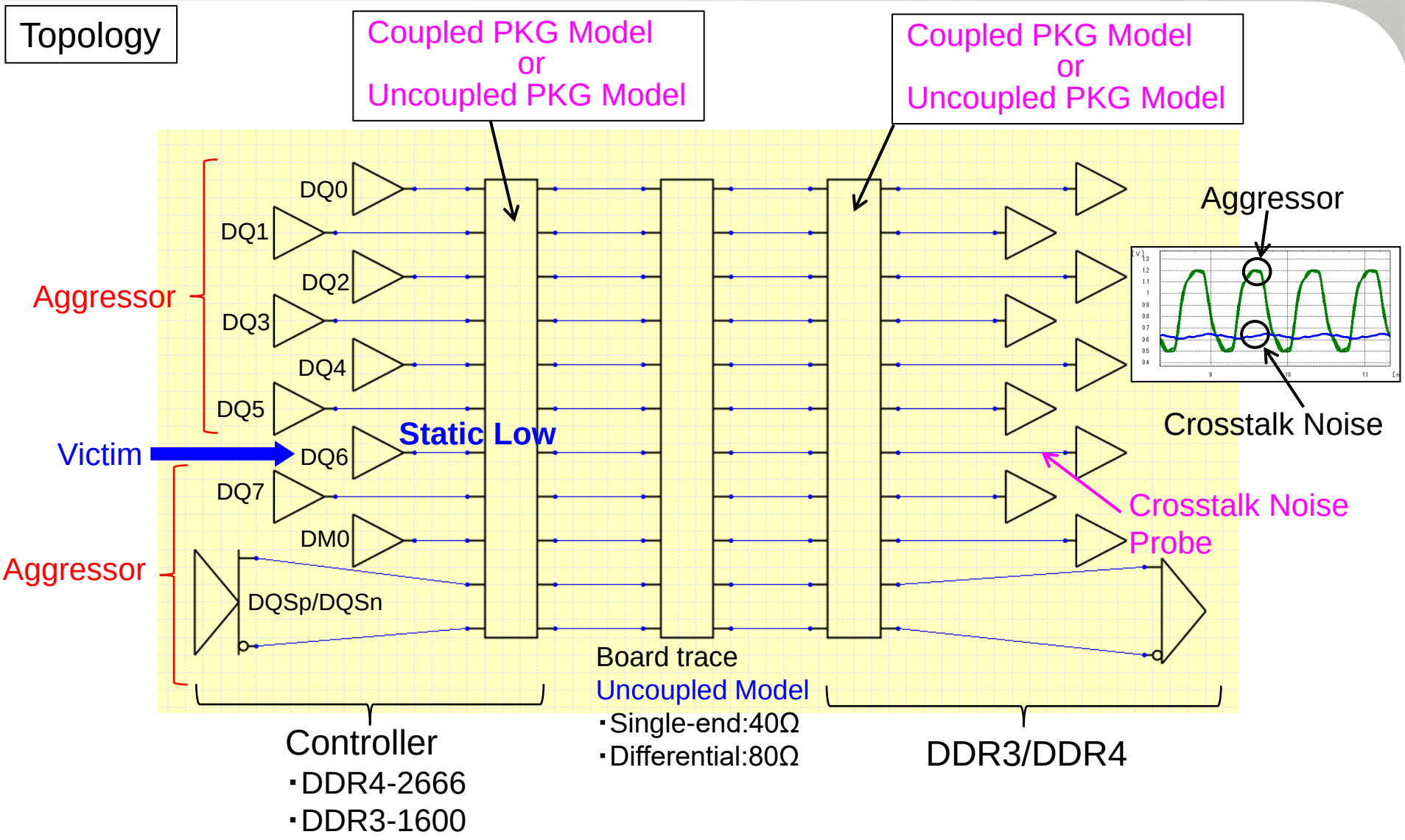
Topology

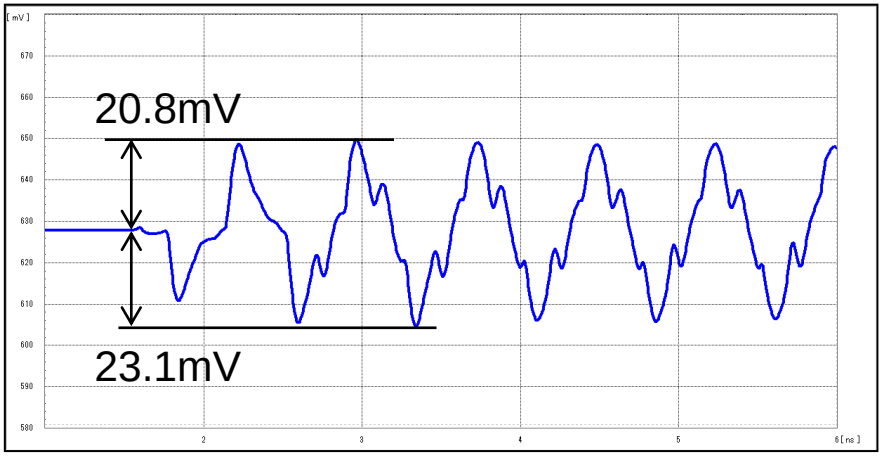


Crosstalk Noise Level only with a Package

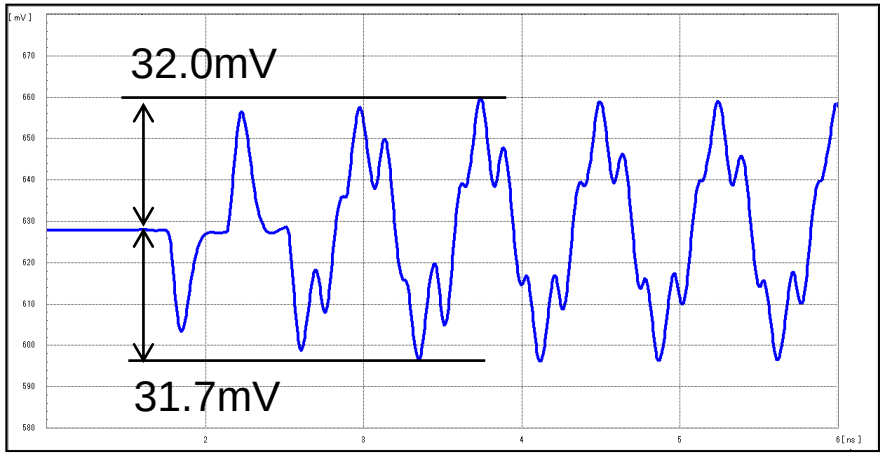
DDR4-2666

Case	DDR4 Controller PKG Model	DDR4 PKG Model	Crosstalk Noise Level
1	Coupled	Uncoupled	23.1mV
2	Uncoupled	Coupled	32.0mV

Case1: Controller PKG Crosstalk Noise



Case2: DDR4 PKG Crosstalk Noise

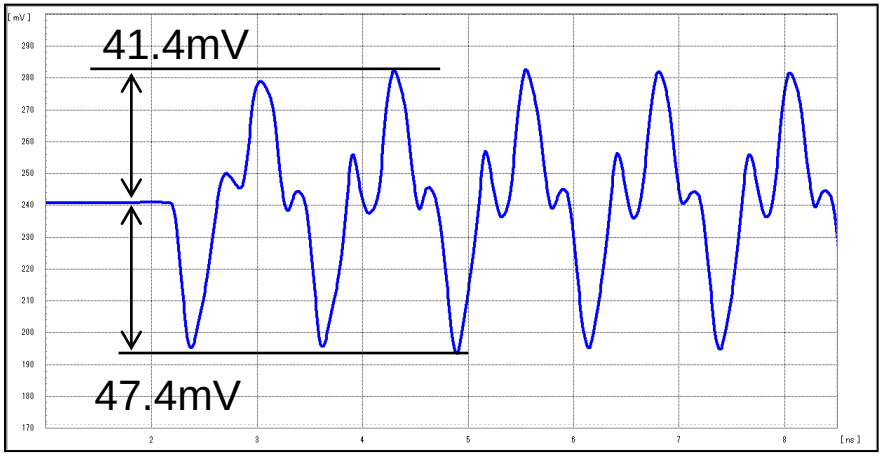


Crosstalk Noise Level only with a Package

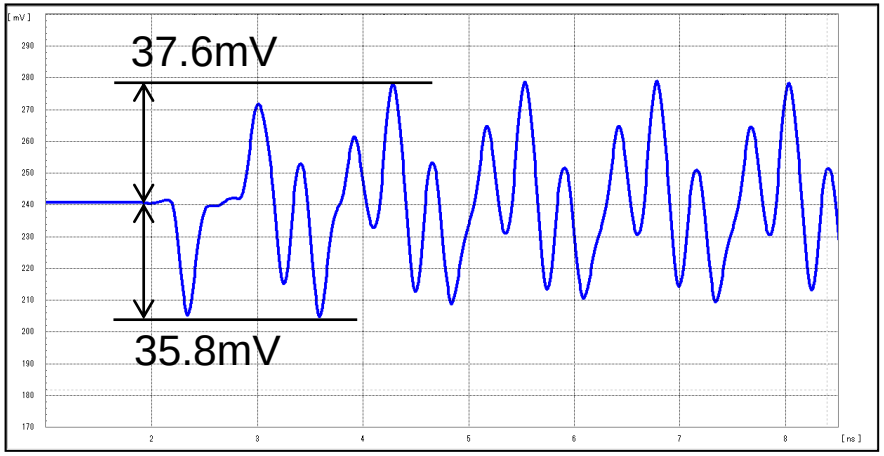
DDR3-1600

Case	DDR3 Controller PKG Model	DDR3 PKG Model	Crosstalk Noise Level
3	Coupled	Uncoupled	47.4mV
4	Uncoupled	Coupled	37.6mV

Case3: Controller PKG Crosstalk Noise



Case4: DDR3 PKG Crosstalk Noise



Skew only by a Package Crosstalk Noise

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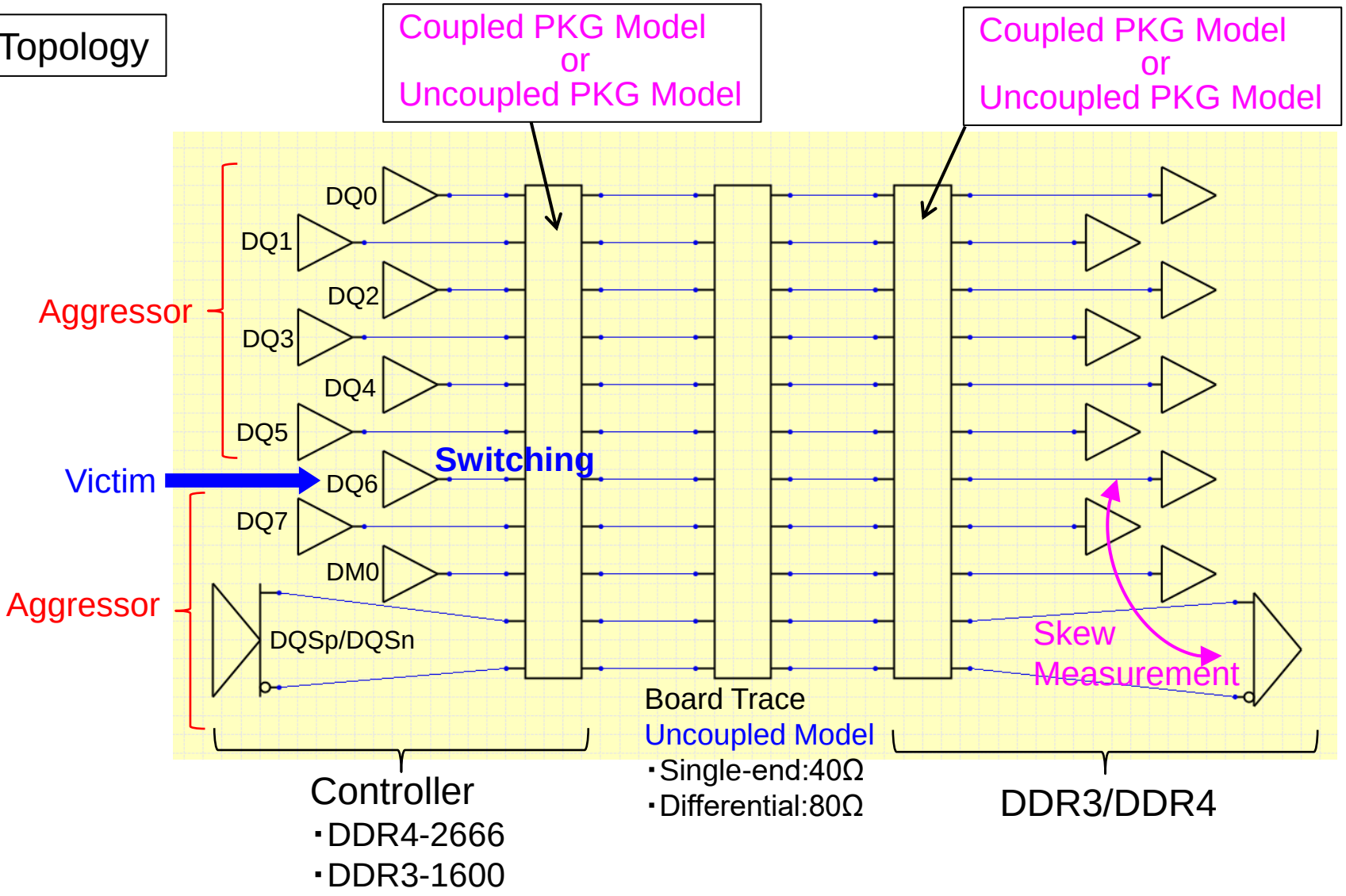
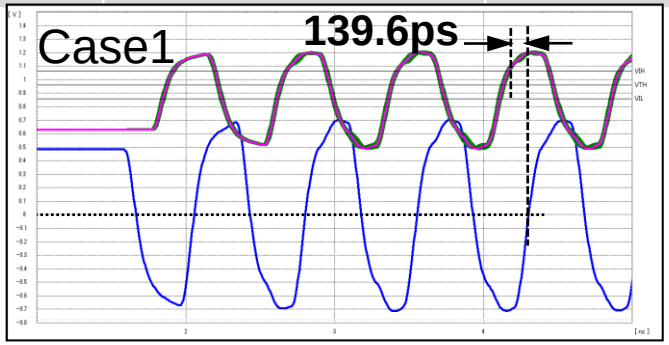
Topology

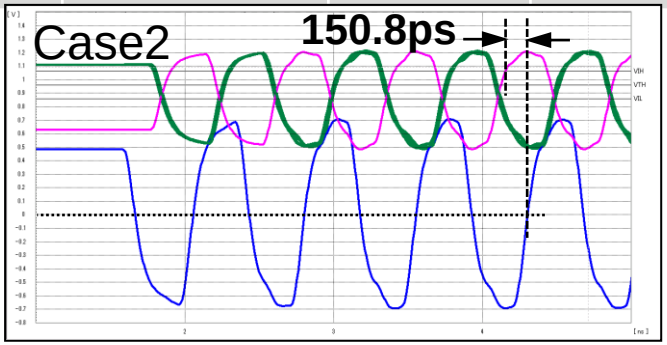


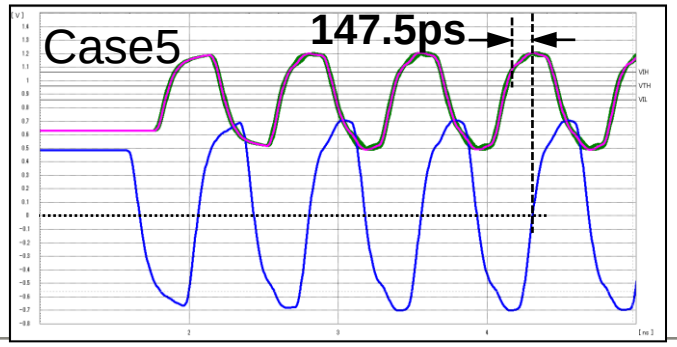
Skew only by a Package Crosstalk Noise

DDR4 -2666

Case	DDR4 Controller PKG Model	DDR4 PKG Model	Switching Pattern(*)	Skew	Skew Variation (Difference with case 5)
1	Coupled	Uncoupled	Even mode	139.6ps	-7.9ps
2	Coupled	Uncoupled	Odd mode	150.8ps	3.3ps
3	Uncoupled	Coupled	Even mode	137.5ps	-10ps
4	Uncoupled	Coupled	Odd mode	153.7ps	6.2ps
5	Uncoupled	Uncoupled	Even mode	147.5ps	---







DQS
Victim DQ
Aggressor DQ

*Switching Pattern

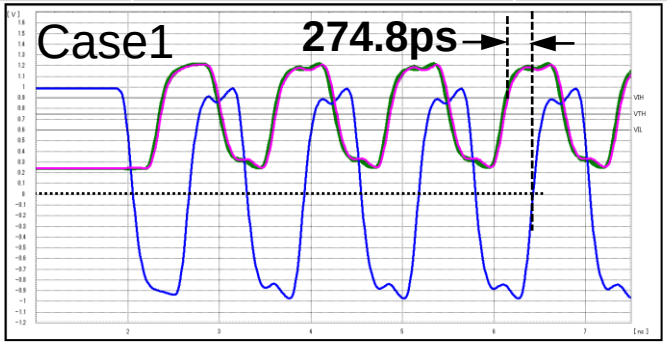
Even mode: Victim
Aggressor

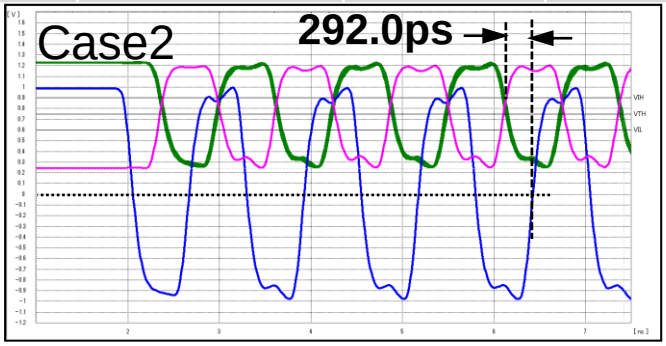
Odd mode: Victim
Aggressor

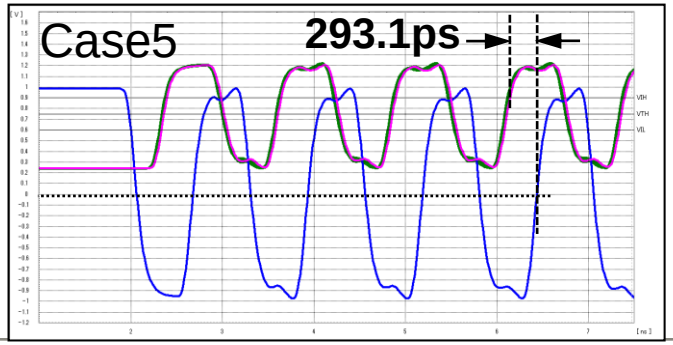
Skew only by a Package Crosstalk Noise

DDR3 -1600

Case	DDR3 Controller PKG Model	DDR3 PKG Model	Switching Pattern	Skew	Skew Variation (Difference with case 5)
1	Coupled	Uncoupled	Even mode	274.8ps	-18.3ps
2	Coupled	Uncoupled	Odd mode	292.0ps	-1.1ps
3	Uncoupled	Coupled	Even mode	277.8ps	-15.3ps
4	Uncoupled	Coupled	Odd mode	296.4ps	3.3ps
5	Uncoupled	Uncoupled	Even mode	293.1ps	---







DQS
Victim DQ
Aggressor DQ

Crosstalk Noise by Package and Board

Crosstalk Noise Level only with a Board

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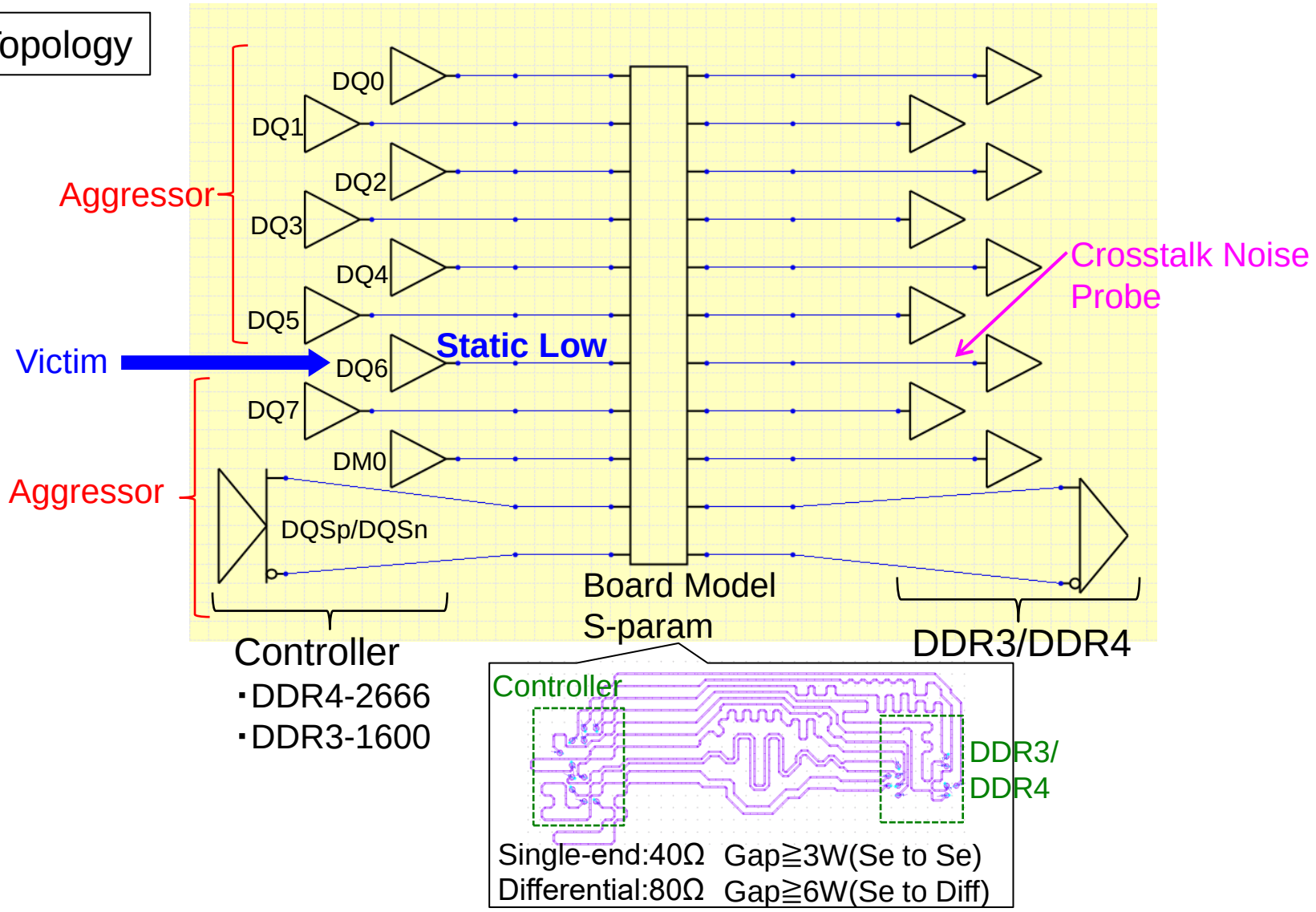
Topology



Crosstalk Noise Level only with a Board

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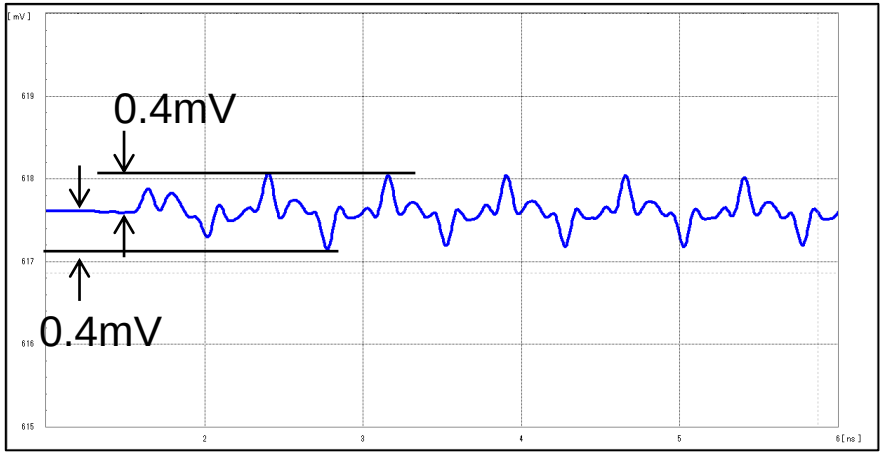
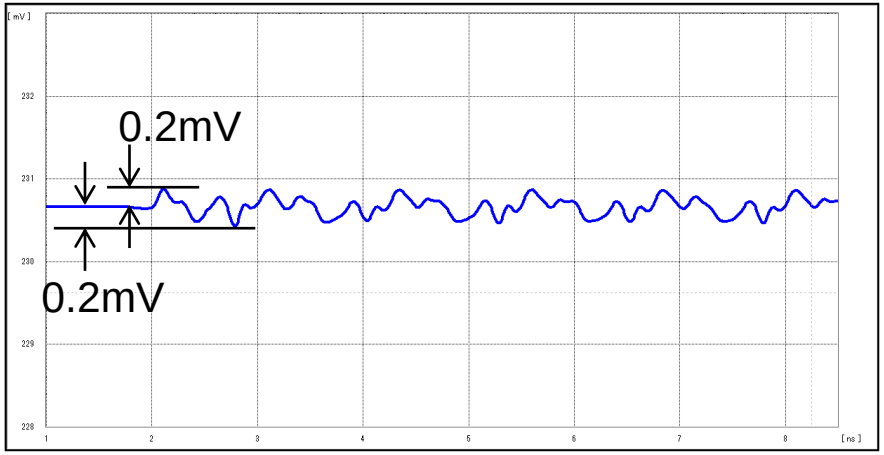
Board Crosstalk Noise Level

Case	Controller PKG Model	Board Model	Memory PKG Model	Crosstalk Noise Level
1	DDR4 Cont. wo PKG	Coupled	DDR4 Mem. wo PKG	0.4mV
2	DDR3 Cont. wo PKG	Coupled	DDR3 Mem. wo PKG	0.2mV

Case1: Board Crosstalk Noise by DDR4-2666

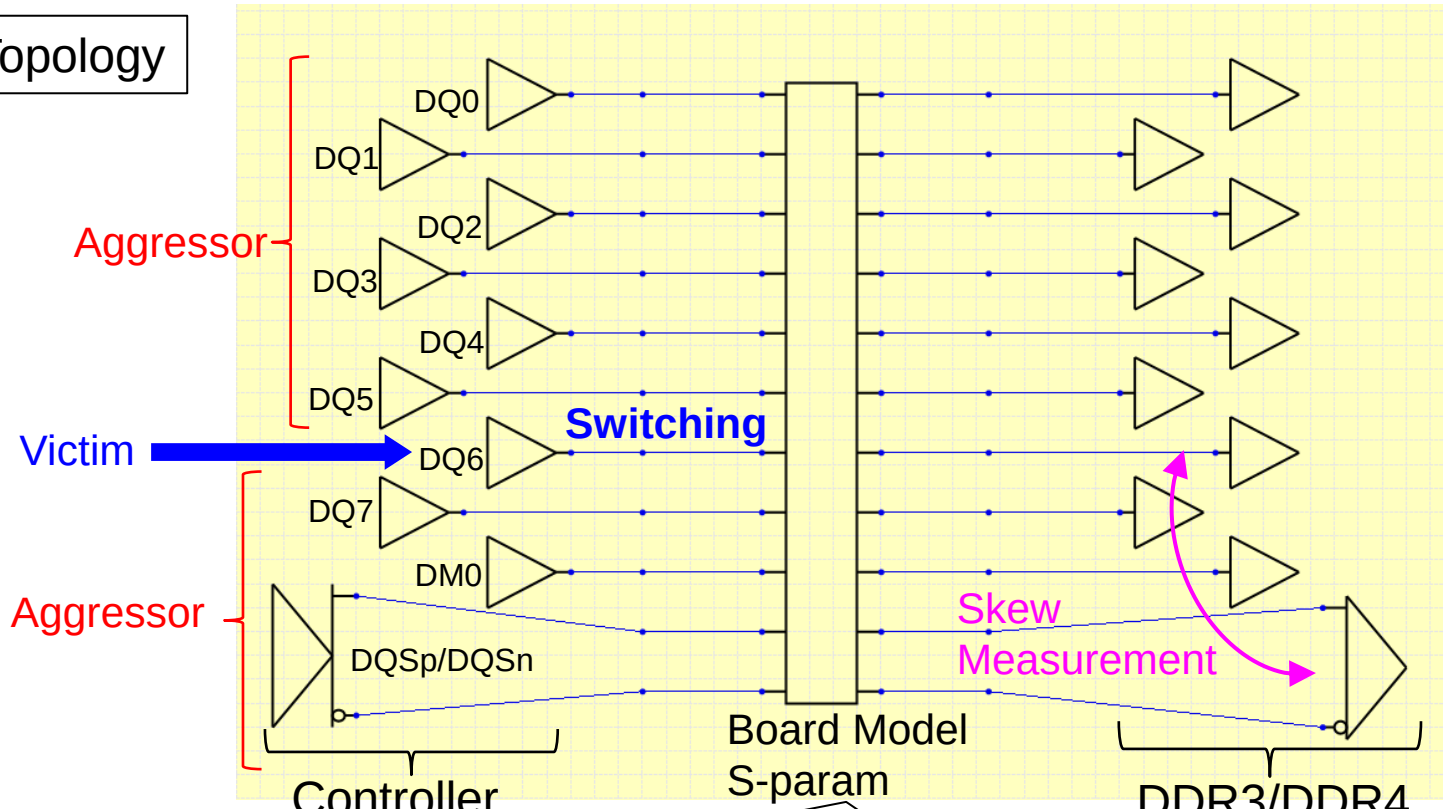


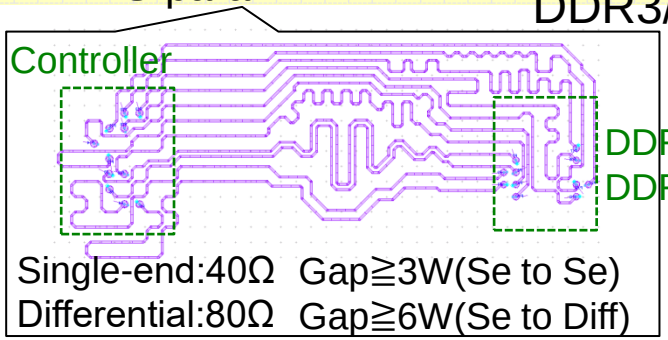
Case2: Board Crosstalk Noise by DDR3-1600



Skew only by a Board Crosstalk Noise

Topology



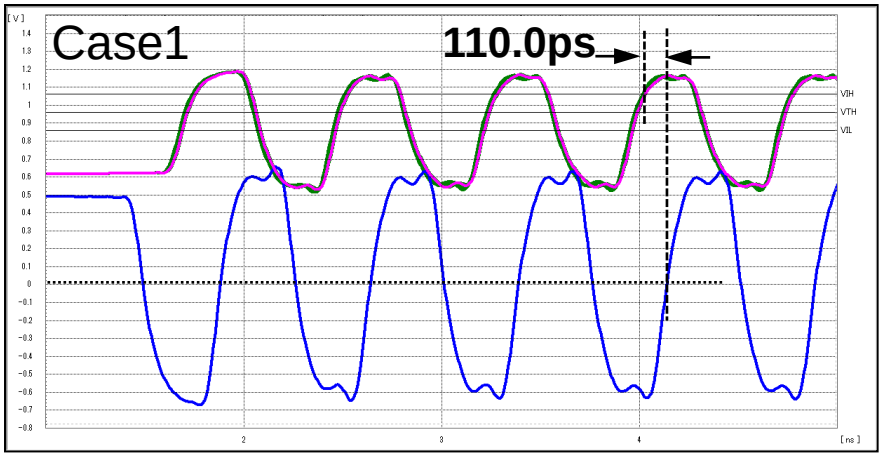


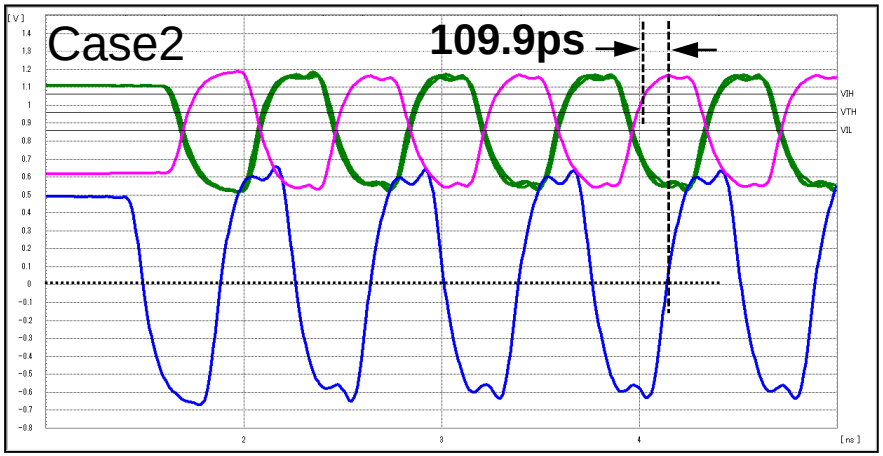
Skew only by a Board Crosstalk Noise

DDR4-2666

Case	DDR4 Cont. PKG Model	Board Model	DDR4 PKG Model	Switching Pattern	Skew	Skew Variation (Difference of case 1 and 2)
1	Nothing	Coupled	Nothing	Even mode	110.0ps	0.1ps
2	Nothing	Coupled	Nothing	Odd mode	109.9ps	

DQS
Victim DQ
Aggressor DQ



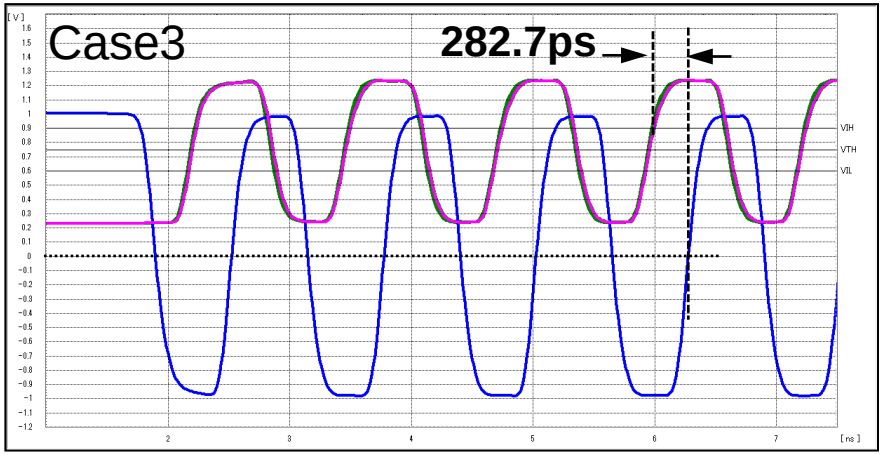


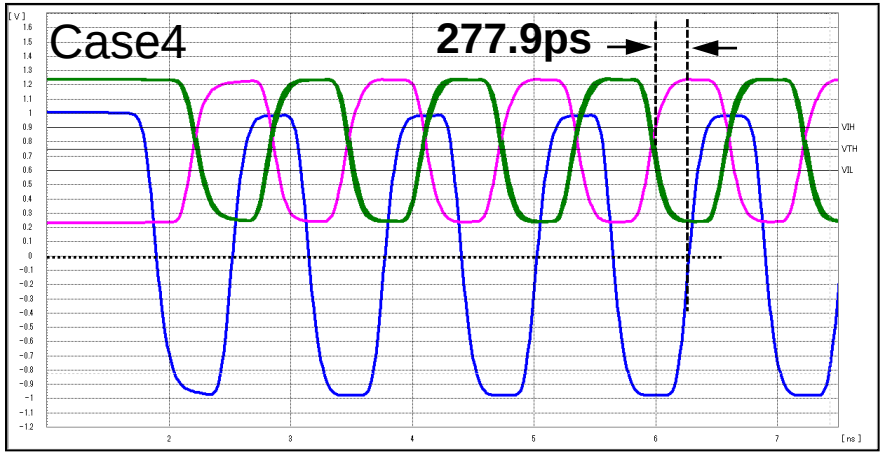
Skew only by a Board Crosstalk Noise

DDR3-1600

Case	DDR3 Cont. PKG Model	Board Model	DDR3 PKG Model	Switching Pattern	Skew	Skew Variation (Difference of case 3 and 4)
3	Nothing	Coupled	Nothing	Even mode	282.7ps	4.8ps
4	Nothing	Coupled	Nothing	Odd mode	277.9ps	

DQS
Victim DQ
Aggressor DQ





Crosstalk Noise Level with Package and Board

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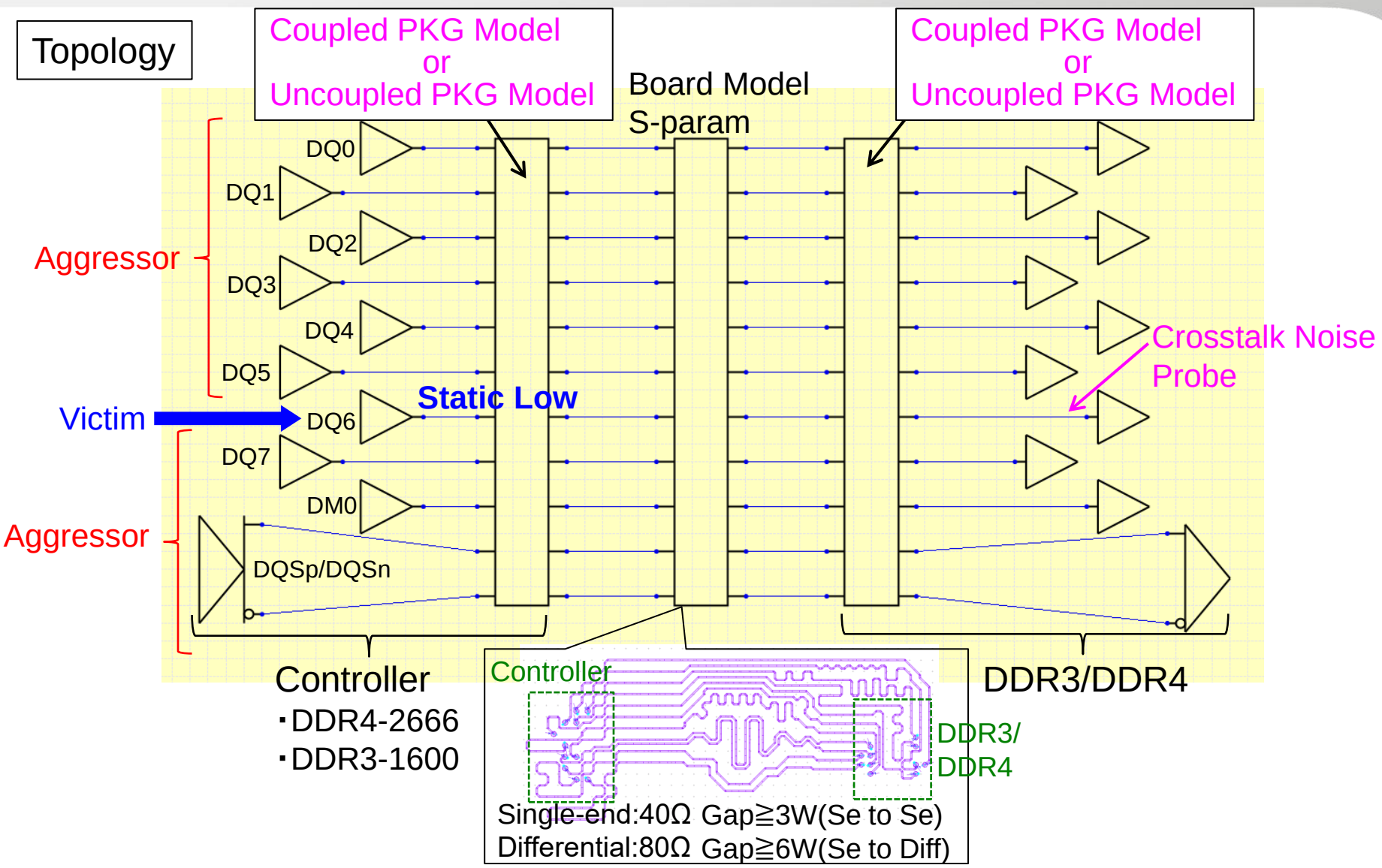
Topology

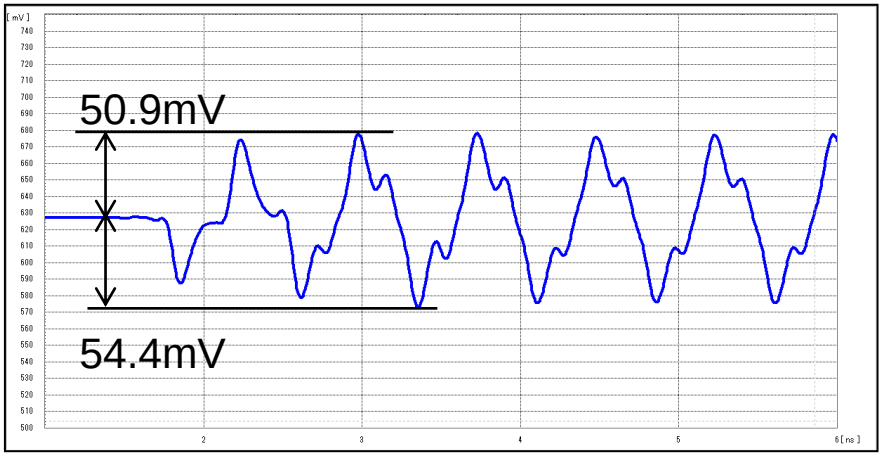


Crosstalk Noise Level with Package and Board

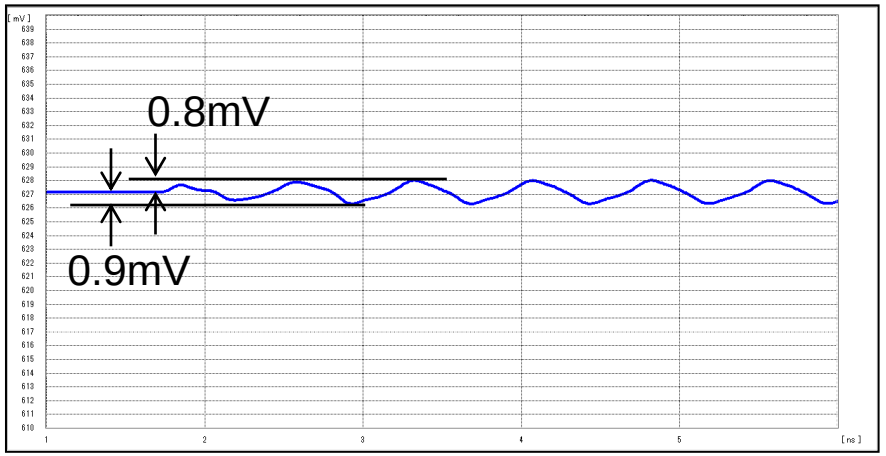
DDR4-2666

Case	DDR4 Controller PKG Model	Board Model	DDR4 PKG Model	Crosstalk Noise Level
1	Coupled	Coupled	Coupled	54.4mV
2	Uncoupled	Coupled	Uncoupled	0.9mV

Case1: Coupled
Controller & DDR4 PKG Model



Case2: Uncoupled
Controller & DDR4 PKG Model

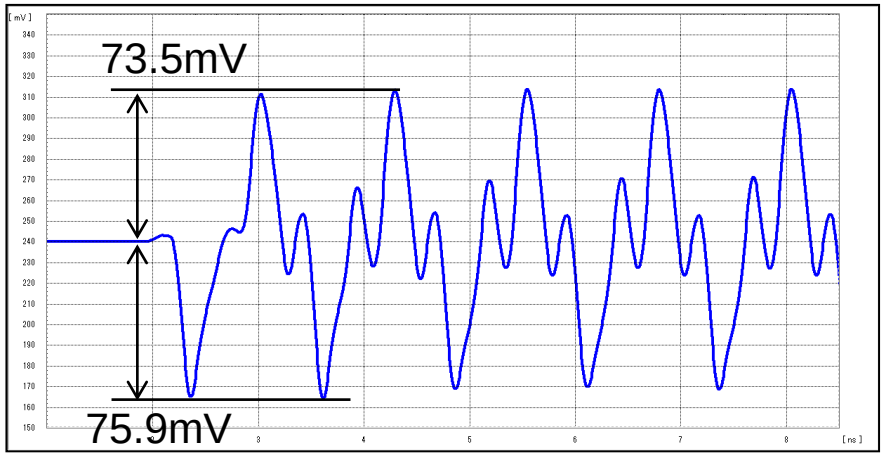


Crosstalk Noise Level with Package and Board

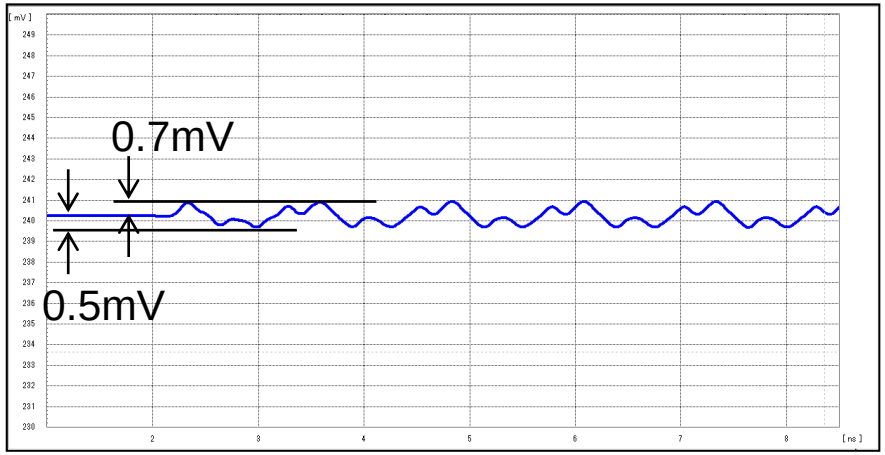
DDR3-1600

Case	DDR3 Controller PKG Model	Board Model	DDR3 PKG Model	Crosstalk Noise Level
3	Coupled	Coupled	Coupled	75.9mV
4	Uncoupled	Coupled	Uncoupled	0.7mV

Case3: Coupled
Controller & DDR3 PKG Model



Case4: Uncoupled
Controller & DDR3 PKG Model



Skew by Package and Board Crosstalk Noise

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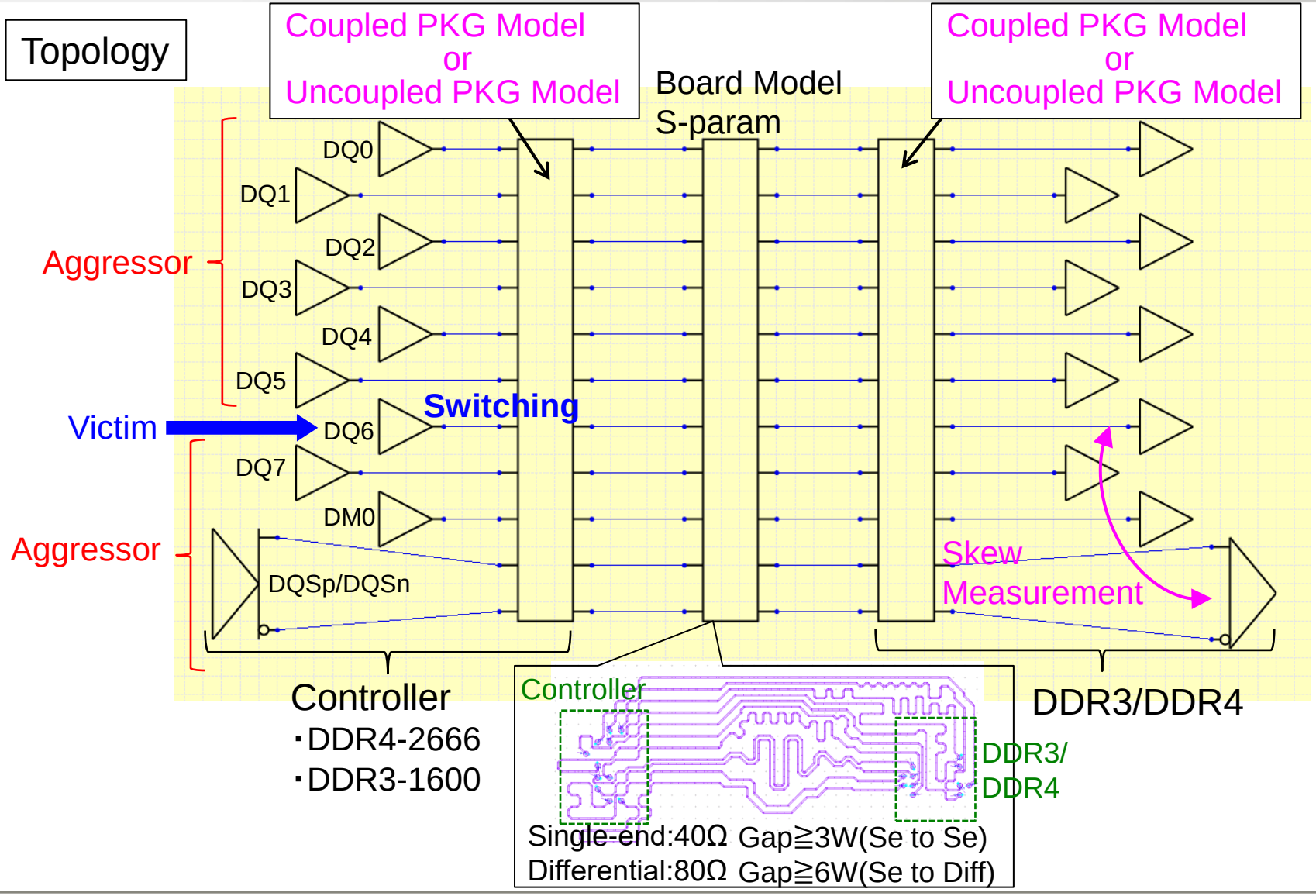
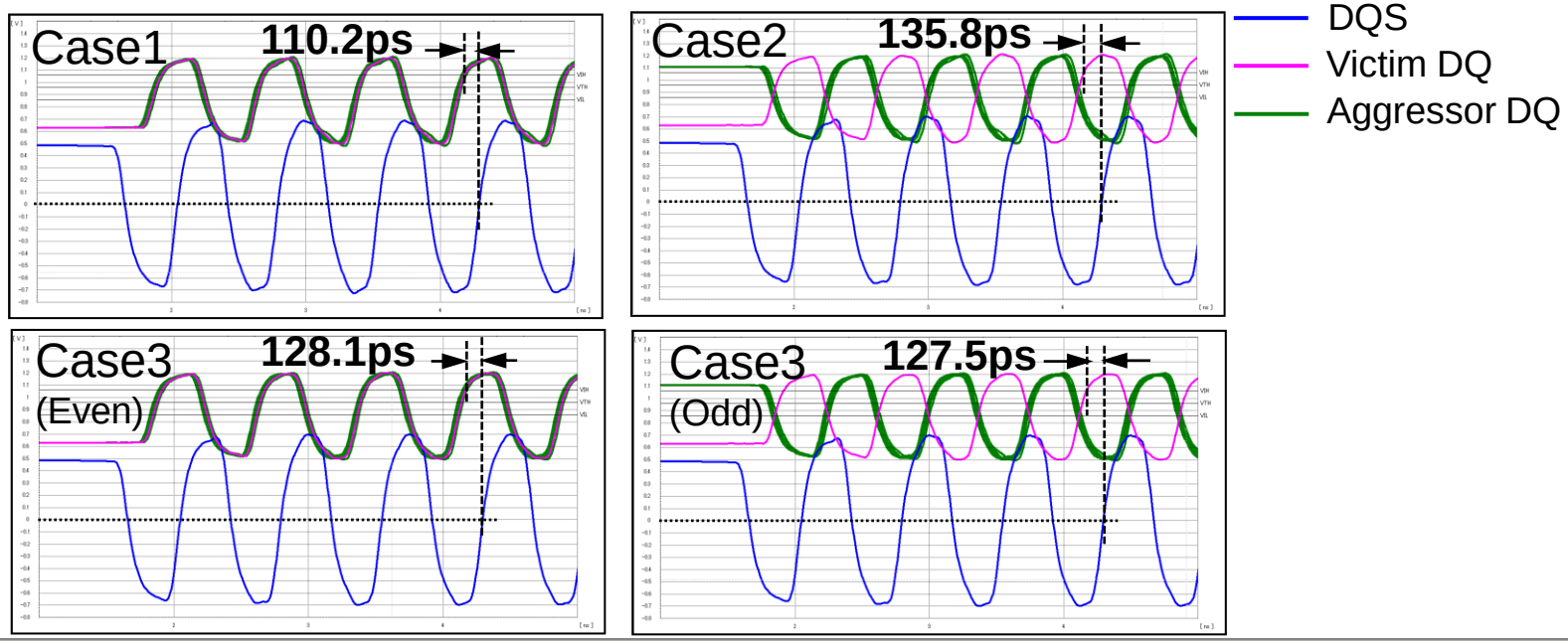
Topology



Skew by Package and Board Crosstalk Noise

DDR4-2666

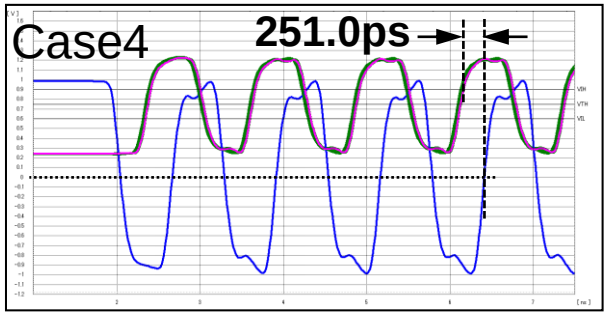
Case	DDR4 Controller PKG Model	Board Model	DDR4 PKG Model	Switching Pattern	Skew	Skew Variation (Difference with case 3)
1	Coupled	Coupled	Coupled	Even mode	110.2ps	-17.6ps
2	Coupled	Coupled	Coupled	Odd mode	135.8ps	8ps
3	Uncoupled	Coupled	Uncoupled	Even/Odd mode Average	127.8ps	---

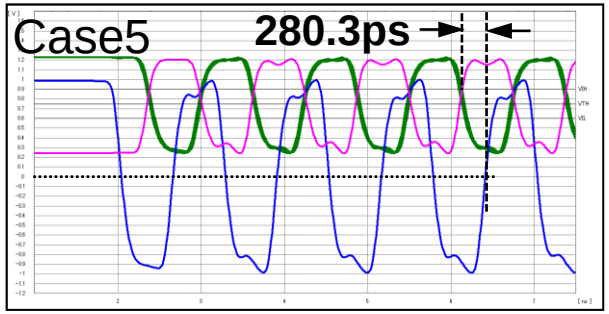


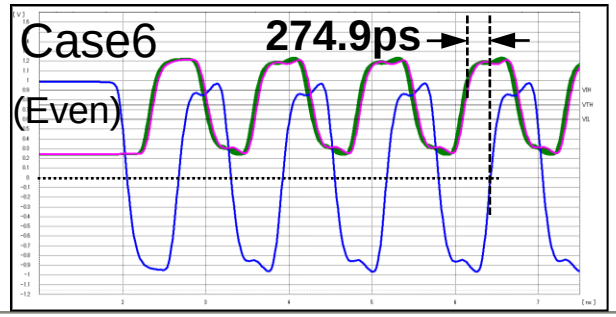
Skew by Package and Board Crosstalk Noise

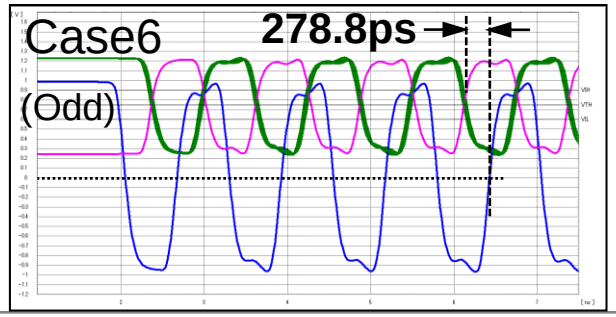
DDR3-1600

Case	DDR3 Controller PKG Model	Board Model	DDR3 PKG Model	Switching Pattern	Skew	Skew Variation (Difference with case 6)
4	Coupled	Coupled	Coupled	Even mode	251.0ps	-25.9ps
5	Coupled	Coupled	Coupled	Odd mode	280.3ps	3.4ps
6	Uncoupled	Coupled	Uncoupled	Even/Odd mode Average	276.9ps	---







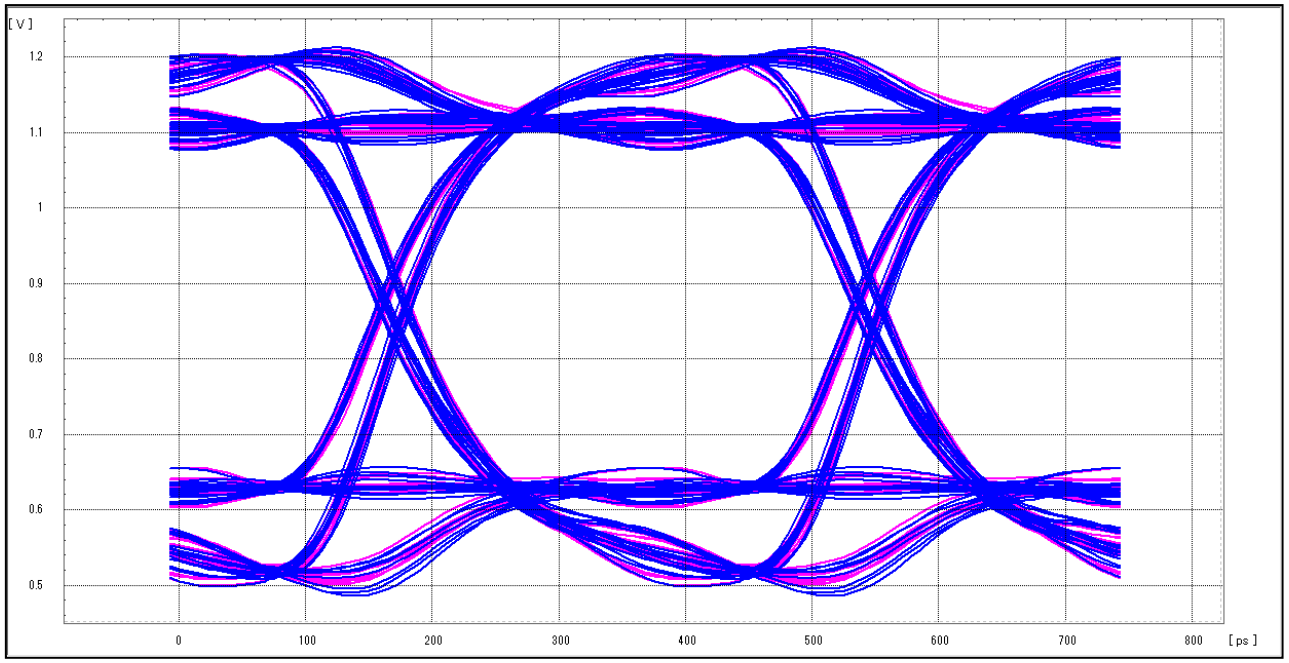


DQS
Victim DQ
Aggressor DQ

Eye Diagram by Package and Board Crosstalk Noise

DDR4-2666

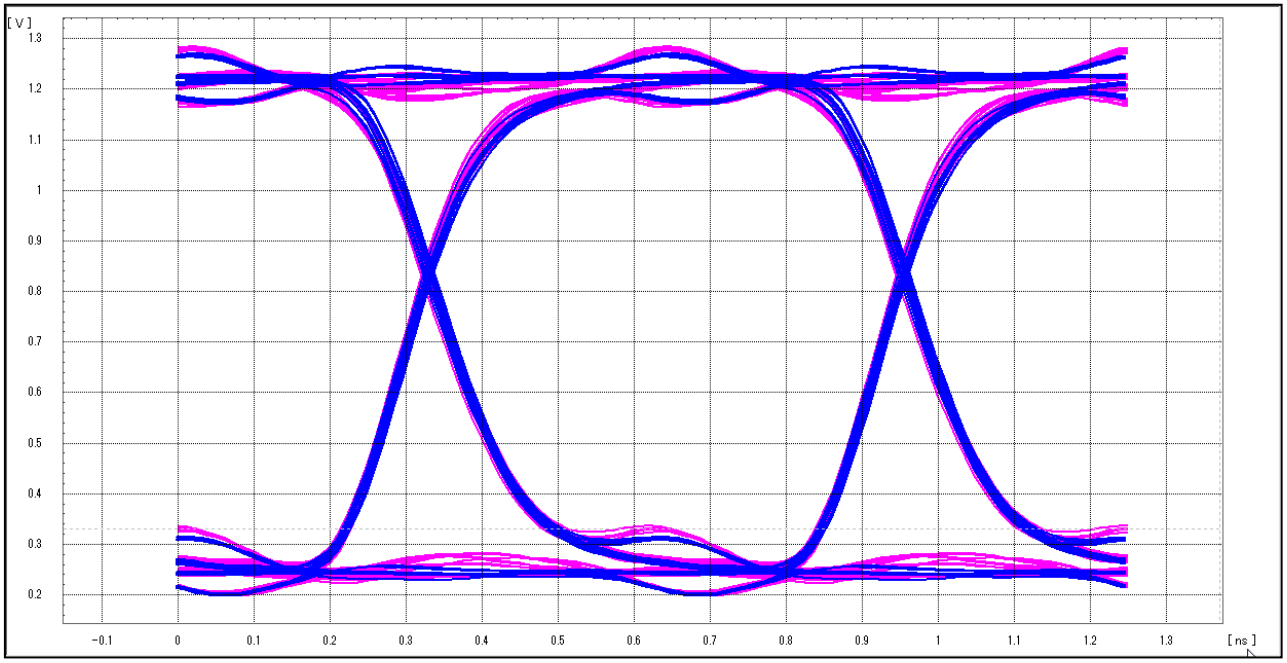
Case	DDR4 Controller PKG Model	Board Model	DDR4 PKG Model	Random Pattern
1	Coupled	Coupled	Coupled	PRBS2^7-1
2	Uncoupled	Coupled	Uncoupled	



Eye Diagram by Package and Board Crosstalk Noise

DDR3-1600

Case	DDR3 Controller PKG Model	Board Model	DDR3 PKG Model	Random Pattern
3	Coupled	Coupled	Coupled	PRBS2^7-1
4	Uncoupled	Coupled	Uncoupled	



Case3

Case4

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Conclusions

Conclusions

- The crosstalk noise of the package of controller and DDR3/4 is 20~50mV each.
- The skew variation by the crosstalk noise of the package of controller and DDR3/4 is 20ps each.
- These are bigger than noise level (0mV) and the skew variation (<5ps) of the DDR4-IF board which we used in this investigation.
- The crosstalk noise when we connected the coupled model of controller, board and DDR3/4 became almost the value that added the noise level of each model.
  (DDR4: 54.4mV≒23.1mV+0.4mV+32.0mV=55.5mV, DDR3: 75.9mV≒47.4mV+0.2mV+37.6mV=85.2mV)
- The skew variation when we connected the coupled model of controller, board and DDR3/4 became almost the value that added the skew of each model.
  (DDR4: 25.6ps≒11.2ps+16.2ps=27.4ps, DDR3: 29.3ps≒17.2ps+18.6ps=35.8ps)
- The Eye Diagram when we connected the coupled model of controller, board and DDR3/4, had little influence by the crosstalk noise.
  This is because all bits did not change at the same time and in the same direction for a random pattern.

Conclusions

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- The above skew exceeds the rule of the board design guide of the IC vendor.
- The crosstalk noise of the package cannot control the IC user.
- Therefore it is thought that the IC vendor decides the rule of the board design guide of DDR-IF in consideration of the skew variation by package crosstalk noise.
  In addition, it is supposed that the skew adjustment function of the controller IC coordinates the skew by the package crosstalk noise more than rules.
- In the case of DDR3, DDR4, there is not a rule to judge the good or bad even if we simulate a skew variation by the package crosstalk noise.
- In the case of former PCI-IF, SDR-SDRAM, DDR-SDRAM, a user calculated a timing margin using the AC specifications of the IC and decided a board design rule.
  Therefore the coupled package model was necessary to consider the skew variation of package.
- But in the case of DDR3, DDR4, we think that it does not have to do simulation including coupled package model, because rule of skew and pitch between signals of the board are given from the IC vendor.

References

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  IBIS Open Forum 2015
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- “IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0”,
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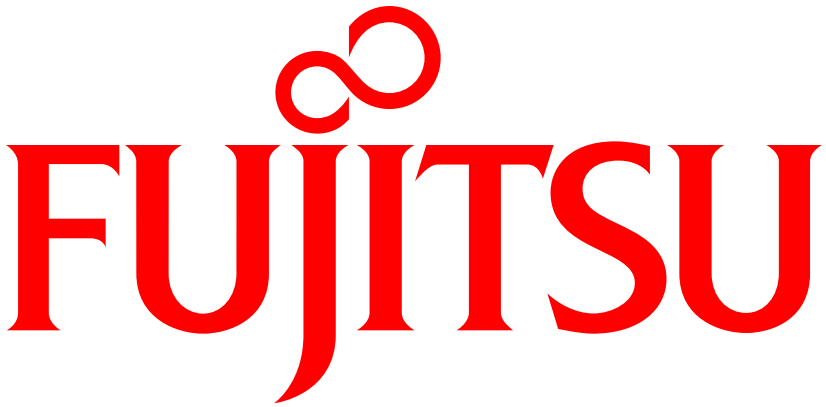

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