DDR System Simulation: What Issue to Simulate

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Shinichi Maeda

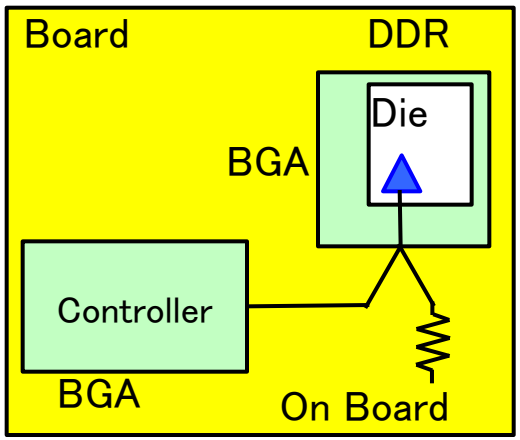
KEI Systems

JEDEC DDR Specifications

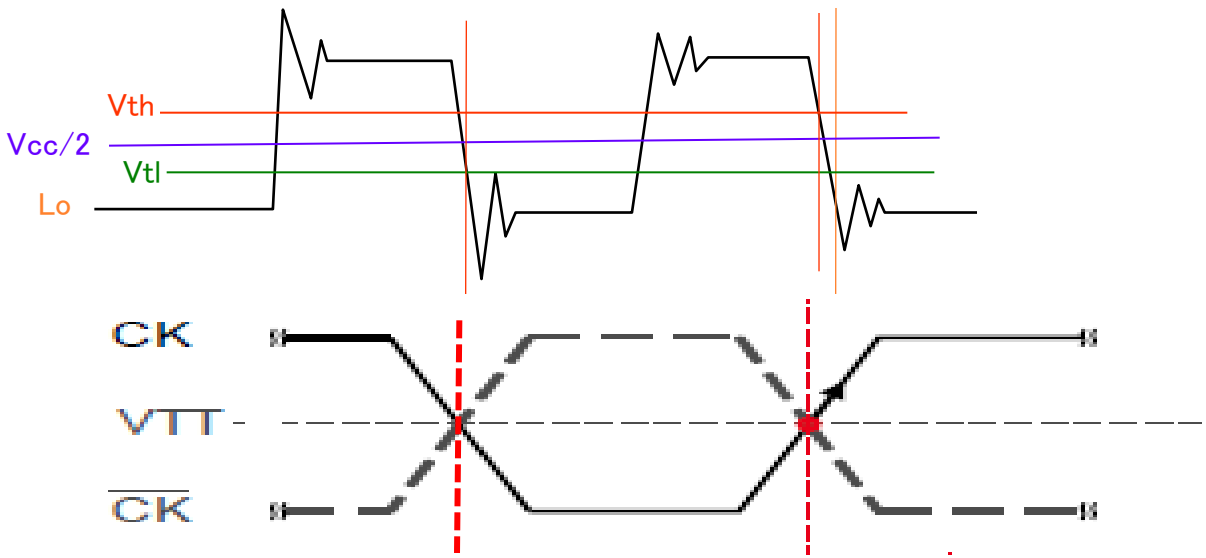
	DDR	DDR2	DDR3	DDR3L	DDR3U	DDR4
Vdd	2.5	1.8	1.5	1.35	1.25	1.2(IO) + 2.5(Core)
ODT（ohm）	N/A	50/75/150/OFF	20/30/40/60/120/OFF			34/40/48/60/80/120/240/ OFF
Diff Clock	Single	Diff	Diff			Diff
DQS	Single	Single/Diff	Diff			Diff
Driver Z (ohm)	Full/Half	Full/Reduce	34/40			34/40/48
ADD/CMD Topology	T	T	Fly-by			Fly-by
Memory Size	~64Mbit	~4GBit	0.5~8GBit			2/4/8/16GBit
DQ Prefetch	2	4	8			8X2 (4x4)
Clock(MHz)	100~200	200~400	400~1066			800~1600
Data Speed (Mbps)	200~400	400~800	800~2133			1600~3200
Bus Width (Max)	4/8/16/32	4/8/16	4/8/16			4/8/16

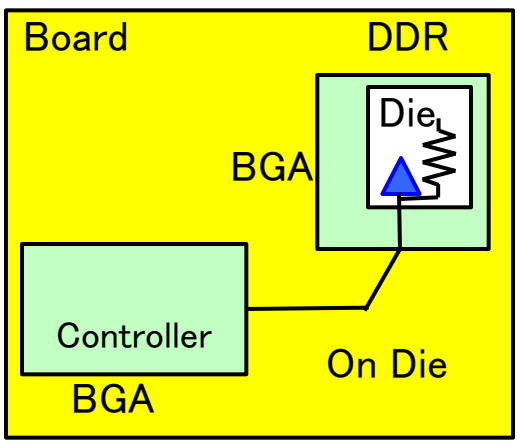
New Feature of DDR2

- ODT (DQ/DQn)
  - 50/75/150/OFF
  - Terminate to Vtt (Vdd/2)
- Output Characteristics
  - Full Strength/Reduced Strength
- Diff Clock/ Diff DQ



On Board Termination

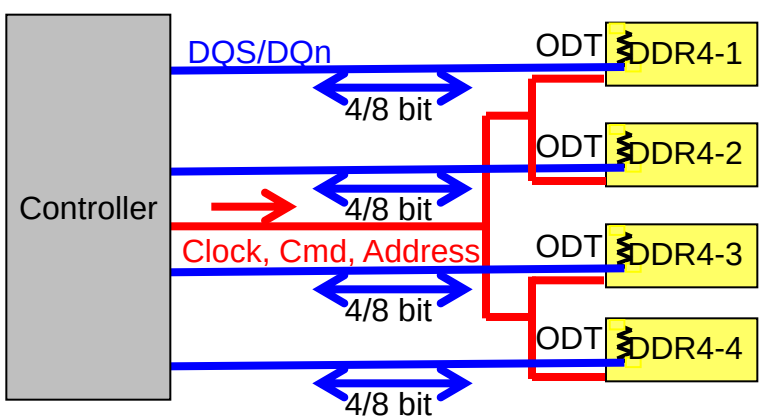




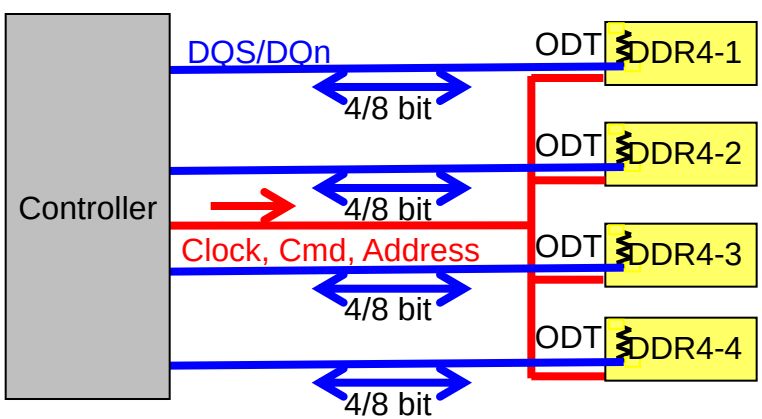
On Die Termination

DDR2

- Topology (Clock/Add/CMD/CTRL)
  - Equal Delay
  - Terminate to Vtt (Vdd/2)



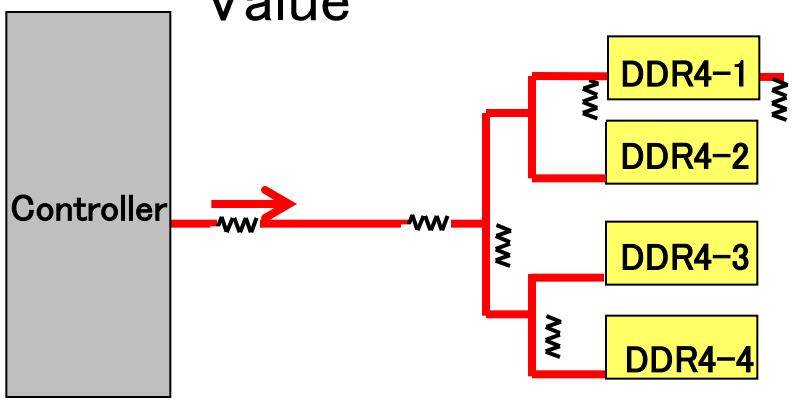
2 x 2 Branch

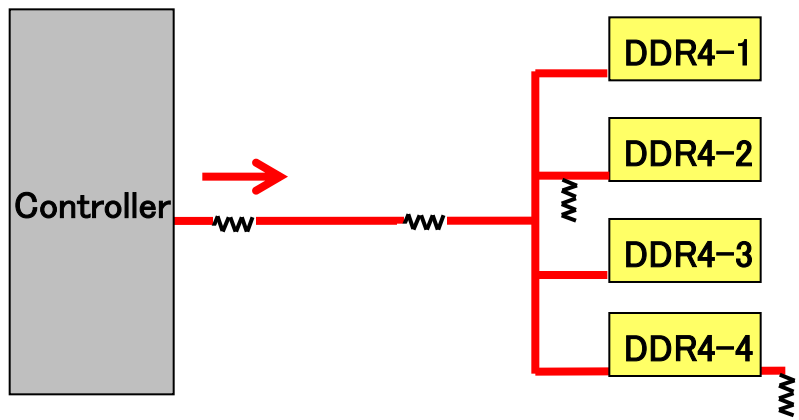


4 Branch

DDR2 Simulation

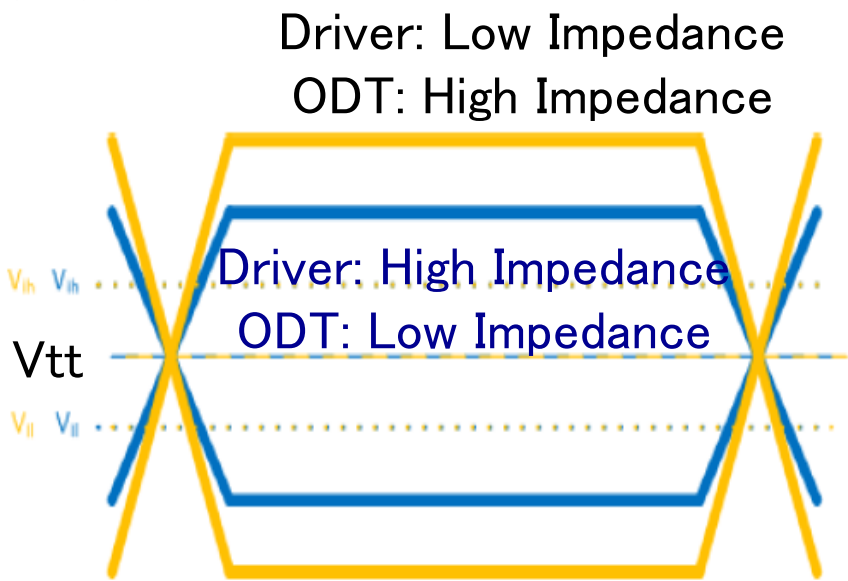
- Select best combination Driver and Receiver (ODT)
  - Full Strength/Reduced Strength ↔ 50/75/150 ohm
    - 6 Combinations
- Topology (Clock/Add/CMD/CTRL)
  - Equal Delay
  - Termination
    - Place
    - Value





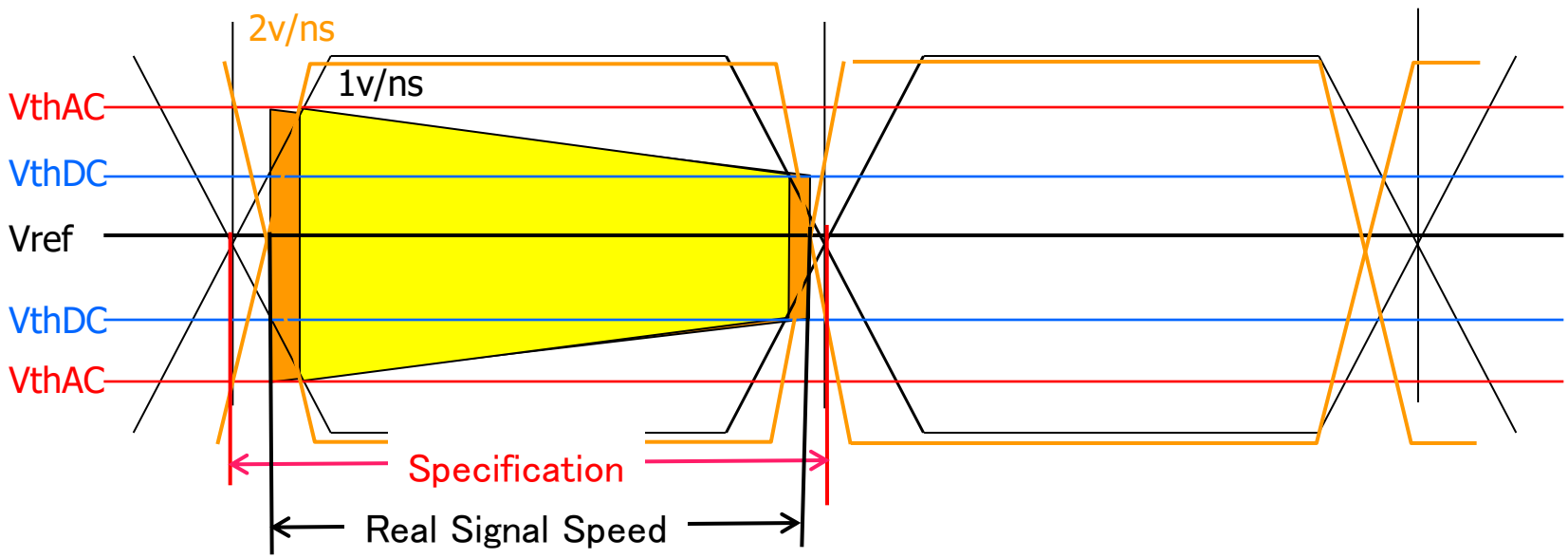
Combination Driver and Receiver

- Timing
  - Driver: Low/Receiver: High
    - High Signal Level. Fast, Shoot
    - High Power, Noisy (SSN, EMI)
  - Driver: Low/Receiver: High
    - High Signal Level. Fast, Shoot
- Driver: 34/40 ohm
- ODT: 50/75/150 ohm



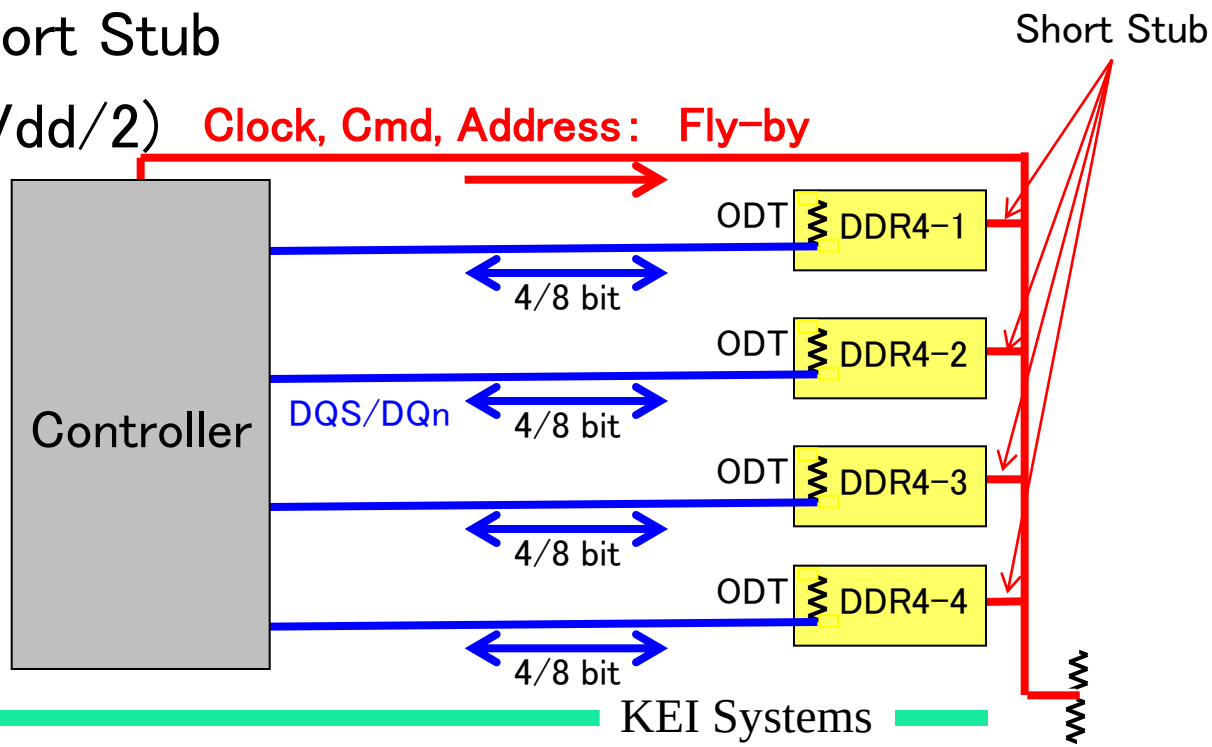
DDR2/DDR3 Timing Simulation

- Derating
  - **Specification Assign on Vref Timing**
  - **IC Works on Threshold Voltage**
  - **Necessary to adjust the timing on Vref to Threshold Voltage**
- Specification based on 1v/ns signal



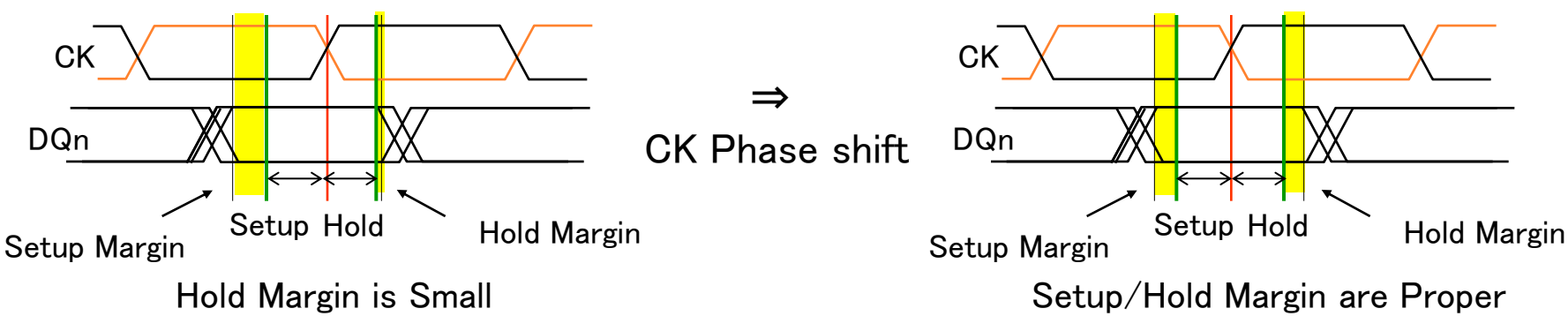
DDR3

- ODT
  - 20/30/40/60/120/OFF
- Output Characteristics
  - Full Strength/Reduced Strength
- Fly-by Topology (Clock/Add/CMD/CTRL)
  - Daisy-Cain with Short Stub
  - Terminate to Vtt (Vdd/2)



Simulation of DDR3 System

- Select best combination Driver and Receiver (ODT)
  - Full Strength/Reduced Strength – 20/30/40/60/120 ohm
    - 10 Combinations
- Fly-by
  - Effect of Stub Length
  - Leveraging
    - Read (Max. Timing Skew form 1st DDR to Last DDR) – Fly-by
    - Write (Option)



DDR4 Features

- Faster (Two times faster than DDR3)
  - DDR3: 400MHz ~ 800MHz, 933, 1066 MHz
  - DDR4: 800MHz ~ 1600MHz (2400, 2666)
  - 2.5V Core Logic
- Lower Power
  - More ODT Value
  - Partial Refresh (LPDDR technology)
  - 1.2V Interface
  - POD Termination
  - DBI (Data Bus Inversion)

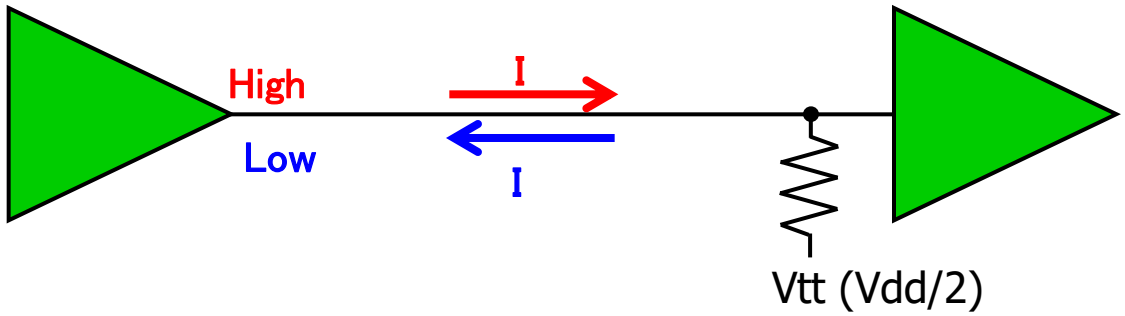
DDR4 Technology

- Same Technology of DDR3
  - ODT (34/40/48/60/80/120/240)
  - Fly by Wire
  - Output Impedance(34/40)
- New Feature
  - Multi-Purpose Register(MPR)

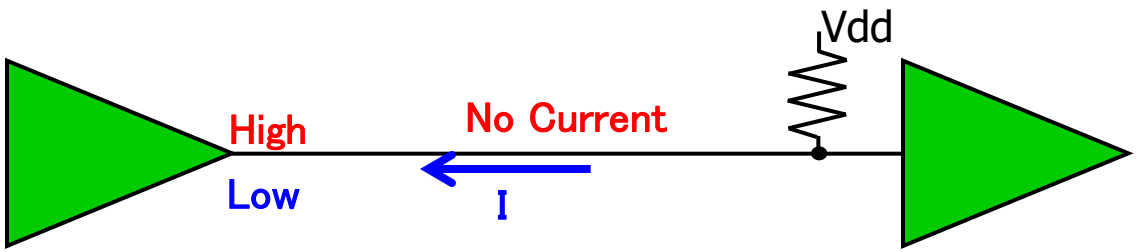
POD (Pseudo Open Drain) makes simulation difficult

POD

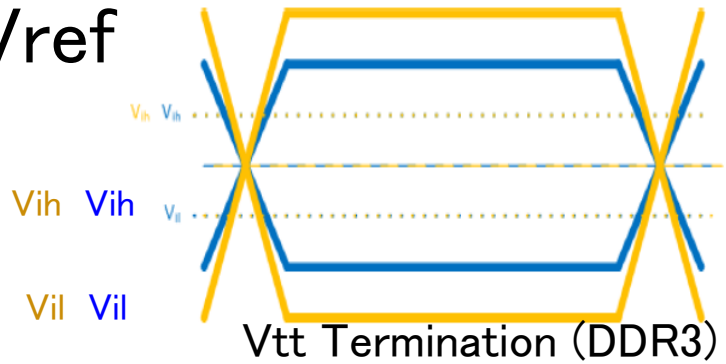
- ODT Termination Voltage: Vtt (DDR2/DDR3)

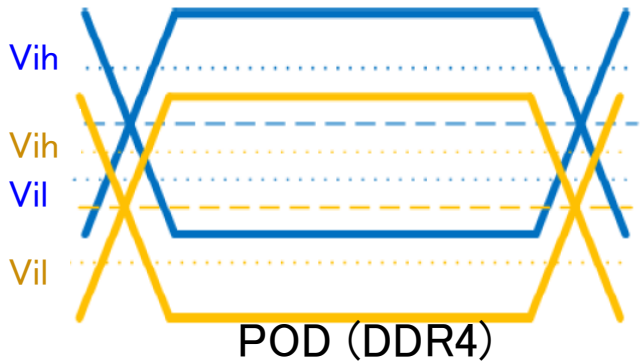


- POD (ODT Termination Voltage: Vdd(DDR4)



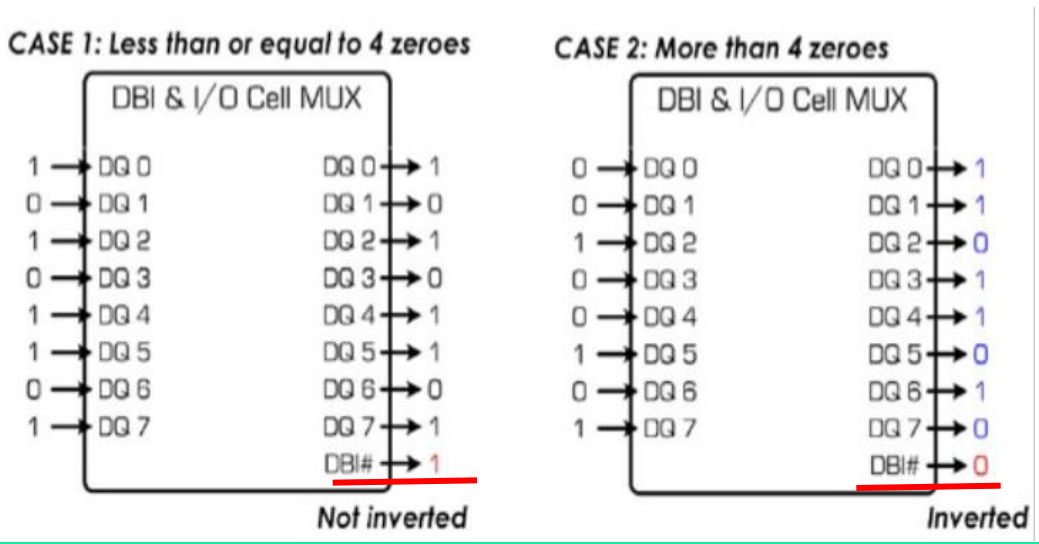
- POD Moves Vref





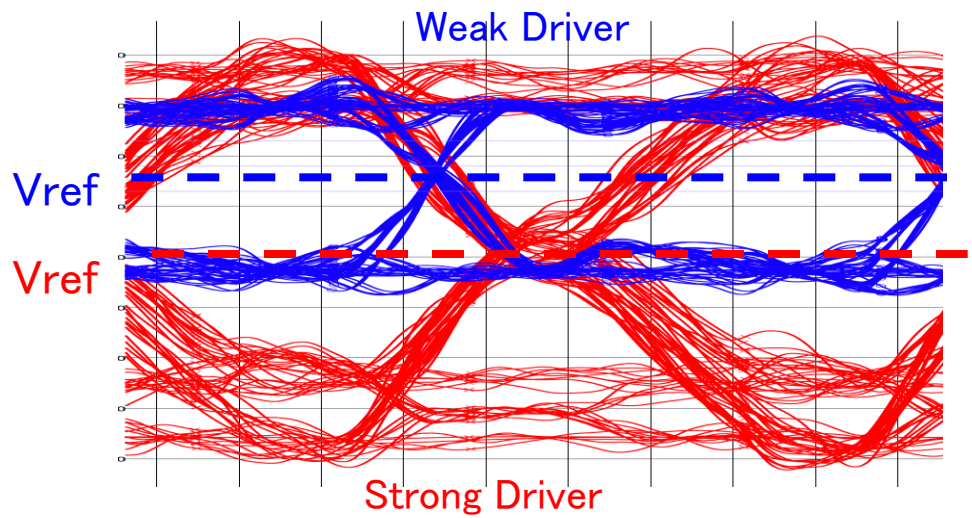
DBI (Data Bus Inversion)

- POD Termination
  - Low Level Data Drive High Current/High Level Data Drive no Current
  - When Low Level bits are Majority, Invert the Data
  - In Any Data, High bits are Majority
  - Simultaneous Switching: Less than 4 bits
    - Lower SSN



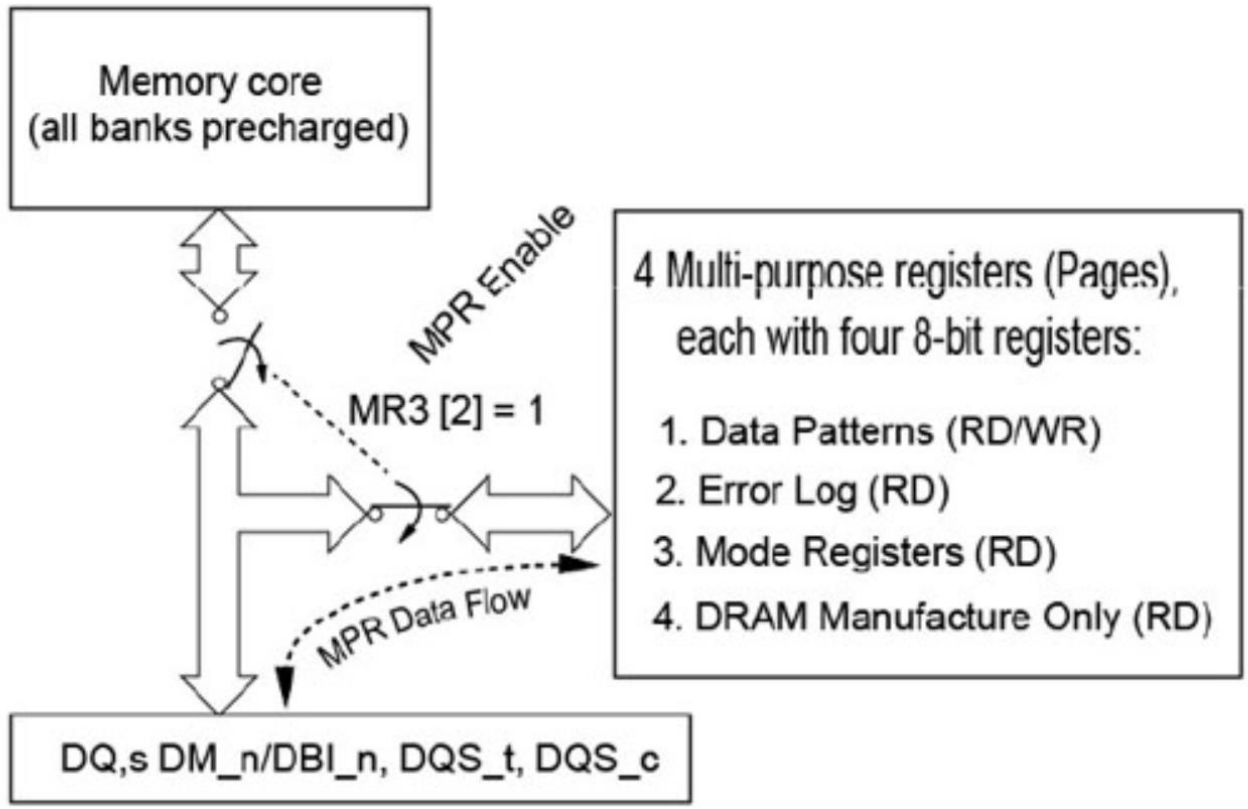
DDR4 System Design/Simulation

- DDR3 Methodology Can not be Used for DDR4 Design/Simulation
  - To Many combination of Driver-Receiver (18 Ways)
    - ODT: 34/40/48/60/120/240
    - Ron: 34/40/48
  - Vref Voltage is not fixed
- Vref, DQ Training
- ZQ Calibration



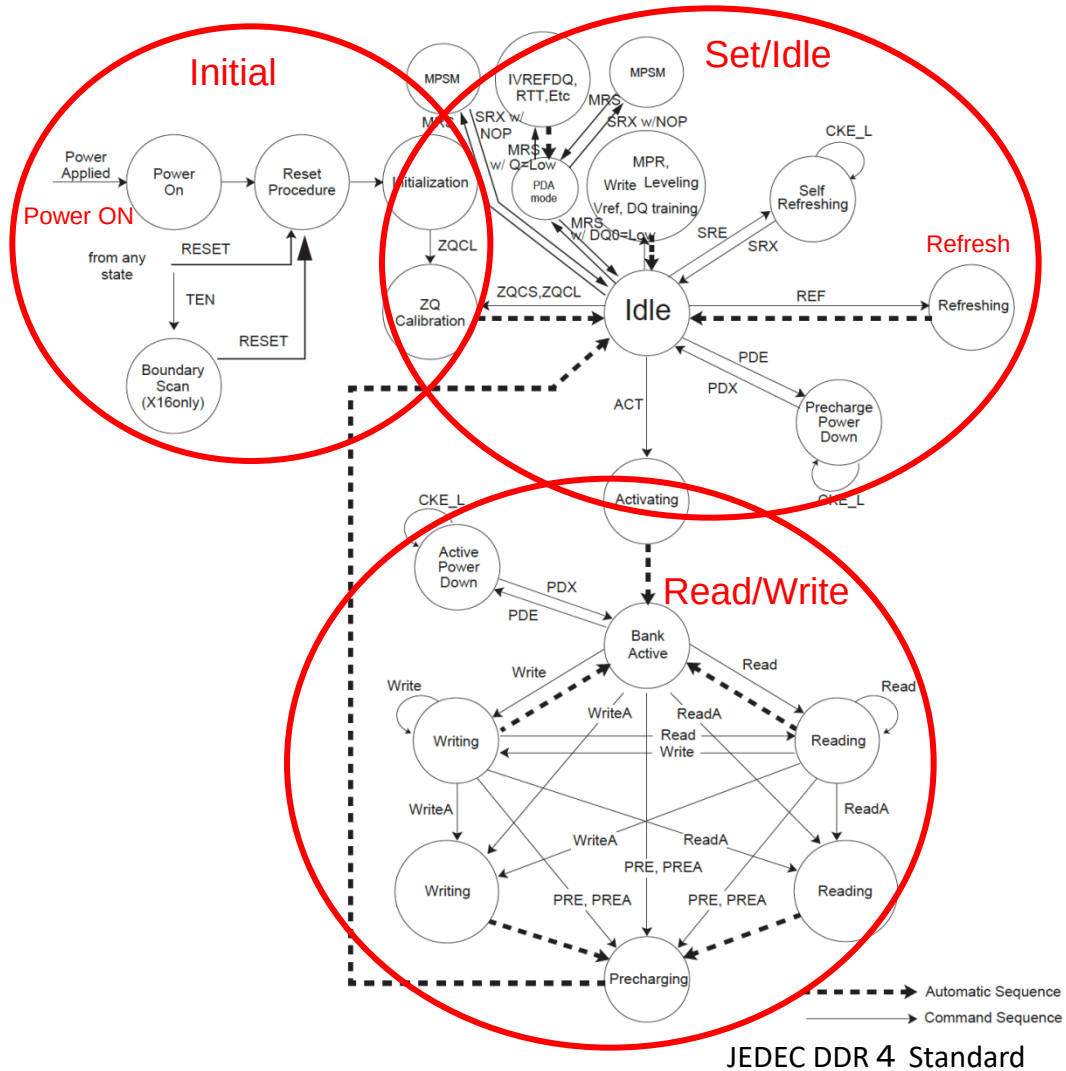
MPR (Multipurpose Register)

- Implement from DDR3
- Strongly Enhanced on DDR4
  - 4 4 Byte Registers
  - Training



DDR4 State Diagram

- Set/Idle State and Read/Write State
  - Initial
    - Initialize
    - ZQ Calibration
  - Set/Idle State
    - Write Leveling
    - ZQ Calibration
    - Vref, DQ Training
    - Refreshing
  - Read/Write State



JEDEC DDR 4 Standard

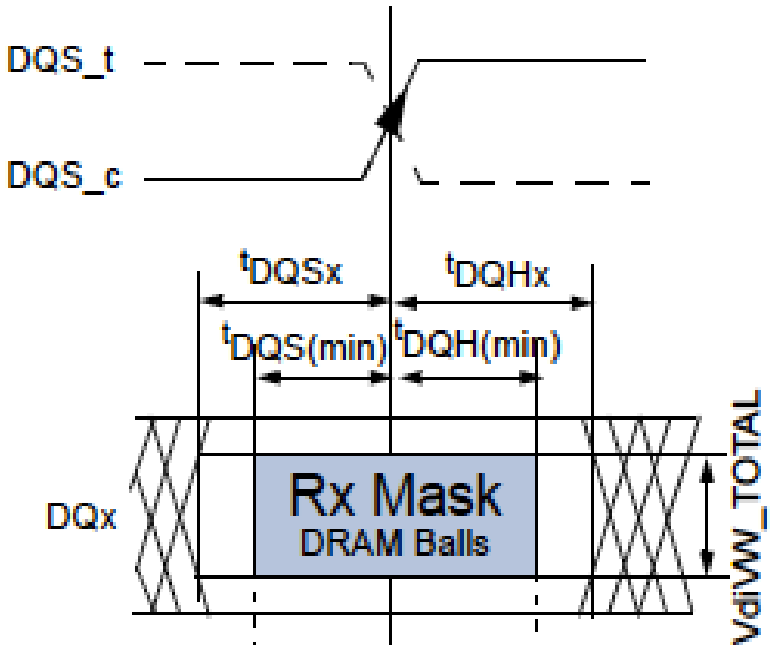
Adapt Eye Mask

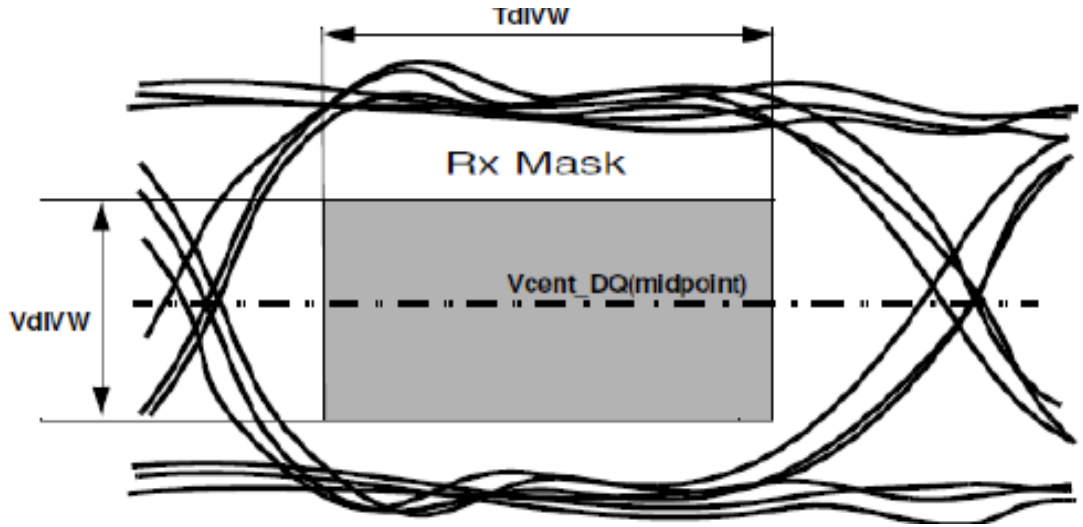
- Vref is Unstable
- Can't Fix Vref Based Timing Specification (DDR3)
  - No More Derating

DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	-
DQS_t,DQS_c to DQ Skew deterministic, per group, per access	tDQSQ	-	TBD	-
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	TBD
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	-
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD

DQS, DQS Data-in at DRAM ball

non Minimum Data-Eye / Maximum Rx Mask





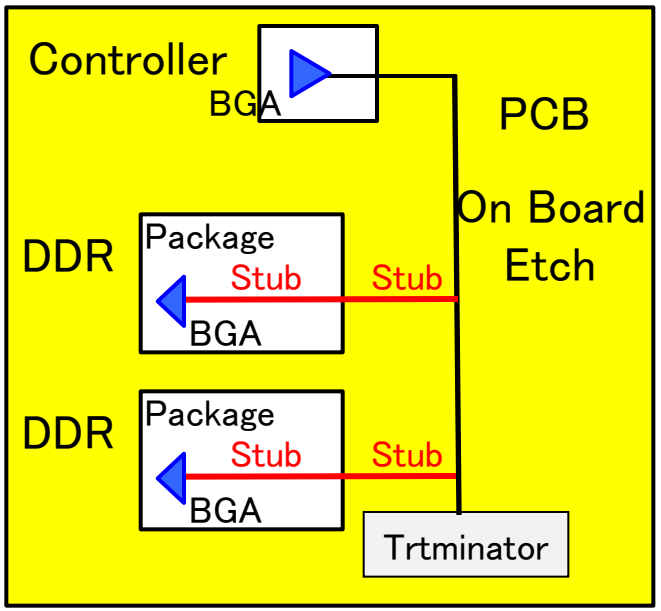
KEI Systems

DDR4 Simulation is very difficult

- Timing Analysis for Training
  - ZQ Calibration
  - Vref Training
  - Write Leveling
- SSN becomes more important
  - Lower voltage (1.2V)
  - Faster signal (dv/dt)
- X'talk
  - Faster signal (dv/dt)
- Package Model
  - Signal skew of In Package connection
  - In package X'talk (Bigger than on board connection)
  - Stub for Fly-by

IBIS Model for DDR4 Simulation

- Power Aware (IBIS 5.0)
- Vref Training/Write Leveling
  - Eye Mask



- Overclock
- Support DQ Training
  - How to determine best Driver-Receiver simulation model
- Fly-by Support
  - In-Package Stub

DDR5

- JEDEC Already working DDR5 Specification
  - Focus in 2018
    - Products in 2020?
  - x2 Faster than DDR4
  - DFE (Decision Feedback Equalizer)
    - Reduce ISI
  - More Training
  - Bigger Memory size
  - Power Reduce Technology
  - Analog Filter? (to reduce ISI jitter)
- Hard to Simulate

Conclusion

- DDR2 System Simulation
  - ADD/CMD/CTRL Topology
  - Combination of Driver/ODT
  - Sign-off Analysis
- DDR3 System Simulation
  - ADD/CMD/CTRL Fly-by Topology
  - Combination of Driver/ODT
  - Sign-off Analysis
- DDR4 System Simulation
  - ADD/CMD/CTRL Fly-by Topology (in Package Etch)
  - Combination of Driver/ODT (Too many combination to Simulate)
  - Can't execute Sign-off Analysis (Can't follow Training Result)
  - Power aware/Over Clock
- DDR5 System Simulation ?
  - More Intelligent I/F specification (More training functions)
  - Analog Filter Circuit? (IBIS AMI?)