IBIS Open Forum Minutes

Meeting Date: **November 17, 2017**
Meeting Location: **Tokyo, Japan**

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Yi Chuan Technology	Wei Ming Lu
Zhaoxin	Liam Li, Eddrick Wang
Zhejiang Uniview Technologies	Busen Cai, Jilun Fang

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
December 1, 2017	624 999 876	IBISfriday11

For teleconference dial-in information, use the password at the following website:

http://tinyurl.com/zeulerr

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Asian IBIS Summit took place on Friday, November 17, 2017 at the Akihabara UDX building in Tokyo. About 108 people representing 65 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/nov17c/

Mike LaBonte began with a welcome address from the IBIS Open Forum, in which he thanked JEITA for hosting the IBIS summit and for their work supporting IBIS in general. Mike said IBIS remains the most popular format for describing digital buffers, and most digital electronic devices today are designed using IBIS.

Mike also thanked the sponsors ANSYS, Cadence Design Systems, Cybernet Systems, Keysight Technologies, Ricoh, Toshiba Corporation, and Zuken. He said minutes of the summit would be posted and officially opened the meeting.

Mitsuharu Umekawa gave a welcome address from JEITA, noting that the morning workshop was arranged by the JEITA EDA Model Specialty Committee, and the topic was power aware IBIS simulation.

IBIS UPDATE

Mike LaBonte (SiSoft, USA)

Mike LaBonte detailed the activities of the IBIS Open Forum over the past year. He showed a possible timeline for the passage of IBIS 7.0, as well as the status of all current BIRDs that may or may not be part of IBIS 7.0. Mike gave a brief summary of the changes in three BIRDs likely to become part of IBIS 7.0.

Further explanation of BIRD 147 was requested. Mike gave some of the history of BIRD 147, saying that it originally was a more comprehensive proposal, including the BCI file to describe the protocol for communication between buffers. The accepted BIRD does not specify the protocol, leaving model makers to define the contents of the files themselves. It was noted that this posed a challenge for model portability across vendors. Mike said that there was general agreement that protocol descriptions could be submitted and posted on the IBIS website informally, and that this approach should provide for faster adoption of protocols than might be possible if the protocols would have to be described in the IBIS specification itself. A question was asked about what applications need a back channel interface. Mike noted that PCIe was an example.

Shinichi Maeda noted that DDR4 uses training to decide the Vref level. He asked if BCI is available for traditional IBIS too. Mike noted that BCI is an IBIS-AMI protocol and the RX algorithmic model controls the process. A question was asked about IBIS support for DDR4 single-ended equalization. Mike said that although IBIS does not explicitly support single-ended IBIS-AMI, it does not strictly limit IBIS-AMI to differential signaling, and some tools have been

using IBIS-AMI to support DDR4.

WHAT'S EXPECTED FOR IBIS-AMI FROM THE PERSPECTIVE OF END-USER SUPPORT
Masao Nakane (Xilinx, Japan)

Masao Nakane listed user expectations for IBIS-AMI models. One of these is result matching between different simulators and between simulators and measurement, but there are often problems in that area. Often, the cause of the trouble is not necessarily in the algorithmic models, but in the S-parameters that form the channel. Lack of causality was a common issue. One way to determine if that is the cause of mismatch between simulators is to capture and compare the impulse responses sent by the simulators to the first IBIS-AMI model, which often differ. He said a unified methodology is needed for channel characterization. Mike LaBonte commented that sometimes the algorithmic models were found to be improperly sensitive to samples per bit and block size settings, and that the different defaults for those between tools would sometimes cause differences.

DDR SYSTEM SIMULATION: WHAT ISSUE TO SIMULATE
Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda gave an overview of DDR technologies from DDR through DDR4. He described difficulties encountered in producing good package models for DDR4, as well as factors that could make DDR5 difficult to simulate. One of the DDR4 issues was the large number of variable parameters, leading to a large number of simulations that would need to be performed.

INVESTIGATION OF THE PACKAGE CROSSTALK NOISE TO DDR4-IF SIGNAL BY IBIS [DEFINE PACKAGE MODEL]
Akiko Tsukada, Masaki Kirinaka (Fujitsu Interconnect Technologies Limited, Japan)
[Presented by Akiko Tsukada (Fujitsu Interconnect Technologies Limited, Japan)]

Akiko Tsukada showed the results of extensive crosstalk simulation across a variety of cases. She said the ability to design out crosstalk on boards has improved, leaving package crosstalk as a more significant factor. The [Define Package Model] matrix formats were explained, as well as equivalent IBIS-ISS circuits that can be used. In crosstalk testing the victim net is held static while a stimulus pattern is applied to the aggressors, allowing crosstalk to be measured in the voltage domain. The timing skew effect of crosstalk on active signals can also be measured. It was found that even mode aggressors had more crosstalk-induced skew effect than odd mode aggressors, and that board coupling produced less skew than package coupling.

A question was asked about how the aggressor signal location is selected for a victim line. Tadashi Arai commented that crosstalk skew is dynamically changed by signals. So it's relatively averaged. Generally, IC vendors factor in skew induced by IC packages and budgets as part of jitter in advance.

ON DIE DE-CAP MODELING PROPOSAL

Kazuki Murata (Ricoh Company, Japan)

Kazuki Murata noted that the LSI Package Board (LPB) format is an IEEE standard format produced by the JEITA Semiconductor Design Technology Subcommittee. The subcommittee had surveyed people involved in LSI design, and found that while on-die decoupling is considered very important, availability of models including that decoupling was poor. Measurements of decoupling do not all use the same circuit topology, and that should be standardized. IBIS offers no specific support for modeling decoupling. He showed how [Series Model] could be used to define capacitance between power and ground pins. He felt that that was not a good choice for describing a power delivery network model, however, due to topology differences. Alternatively, [External Model] and [External Circuit] could be used, but these were considered too complex. The LPB modeling working group is proposing a new IBIS syntax to describe on-die decoupling capacitors. A forum on the topic will be held March 9, 2018.

Mike LaBonte asked if the IBIS checker passes the series De-cap configuration. Kazuki responded yes. A comment was made that from the IC design house side, they don't feel comfortable revealing the on-die de-cap in IBIS format because it may reveal internal system design.

IBIS INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE

Michael Mirmak (Intel Corporation, USA)
[Presented by Mike LaBonte (SiSoft, USA)]

Mike LaBonte presented on behalf of Michael Mirmak. The concepts found in BIRD189.x were summarized. The new format is an improvement over existing IBIS [Define Package Model] in several ways, allowing for both cascaded model sections as well as coupling in any combination. The Touchstone format and the ability to separately model buffer to pad and pad to pin connections would be helpful for the high speed signals used today. The addition of die pads for rails allowed for circuit topologies suitable for modeling the power and ground rails in chips.

A question was asked about the modeling extensions not covered by the presentation. Mike said that bus labels had not been covered in any detail. He added that while BIRD189 was not designed for modules or stacked die, extensions to support that and multi-chip modules were planned.

Mitsuharu Umekawa commented that it's good to have freedom for inter-connect representation. Besides, factoring in end-user scenarios of simulations may be important to have this new standard become popular.

CLOSING REMARKS

Mike LaBonte closed the meeting, thanking JEITA, the sponsors, the speakers, and all who attended. Mitsuharu Umekawa thanked the audience, encouraging support for the LPB effort.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held December 1, 2017. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 15, 2017.

The Asian IBIS Summit in Tokyo will be held November 17, 2017. No teleconference will be available for the Summit meeting.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
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To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	October 27, 2017	November 13, 2017	November 15, 2017	November 17, 2017
ANSYS	User	Active	X	-	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	X	X	X
Cisco Systems	User	Inactive	-	X	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	X	-	-
GLOBALFOUNDRIES	Producer	Inactive	X	-	-	-
Huawei Technologies	Producer	Inactive	-	X	-	-
IBM	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	X	-	-	-
Intel Corp.	Producer	Active	X	-	X	-
IO Methodology	User	Active	X	X	X	-
Keysight Technologies	User	Active	X	-	X	X
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Inactive	X	X	-	-
Micron Technology	Producer	Inactive	X	-	-	X
NXP	Producer	Inactive	-	-	-	-
Qualcomm	Producer	Inactive	-	-	X	-
Raytheon	User	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	X
Synopsys	User	Inactive	X	X	-	-
Teraspeed Labs	General Interest	Inactive	X	-	-	-
Xilinx	Producer	Inactive	-	-	-	X
ZTE Corp.	User	Inactive	-	X	-	-
Zuken	User	Inactive	-	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.