**AGENDA - Asian IBIS Summit (Tokyo)**

**Friday, November 17, 2017**

Akihabra UDX

Tokyo, Japan

Room: **4F UDX4F**

Sponsors: **Japan Electronics and Information Technology Industries Association (JEITA)**

**IBIS Open Forum**

**ANSYS**

**Cadence Design Systems**

**Cybernet Systems**

**Keysight Technologies**

**Ricoh**

**Toshiba Corporation**

**Zuken, Inc.**

*(Order and times subject to change)*

13:30 **SIGN IN**

13:35 **MEETING** **WELCOME**

* Mitsuharu UMEKAWA (Keysight Technologies, Japan)  
   Chair, JEITA EDA Model Subcommittee
* Mike LaBONTE (SiSoft, USA)  
   Chair, IBIS Open Forum

13:45 **IBIS Update**

Mike LaBONTE (SiSoft, USA)

14:10 **What’s Expected for IBIS-AMI from the Perspective of End-User Support**

Masao NAKANE (Xilinx, Japan)

14:40 **DDR System Simulations: What Issue to Simulate**

Shinichi MAEDA (KEI Systems, Japan)

15:10 **BREAK**

* Reconvene at 15:30

15:30 **Investigation of the Package Crosstalk Noise to DDR4-IF Signal by IBIS [Define Package Model]**

Akiko TSUKADA, Masaki KIRINAKA (Fujitsu Interconnect Technologies Limited, Japan)

*[Presented by Akiko TSUKADA (Fujitsu Interconnect Technologies Limited, Japan)]*

16:15 **On die De-cap Modeling Proposal**

Kazuki MURATA (Ricoh Company, Japan)

16:40 **Interconnect Modeling Update Using IBIS-ISS and Touchstone**

Michael MIRMAK (Intel Corporation, USA)

*[Presented by Mike LaBONTE (SiSoft, USA)]*

17:15 **CONCLUDING ITEMS**

17:30 **END OF IBIS SUMMIT MEETING**

* ****Thank you for your participation