

# Interconnect Modeling Update Using IBIS-ISS and Touchstone



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# Agenda

- ❑ History
- ❑ The need for improved interconnect support
- ❑ Principles of the Interconnect Proposal
  - Structure
  - Terminals, Models and Sets, and Groups (new)
  - New Keywords
- ❑ An example explained
- ❑ New or changed features
- ❑ Summary

# History

- ❑ Interconnect Task Group resumed meeting in early 2014
  - Received draft BIRD from Walter Katz (SiSoft) to support IBIS-ISS packages within IBIS
- ❑ BIRD189.x uploaded (awaiting approval)
  - <http://www.ibis.org/birds/>
  - 41 pages with examples
  - Still resolving some issues
  - Comments welcome
- ❑ Intended for IBIS Version 7.0
- ❑ Brief overview with some key points is given here

# Why Update Interconnect Modeling?

- ❑ Improve package models with IBIS-ISS (an HSPICE subset) and Touchstone support
- ❑ Package modeling in IBIS stable since 2000
  - [Pin], [Package], [Package Model]
  - [Alternate Package Models] selector added
  - Limited support of loss, crosstalk and/or partitioning
- ❑ EBD (Electrical Board Description) for boards; No coupling and limited package model application
- ❑ IBIS, IBIS-ISS, Touchstone 2.0 and ICM are separate specifications
  - Limited interaction between them for package modeling
  - ICM (Interconnect Model) never adopted by industry

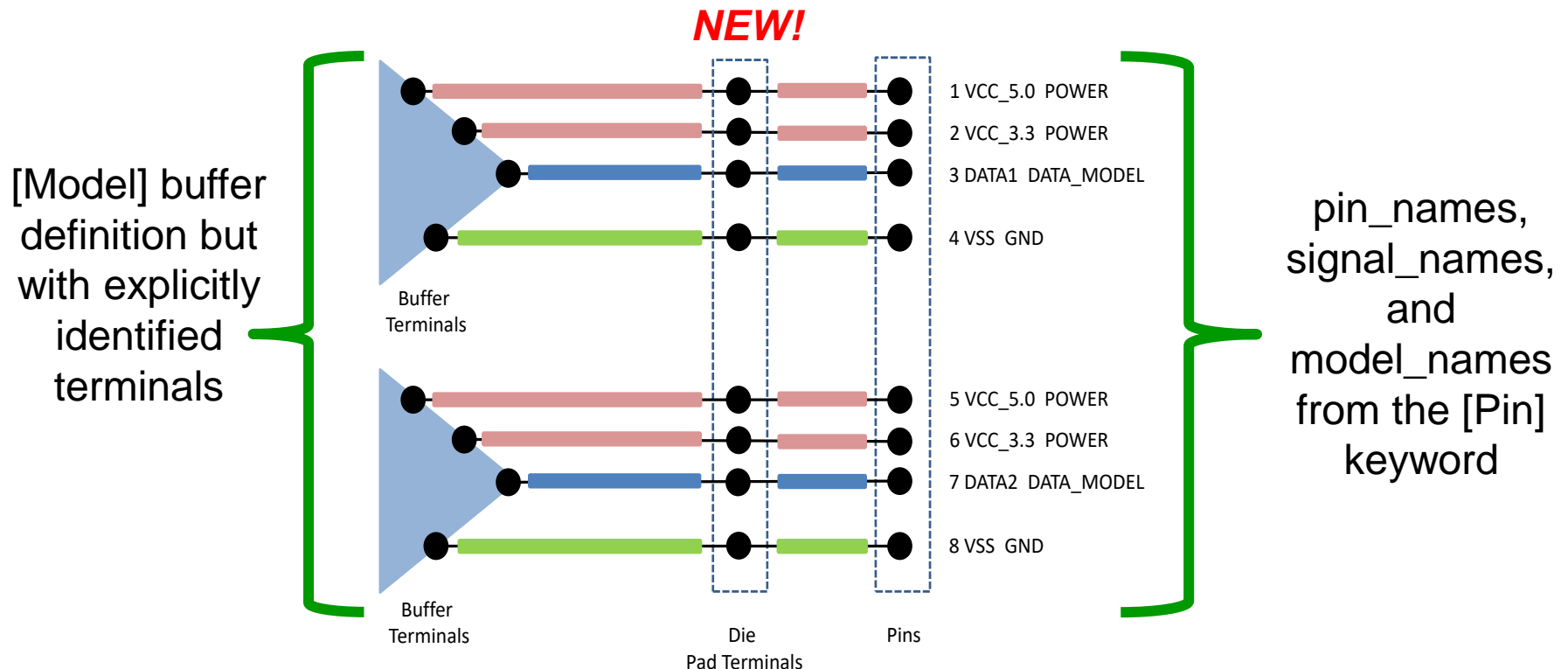
# Features of the Interconnect Proposal

## ❑ Supports...

- IBIS-ISS and Touchstone models (common in industry)
- Both I/O and supply (POWER and GND) connections
- (New) optional Die pad interface between Pins and Buffers
- I/O pin\_names as terminal qualifiers
  - *May have optional Aggressor\_Only designation*
- POWER and GND terminal qualifiers by pin\_name, pad\_name, signal\_name or [Pin Mapping] bus\_label for rail connections with direct or combined terminals
- Many other features not covered here

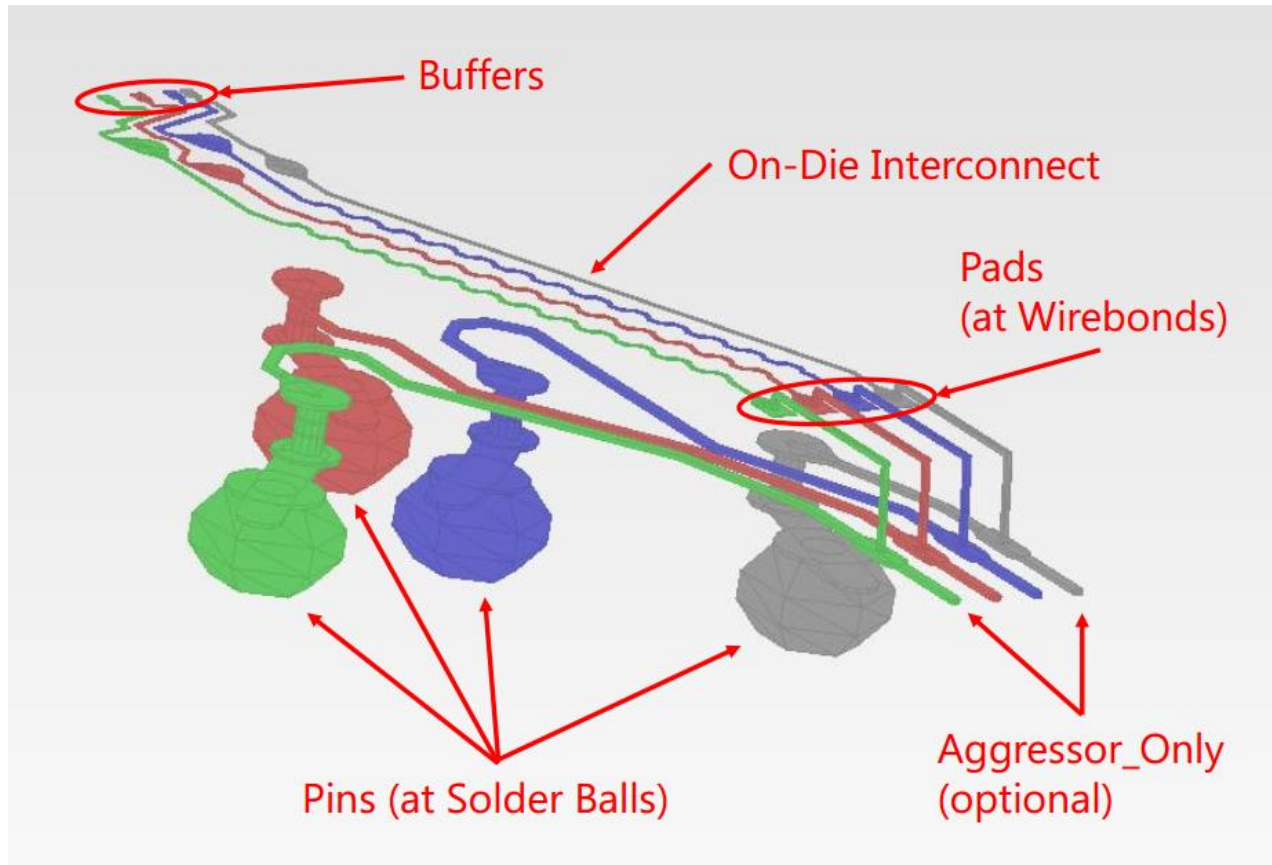
A few objectives for the  
Interconnect Modeling proposal

# Structure of the Interconnect Proposal



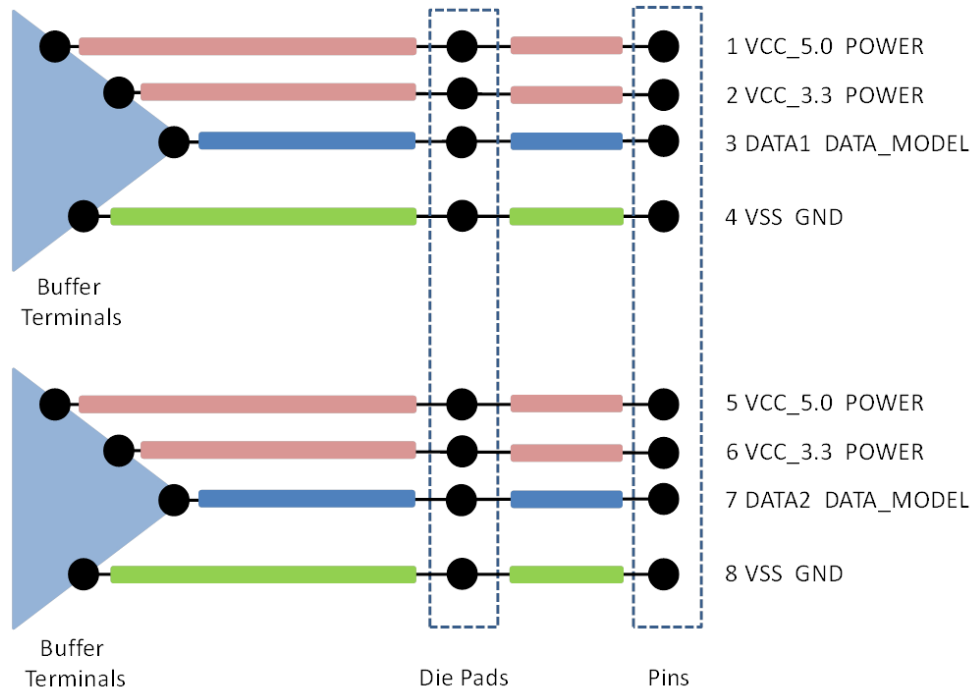
Introduces optional Die pad interface for terminals separate from Buffer and Pin interface terminals

# Relates to Physical Structures



One-to-one path connection; Die pad interface optional;  
Aggressor\_Only designation optional

# Terminals at Buffer, Die Pad and Pin Interfaces



## Original IBIS (4.0 and earlier)

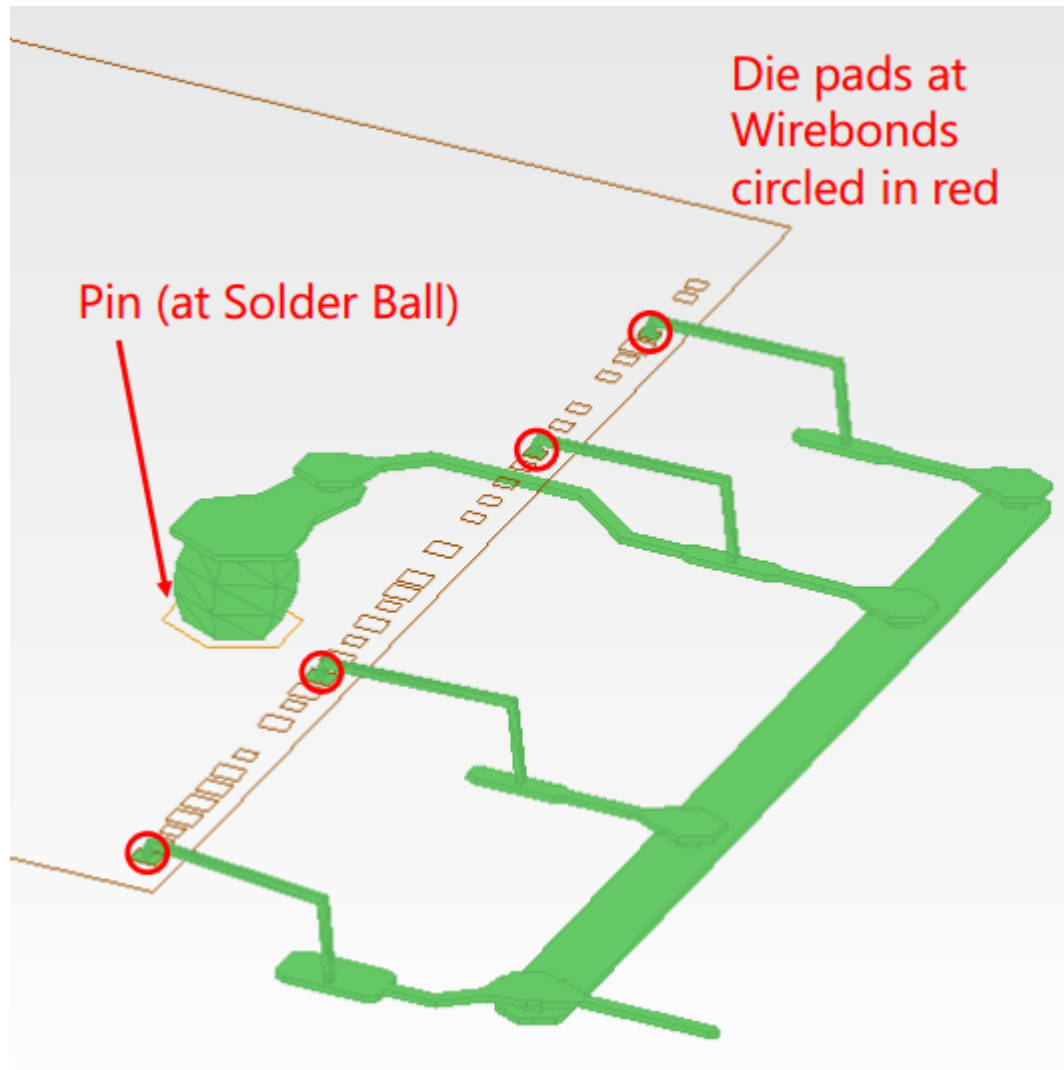
- Pins are explicit
- Buffer terminals implicit in [Model]
- Die pad terminals same as buffer terminals
- Packages defined connections between pins and buffers

## Current Proposal

- Die pad terminals are now explicit
- Buffer terminals are now explicit
- [Pin]s are.... still pins
- Separate interconnect definitions can be created between ...
  - Pin-to-Die pad terminals,
  - Die pad-to-Buffer terminals,
  - Pin-to-Buffer terminals (still) supported



# Physical Rails (Can be Merged)

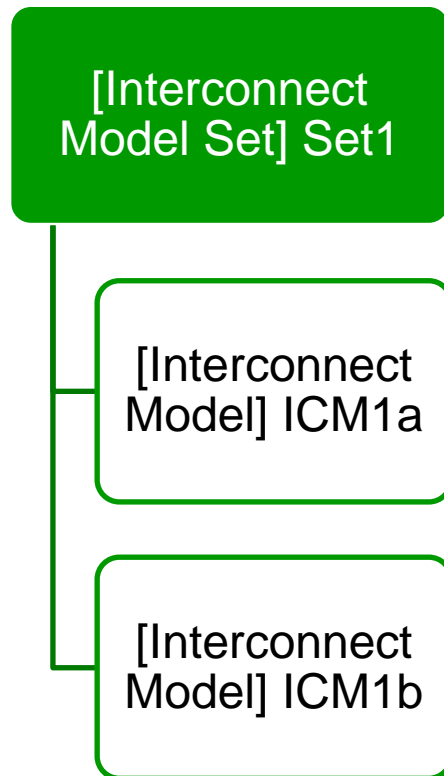


# New Keywords and Subparameters (Limited Discussion Here)

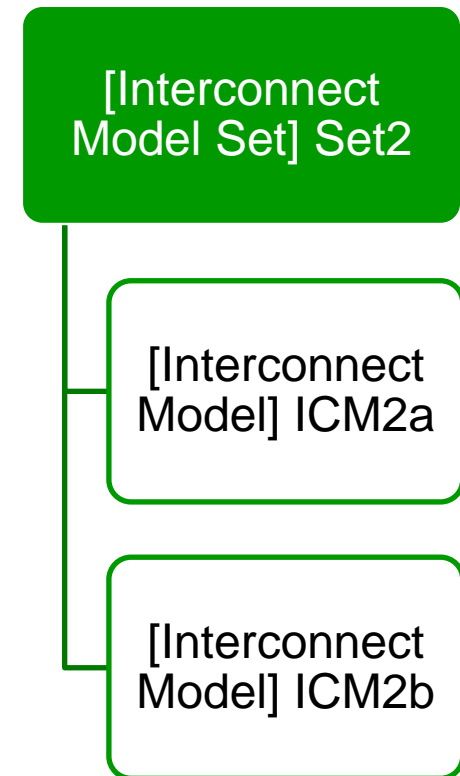
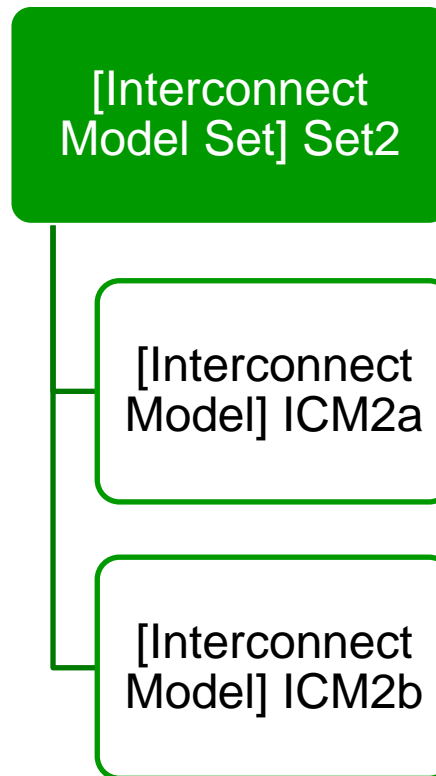
- ❑ [Bus Labels] | bus\_label
- ❑ [Die Supply Pads] | pad\_name, optional bus\_label
- ❑ [Interconnect Model]/[End Interconnect Model]
  - Unused\_port\_termination <Open | Ref.> | Unused port ref. Z
  - Param | parameter passing
  - File\_IBIS-ISS | names IBIS-ISS file
  - File\_TS, File\_TS0 | names Tstone file
  - Number\_of\_terminals=<value> | number of terminals
  - <terminal lines> | described later
- ❑ [Interconnect Model Set]/[End Interconnect Model Set]
- ❑ [Interconnect Model Set Group]/[End Interconnect Model Set Group] (New and changed from “Selector”)

# Interconnect Hierarchy

[Interconnect Model Group] Group 1



[Interconnect Model Group] Group 2



# [Interconnect Model Set]s

## [Interconnect Model Set Group]s (New)

- ❑ [Interconnect Model Set] <set\_name>
  - Encapsulates one or more Interconnect Models
- ❑ [Interconnect Model Set Group] <group\_name>
  - References one or more Interconnect Model Sets to be used together
  - Should be used to establish a complete path for selected buffers
  - <group\_name> helps in identify the buffers that are selected for simulation
- ❑ Some Example Groupings and Applications
  - Separate groups: one per interface (e.g., memory, network)
  - Separate groups for coupled vs. single-line simulations
  - Different sets for different power delivery network complexities
    - *POWER connected at single pin, single buffer terminal*
    - *POWER connected through multiple pins, rails to individual buffer terminals*

# [Interconnect Model]

- ❑ [Interconnect Model] <interconnect\_model\_name>
  - Connections between terminals with IBIS-ISS or Touchstone files
  - Terminal connection points at Buffer, Die pad, or Pin interfaces
  - Identifies rail or I/O terminals
  - Allows pin\_name, signal\_name, pad\_name, or bus\_label terminal qualifiers for rails (and pin\_name for I/O terminals)
  - Identifies whether a coupled signal is only an aggressor or also “experiences” coupling from other sources

How package and on-die electrical information  
is generated and delivered today

# <Terminal lines> Syntax


- ❑ All column entries on one line:

<Terminal\_number> <Terminal\_type>  
    <Terminal\_type\_qualifier> <Qualifier\_entry>  
    [Aggressor\_Only]

- ❑ <Terminal\_number> is IBIS-ISS node position or Touchstone port number
- ❑ Allowable <Terminal\_type> names and associations next

# Allowable <Terminal\_type> Associations

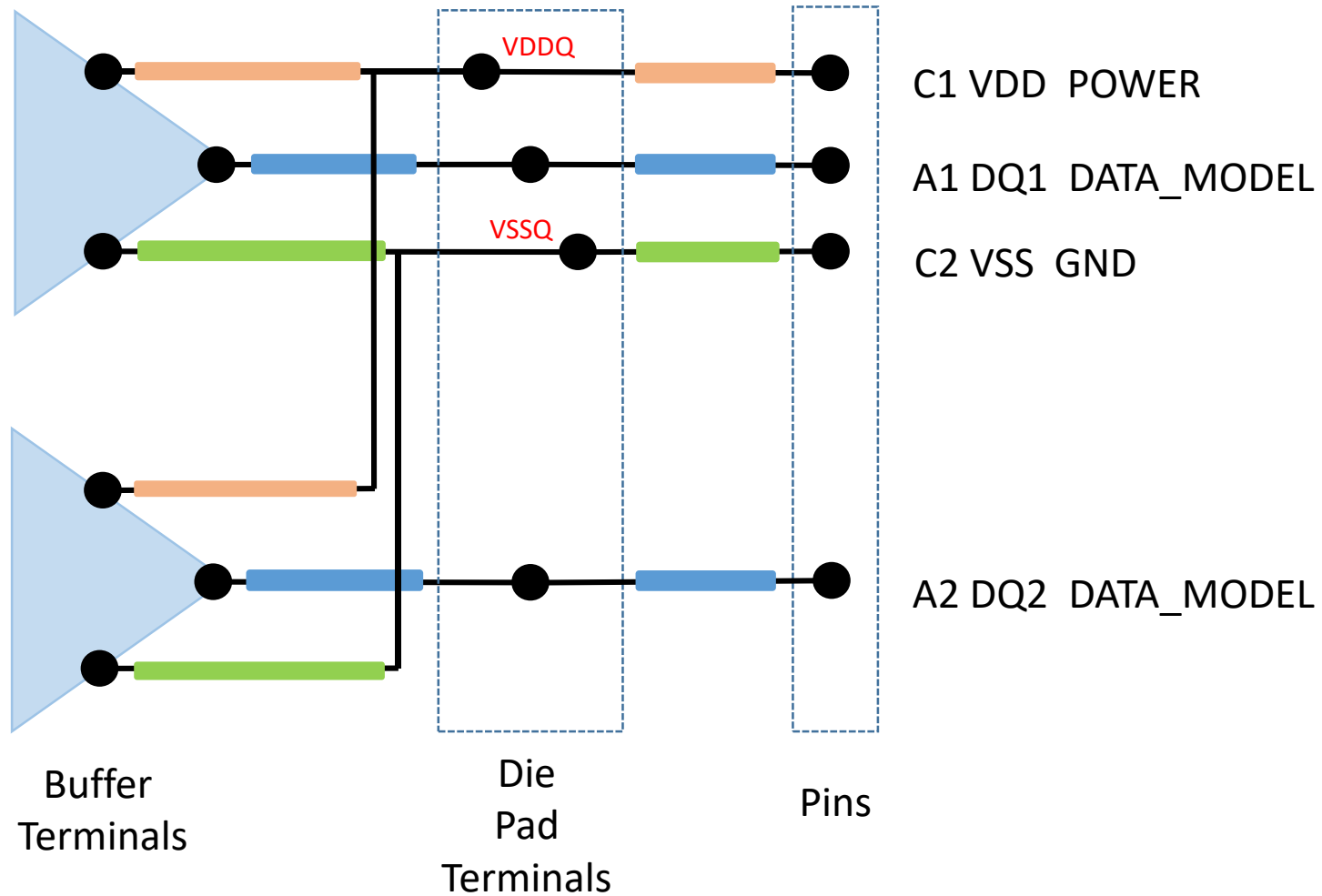
<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]



Terminal_type	Terminal_type_qualifier				Aggressor_Only
	pin_name	signal_name	bus_label	pad_name	
Pin_I/O	X				A
Pad_I/O	X				A
Buffer_I/O	X				A
Pin_Rail	Y	Y	Y		
Pad_Rail		Y	Y	Z	
Buffer_Rail		Y	Y		
Pullup_ref	X				
Pulldown_ref	X				
Power_clamp_ref	X				
Gnd_clamp_ref	X				
Ext_ref	X				

<Qualifier\_entry>: "X" I/O pin\_name; "Y," or "Z": POWER or GND name. Optional "A": "Aggressor\_Only"

# Example Showing Connections





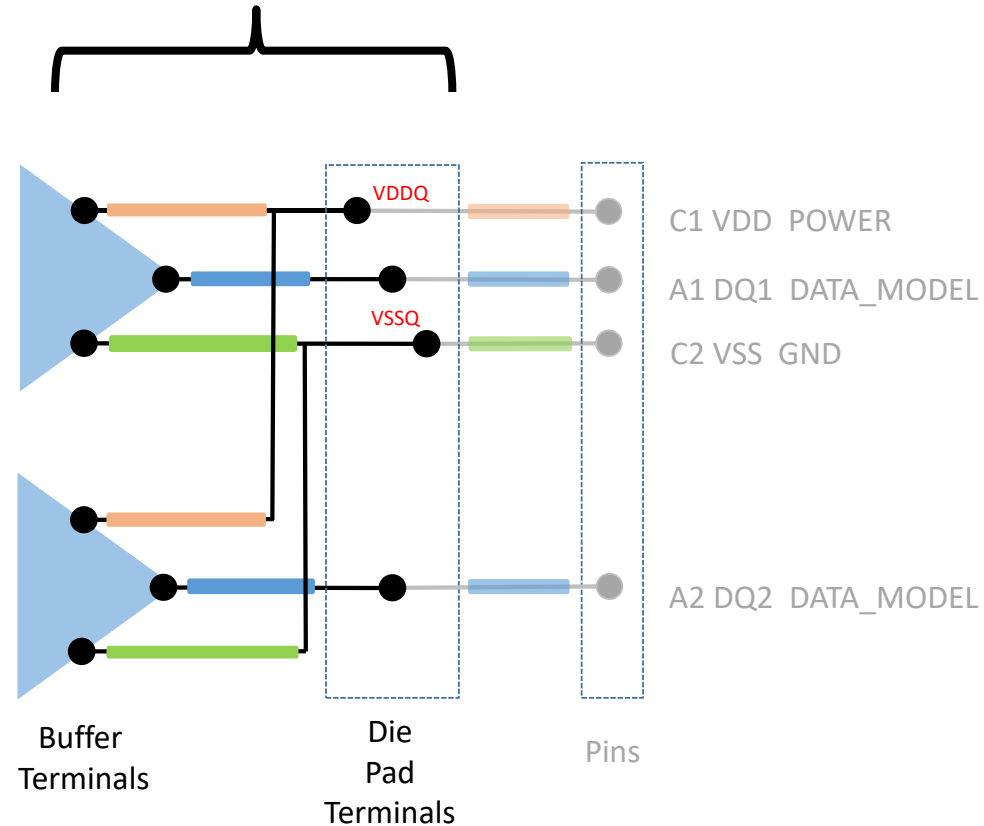
# [Die Supply Pads] for pad\_names Shown in Example

The [Die Supply Pads] keyword establishes pad\_name <Qualifier\_entries> for rails, and associates them with signal\_name (and optionally with bus\_label entries)

```
[Die Supply Pads] signal_name bus_label
| pad_name
VDDQ                VDD
VSSQ                VSS
```

# [Interconnect Model] for Buffer-to-Die Pad Side

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS      buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O          pin_name     A1 | DQ1 (DQ signal)
2  Pad_I/O          pin_name     A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref       pin_name     A1 | VDD (POWER connection)
4  Pulldown_ref     pin_name     A1 | VSS (GND connection)
5  Buffer_I/O       pin_name     A1 | DQ1 (DQ signal)
6  Pullup_ref       pin_name     A2 | VDD (POWER connection)
7  Pulldown_ref     pin_name     A2 | VSS (GND connection)
8  Buffer_I/O       pin_name     A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail         pad_name     VDDQ | VDD  POWER
10 Pad_Rail         pad_name     VSSQ | VSS  GND
|
[End Interconnect Model]
```



# [Interconnect Model] for Buffer-to-Die Pad Side (Expanded)

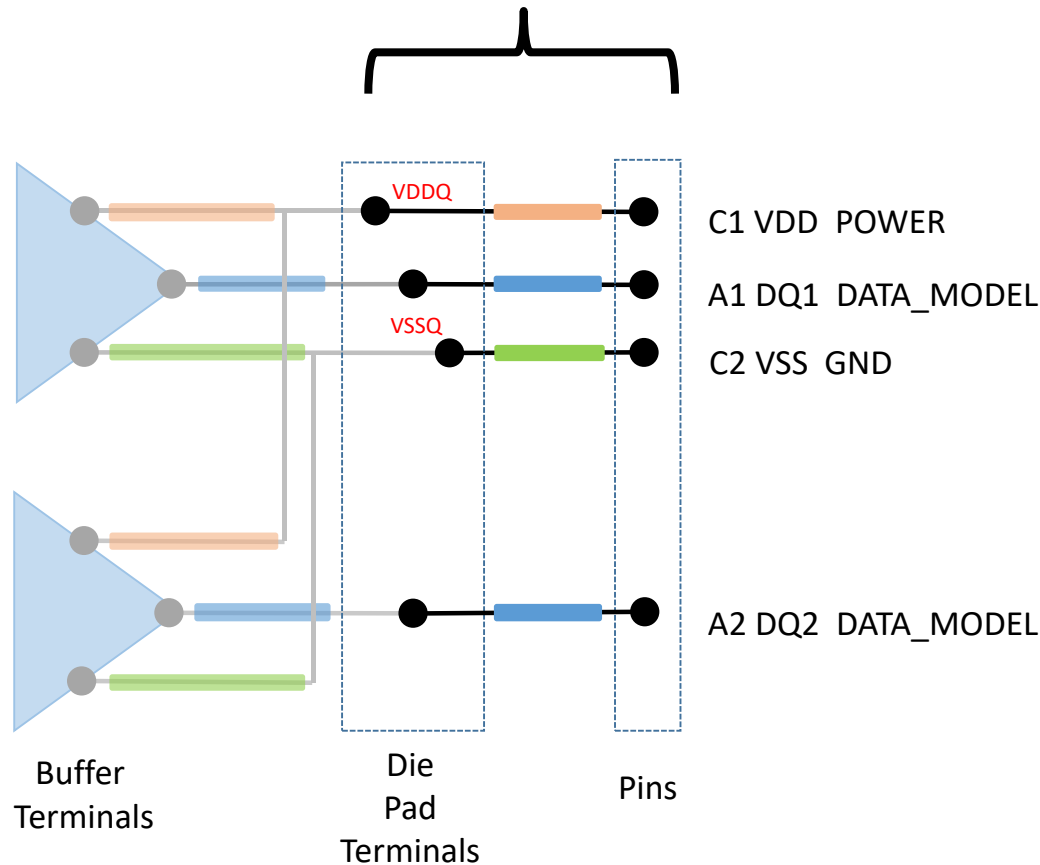
```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS          buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O             pin_name     A1 |  DQ1 (DQ signal)
2  Pad_I/O             pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref          pin_name     A1 |  VDD (POWER connection)
4  Pulldown_ref        pin_name     A1 |  VSS (GND connection)
5  Buffer_I/O          pin_name     A1 |  DQ1 (DQ signal)
6  Pullup_ref          pin_name     A2 |  VDD (POWER connection)
7  Pulldown_ref        pin_name     A2 |  VSS (GND connection)
8  Buffer_I/O          pin_name     A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail            pad_name     VDDQ |  VDD  POWER
10 Pad_Rail            pad_name     VSSQ |  VSS  GND
|
[End Interconnect Model]
```

[Interconnect Model]

File and subcircuit

<Terminal lines> for  
connecting the  
subcircuit nodes (by  
position) to the  
interconnect  
structure

# [Interconnect Model] for Die Pad-to-Pin Side



```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS          pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail     signal_name    VDD | VDD (POWER connection)
4  Pin_Rail     signal_name    VSS | VSS (GND connection)
5  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail     pad_name      VDDQ | pad_name with VDD
8  Pad_Rail     pad_name      VSSQ | pad_name with VSS
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```

# [Interconnect Model] for Die Pad-to-Pin Side (Expanded)

[Interconnect Model]

File and subcircuit

<Terminal lines> for  
connecting the  
subcircuit nodes (by  
position) to the  
interconnect  
structure

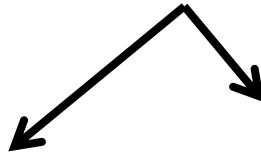
```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS          pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail     signal_name    VDD | VDD (POWER connection)
4  Pin_Rail     signal_name    VSS | VSS (GND connection)
5  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail     pad_name      VDDQ | pad_name with VDD
8  Pad_Rail     pad_name      VSSQ | pad_name with VSS
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```

# Complete [Interconnect Model Set] With Both [Interconnect Models]

[Interconnect Model Set]



[Interconnect Models]



```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS      buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref   pin_name      A1 | VDD (POWER connection)
4  Pulldown_ref pin_name      A1 | VSS (GND connection)
5  Buffer_I/O   pin_name      A1 | DQ1 (DQ signal)
6  Pullup_ref   pin_name      A2 | VDD (POWER connection)
7  Pulldown_ref pin_name      A2 | VSS (GND connection)
8  Buffer_I/O   pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail     pad_name      VDDQ | VDD  POWER
10 Pad_Rail     pad_name      VSSQ | VSS  GND
|
[End Interconnect Model]
```

```
[Interconnect Model] Partial_ISS_pad_pin_2
|
File_IBIS-ISS      pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail     signal_name    VDD | VDD (POWER connection)
4  Pin_Rail     signal_name    VSS | VSS (GND connection)
5  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail     pad_name      VDDQ | VDD is signal name
8  Pad_Rail     pad_name      VSSQ | VSS is signal name
|
[End Interconnect Model]
|
[End Interconnect Model Set]
```



[End Interconnect Model Set]

# [Interconnect Model Set Group] (New) for a Selected Group

```
[Interconnect Model Set Group]      A1_A2_PDN
|
| Interconnect Model Set Name      File_reference
Full_ISS_PDN                      NA
|
[End Interconnect Model Set Group]
```

[Interconnect Model Set Group] is at same level as [Package Model] for selected group of Buffer\_IO pin(s)

Name should be descriptive for easy selection (e.g., A1-A2\_PDN)

Can contain several references to [Interconnect Model Set]s

Sets can be in the .ibs file (NA) or in a separate directories

[Interconnect Model]s within a Group must be connected

# **File\_TS, File\_TS0 (New) Issue**

- ❑ Touchstone files can now be documented with a single reference (File\_TS) or ground “Node 0” reference (File\_TS0)
  - Offering both choices eliminates issue about which is better
  - File\_TS0 would not be used for power-aware simulations
- ❑ File\_IBIS-ISS with S model can be used for more references, if needed



# Touchstone Unused Port Termination

- ❑ Not an issue with IBIS-ISS – all terminal connections are required
- ❑ For Touchstone files
  - Unused\_port\_termination <Open | Reference>
  - Reference: reference impedance reduces the number of Touchstone ports through matrix reduction
  - Open: represents the physically disconnected port
  - EDA tools might still provide an interface to override the choices
- ❑ Other options still being discussed

# Summary

- ❑ BIRD189.x improves IBIS package modeling
- ❑ Links IBIS, IBIS-ISS and Touchstone for package models
  - Adds flexible support for package loss, crosstalk and partitioning
- ❑ Formalizes and separates Die pads and Buffers
- ❑ Other extensions (not covered here) included

**New advanced Interconnect format for IBIS Version 7.0!**