Think PAM4 Serdes

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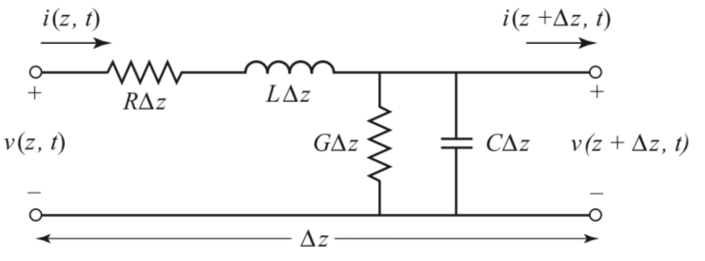
Outline

- Introduction of loss TL
- PAM4 Serdes Architecture
- CTLE characteristics and response
- FFE characteristics and response
- FFE parameter optimization and taps selection
- FFE defects and the advantages of DFE
- PAM4 Serdes Simulation with IBIS-AMI
- Summary

Lossy TL and ISI

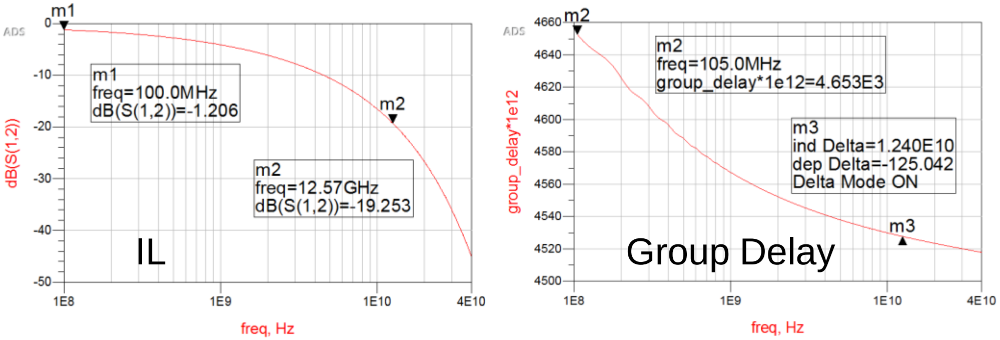
- **Characteristics of Lossy Transmission Line**



$i(z, t)$
$i(z+\Delta z, t)$
$R\Delta z$
$L\Delta z$
$G\Delta z$
$C\Delta z$
$v(z, t)$
$v(z+\Delta z, t)$
+
+
–
–
Δz

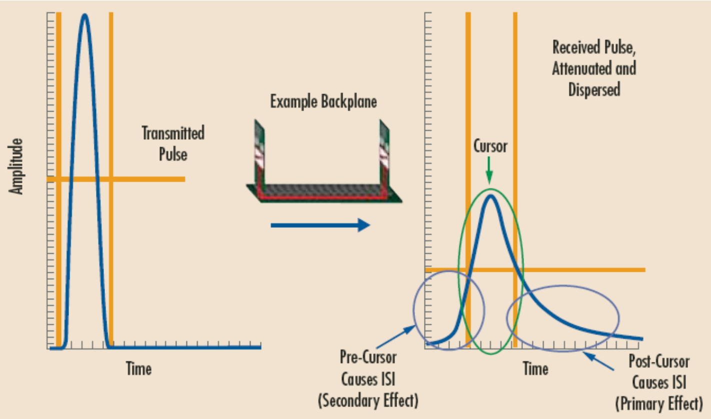
$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

RLGC are frequency dependent



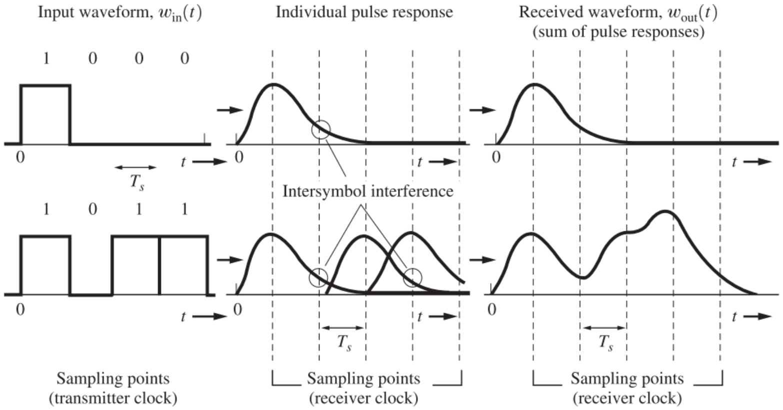
IL and Group Delay are frequency dependent

- **ISI: Channel is band limited, pulse width expands**



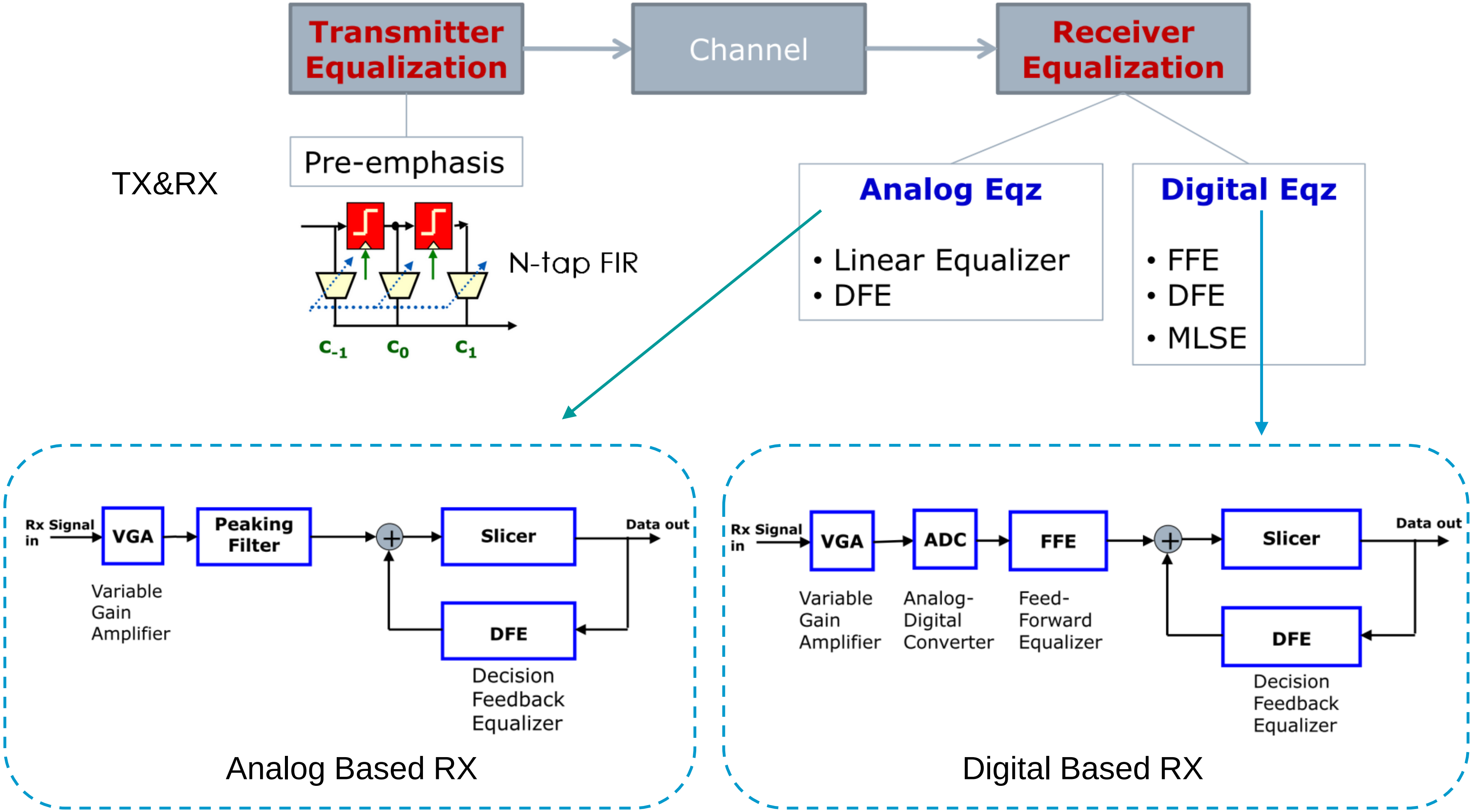
Amplitude
Transmitted Pulse
Time
Example Backplane
Received Pulse, Attenuated and Dispersed
Cursor
Pre-Cursor Causes ISI (Secondary Effect)
Time
Post-Cursor Causes ISI (Primary Effect)

ISI



Input waveform, $w_{in}(t)$
Individual pulse response
Received waveform, $w_{out}(t)$ (sum of pulse responses)
1 0 0 0
0
t
T_s
0
t
0
t
Intersymbol interference
1 0 1 1
0
t
0
t
T_s
0
t
T_s
Sampling points (transmitter clock)
Sampling points (receiver clock)
Sampling points (receiver clock)

PAM4 Serdes Architecture*



Transmitter Equalization → Channel → **Receiver Equalization**

TX&RX

Pre-emphasis

N-tap FIR

Analog Eqz

- Linear Equalizer
- DFE

Digital Eqz

- FFE
- DFE
- MLSE

c_{-1}
c_0
c_1
Rx Signal in
VGA
Peaking Filter
Slicer
Data out
DFE
Variable Gain Amplifier
Decision Feedback Equalizer
Rx Signal in
VGA
ADC
FFE
Slicer
Data out
DFE
Variable Gain Amplifier
Analog-Digital Converter
Feed-Forward Equalizer
Decision Feedback Equalizer

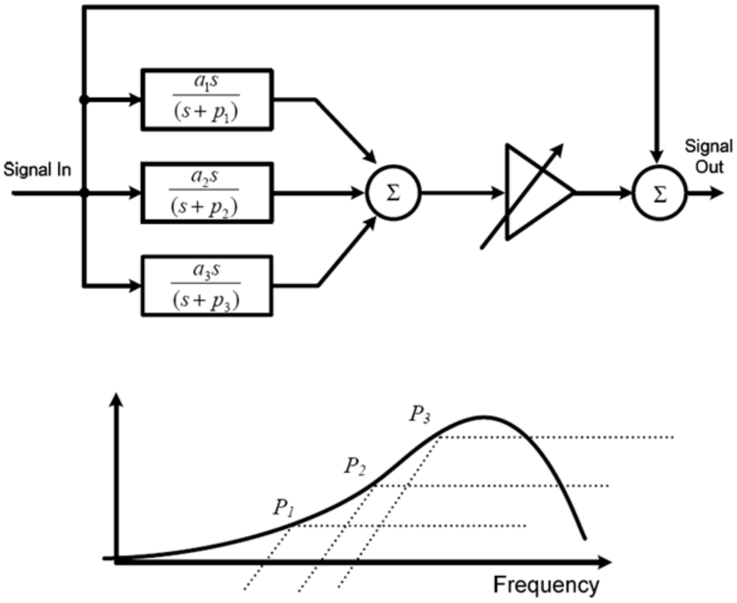
Analog Based RX

Digital Based RX

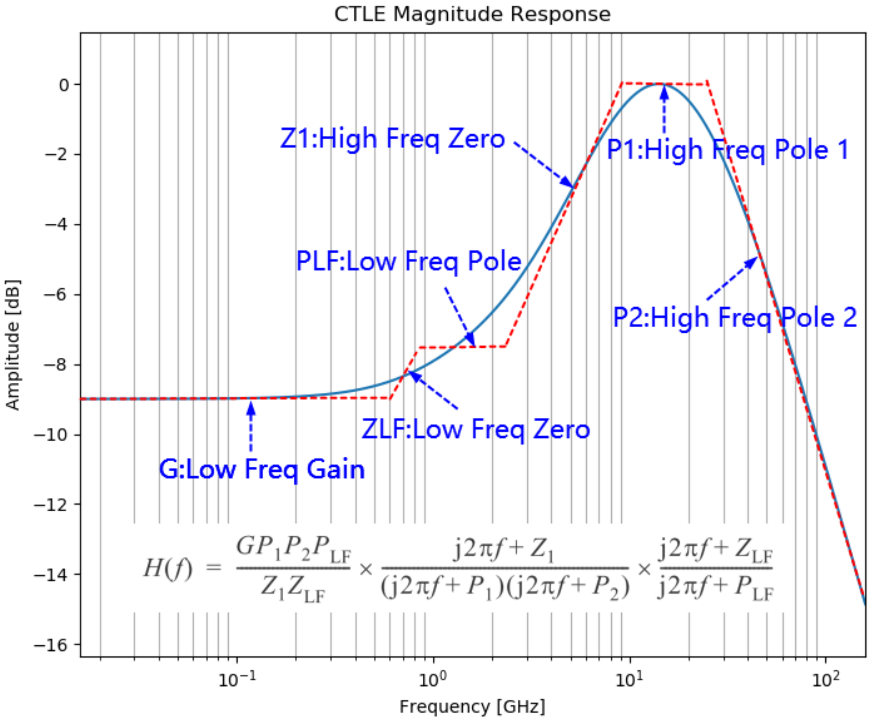
[*: Vivek Telang, Equalization for High-Speed Serdes Systems – A System-level Comparison of Analog and Digital Techniques, IEEE SSCS Technical Seminar, Friday, August 10, 2012]

CTLE Frequency Response

- **CTLE：High-Pass Filter**
  - The locations of Zeros and Poles determine frequency response
  - Zero: Rise at 20dB/decade
  - Pole: Drop at 20dB/decade


Signal In
$\frac{a_1 s}{(s+p_1)}$
$\frac{a_2 s}{(s+p_2)}$
$\frac{a_3 s}{(s+p_3)}$
Σ
Σ
Signal Out
P_3
P_2
P_1
Frequency

Typical CTLE

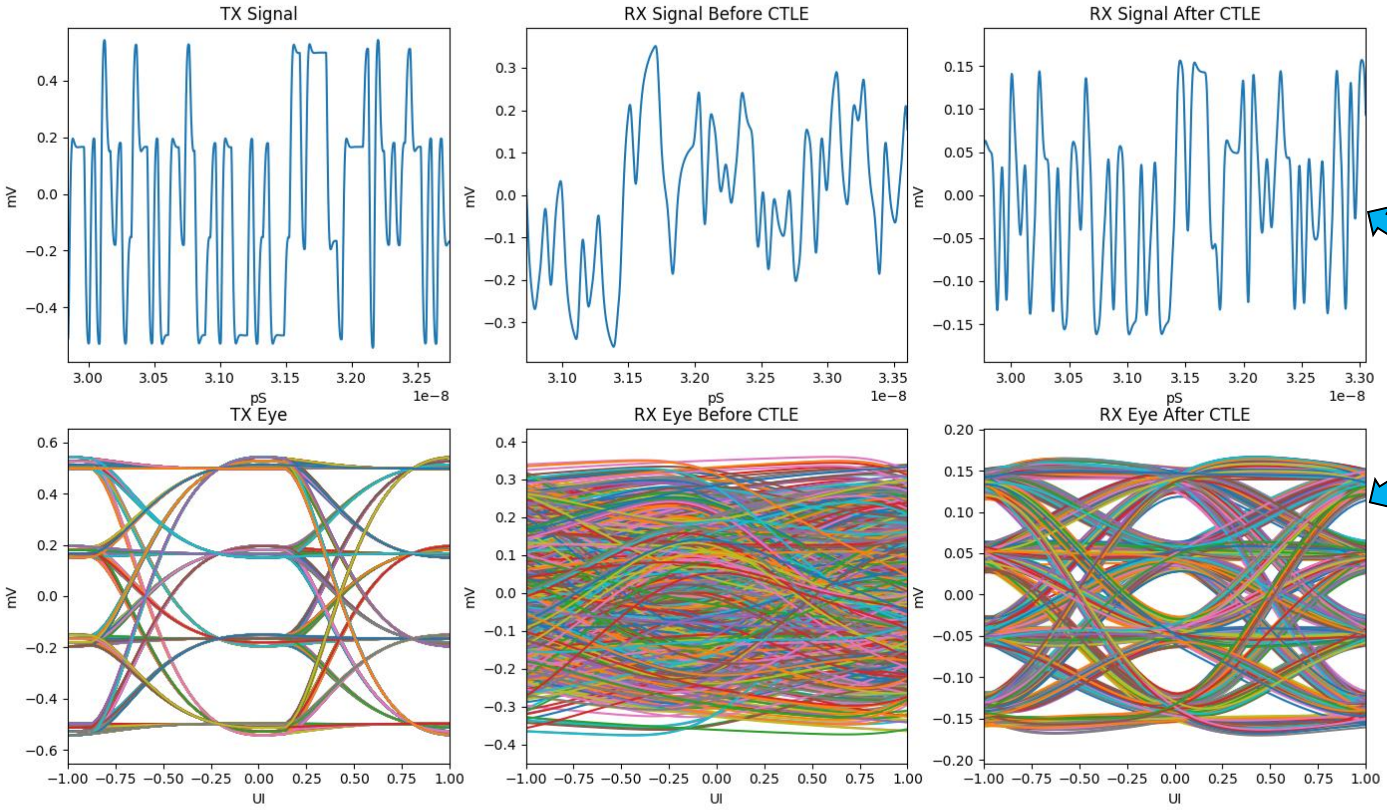


Reference CTLE in 802.3bs

Lossy Channel with CTLE-Time Domain

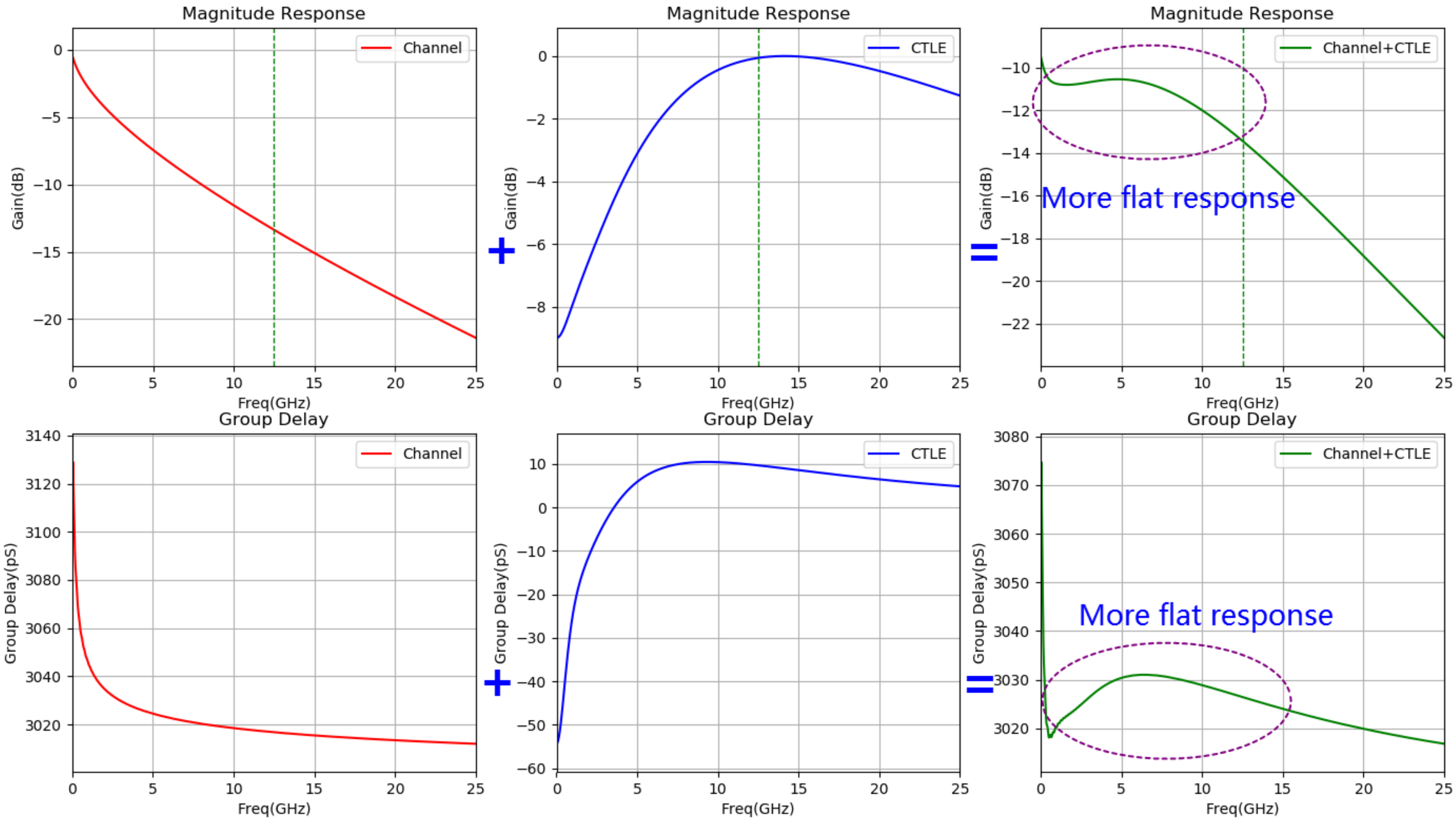
TX(NO EQ) → Channel(Loss=13dB) → RX(CTLE Gain=9dB)

50Gbps PAM4 Signal Simulation



CTLE Open Eye

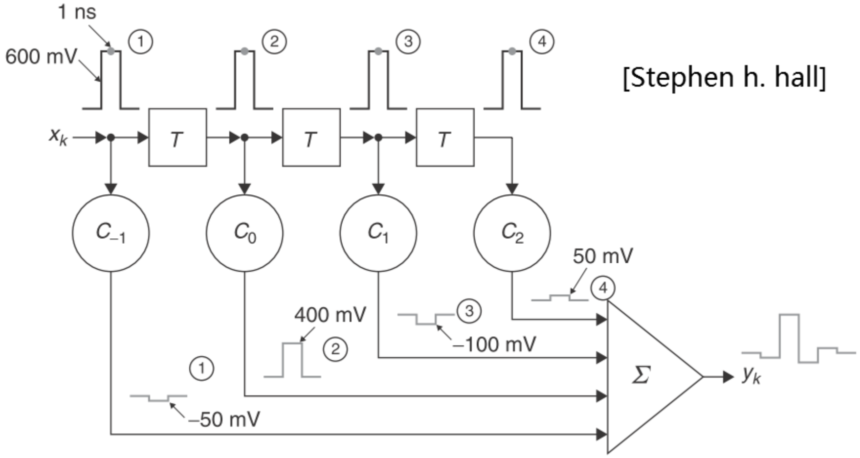
Lossy Channel with CTLE-Frequency Domain



CTLE makes in-band response more flat

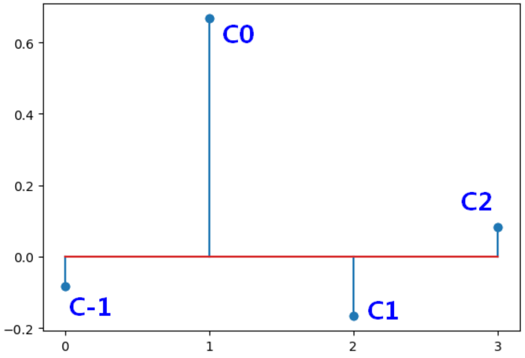
FFE and Its Response

Typical 4-Tap FFE
C-1=-1/12
C0=2/3
C1=-1/6
C2=1/12

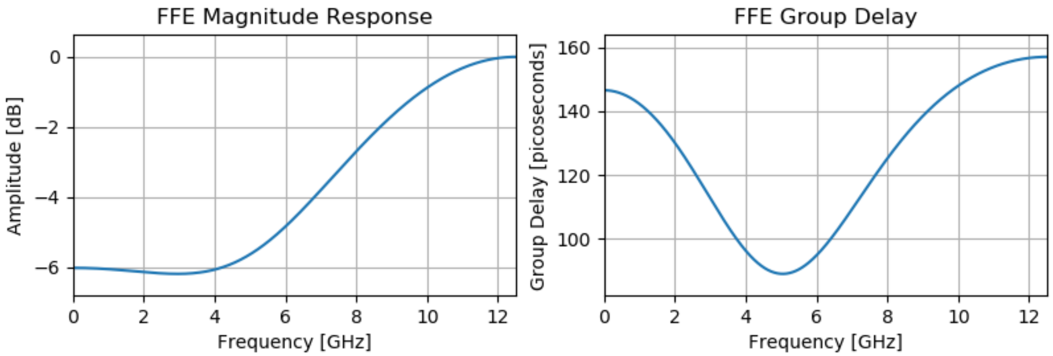


1 ns
600 mV
①
②
③
④
x_k
T
T
T
C_{-1}
C_0
C_1
C_2
50 mV
④
400 mV
③
②
–100 mV
①
–50 mV
Σ
y_k

[Stephen h. hall]



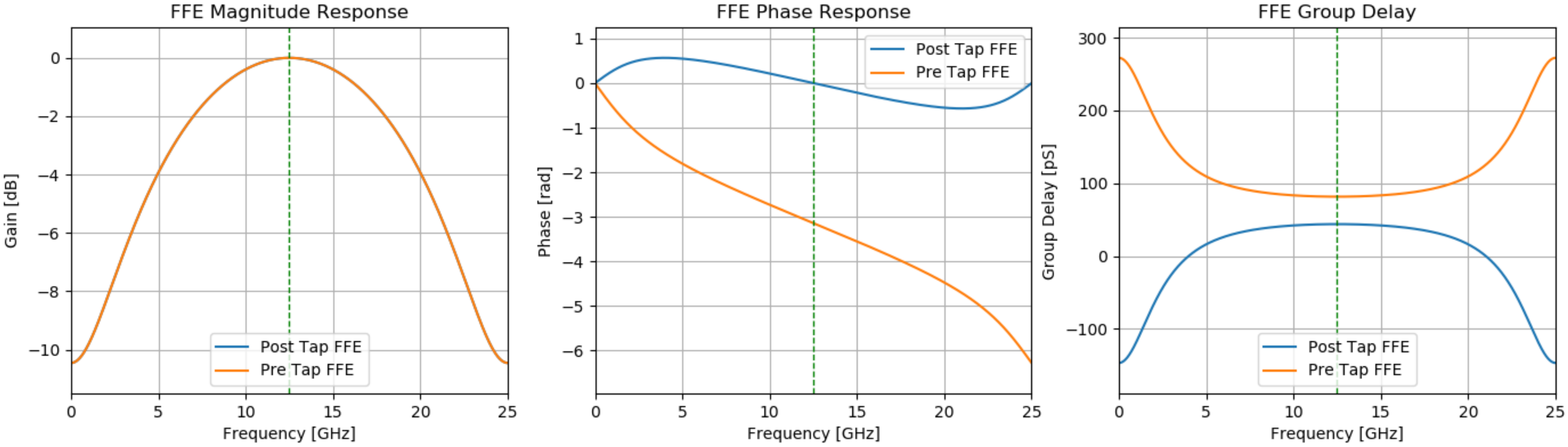
Impulse Response



Frequency Domain Response

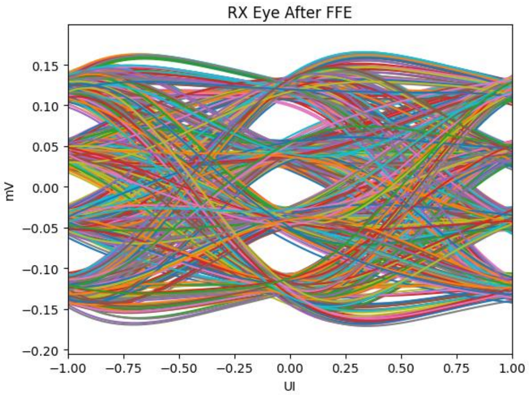
Post Tap versus Pre Tap

- **Post Tap FFE: [0.65, -0.35], Pre Tap FFE: [-0.35, 0.65]**
- **Gain= 20*log(1/0.3)=10.4dB to reach peak gain at Nyquist frequency**
- **Different phase response and group delay**

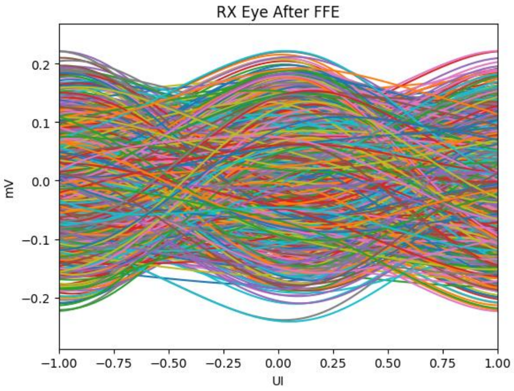


Tap coefficients of FFE

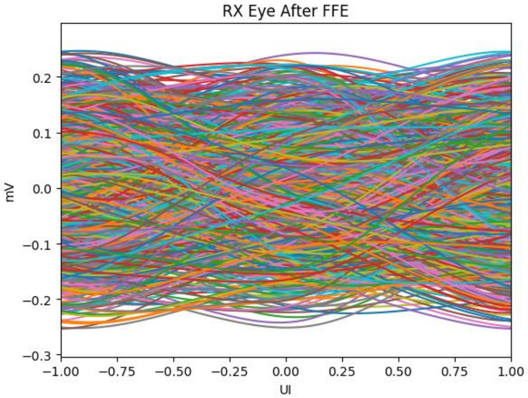
- **Same TX and Channel but different RX FFE**



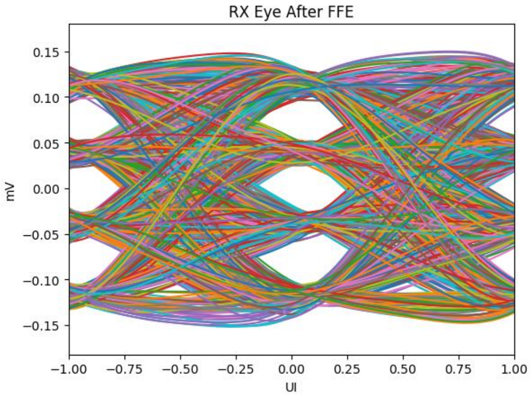
FFE=[0.65, -0.35]



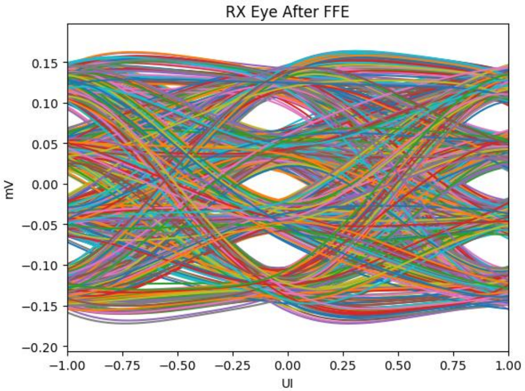
FFE=[-0.35, 0.65]



FFE=[0.65, 0, -0.35]



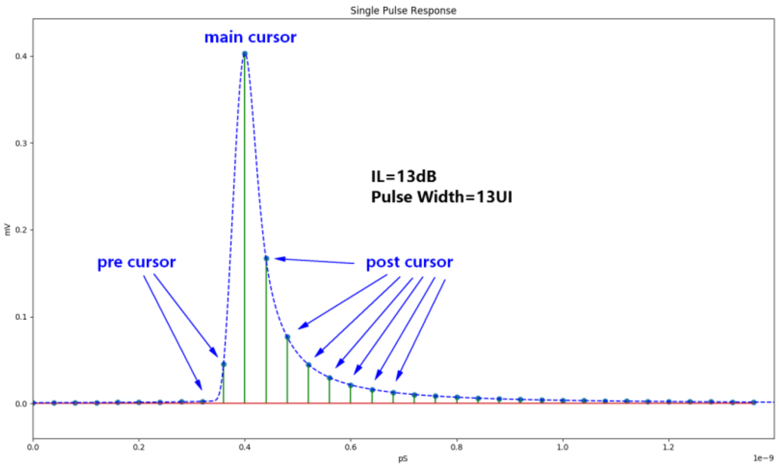
FFE=[-0.1, 0.65, -0.25]

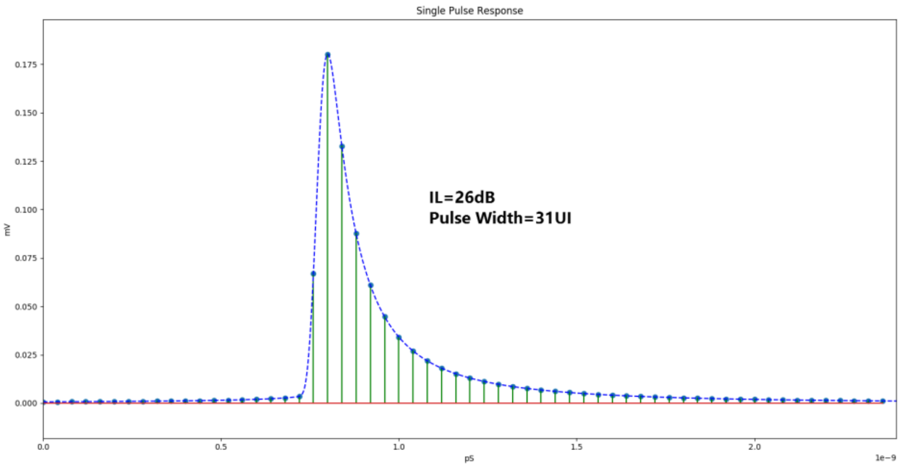


FFE=[0.65, -0.3, -0.05]

How many taps are enough?
How to choose tap values?

Single Pulse Response of Channel

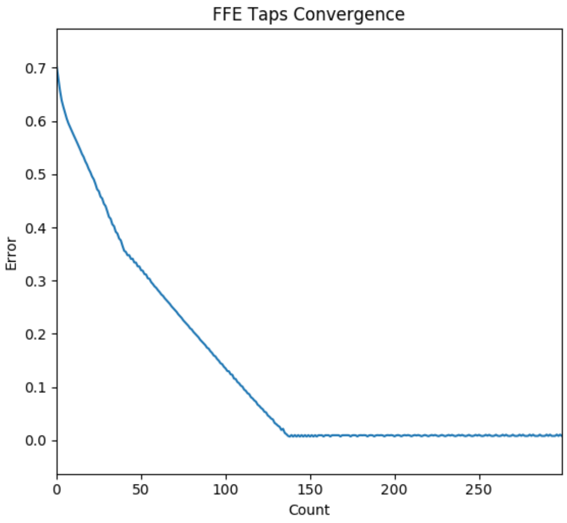




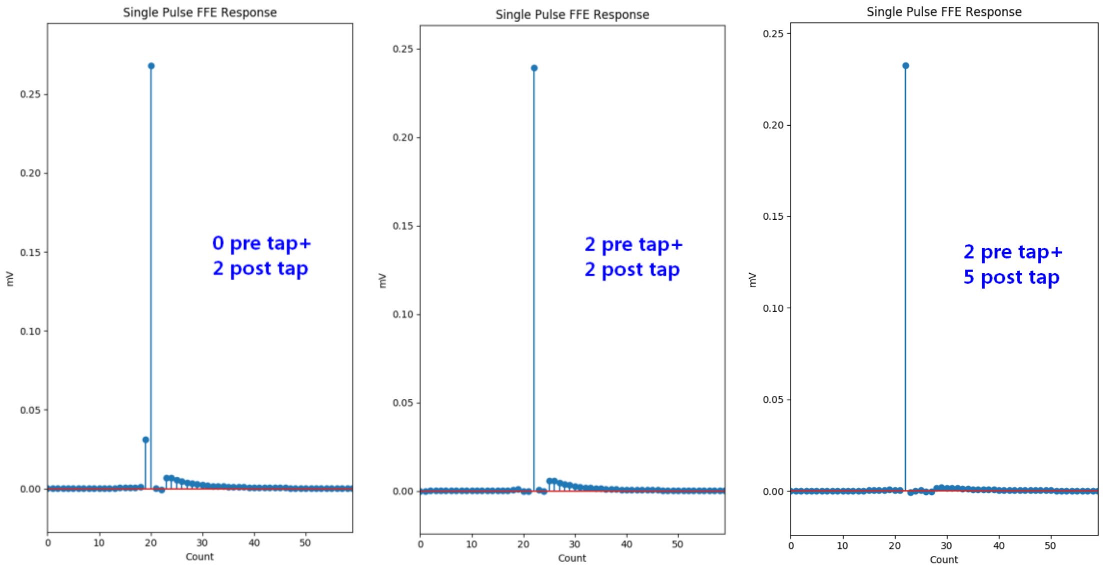
- **The greater loss of the channel produces a lower pulse response amplitude and a greater pulse width**
- **When Σ(|pre cursor|+|post cursor|)>main cursor, eye closed**

How to choose FFE tap values?

- **Adaptive FFE**
  - ZF: Zero-Forcing
  - LMS: Least Mean Square



FFE coefficient convergence



0 pre tap+
2 post tap

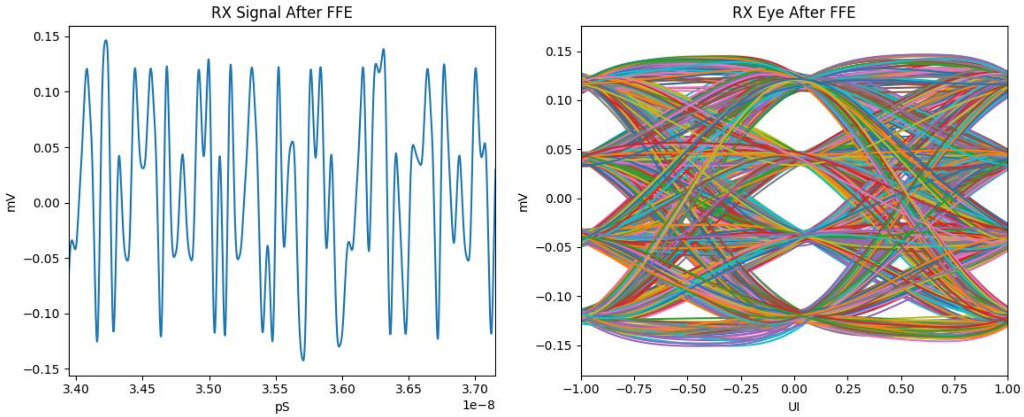
2 pre tap+
2 post tap

2 pre tap+
5 post tap

Different number of taps

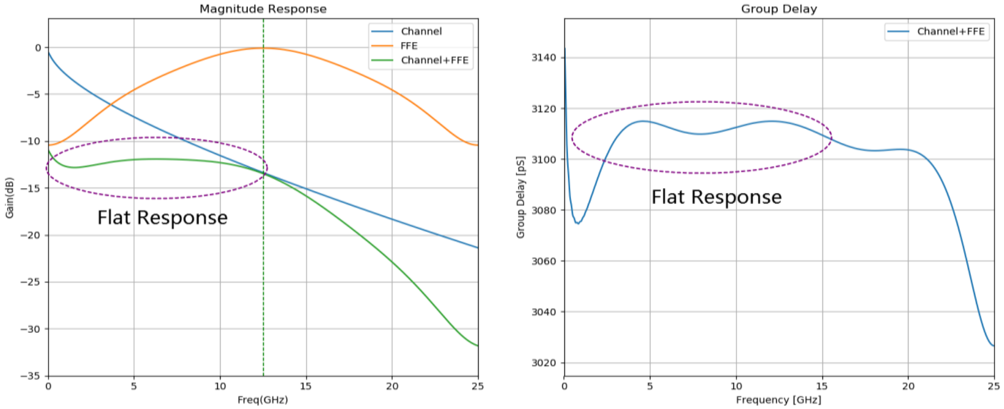
Time-frequency Response of Optimized FFE

TX(NO EQ) → Channel(LOSS=13dB) → RX(FFE,1 pre+3 post)



Time Domain Simulation

The optimal taps coefficient produce the best received eye

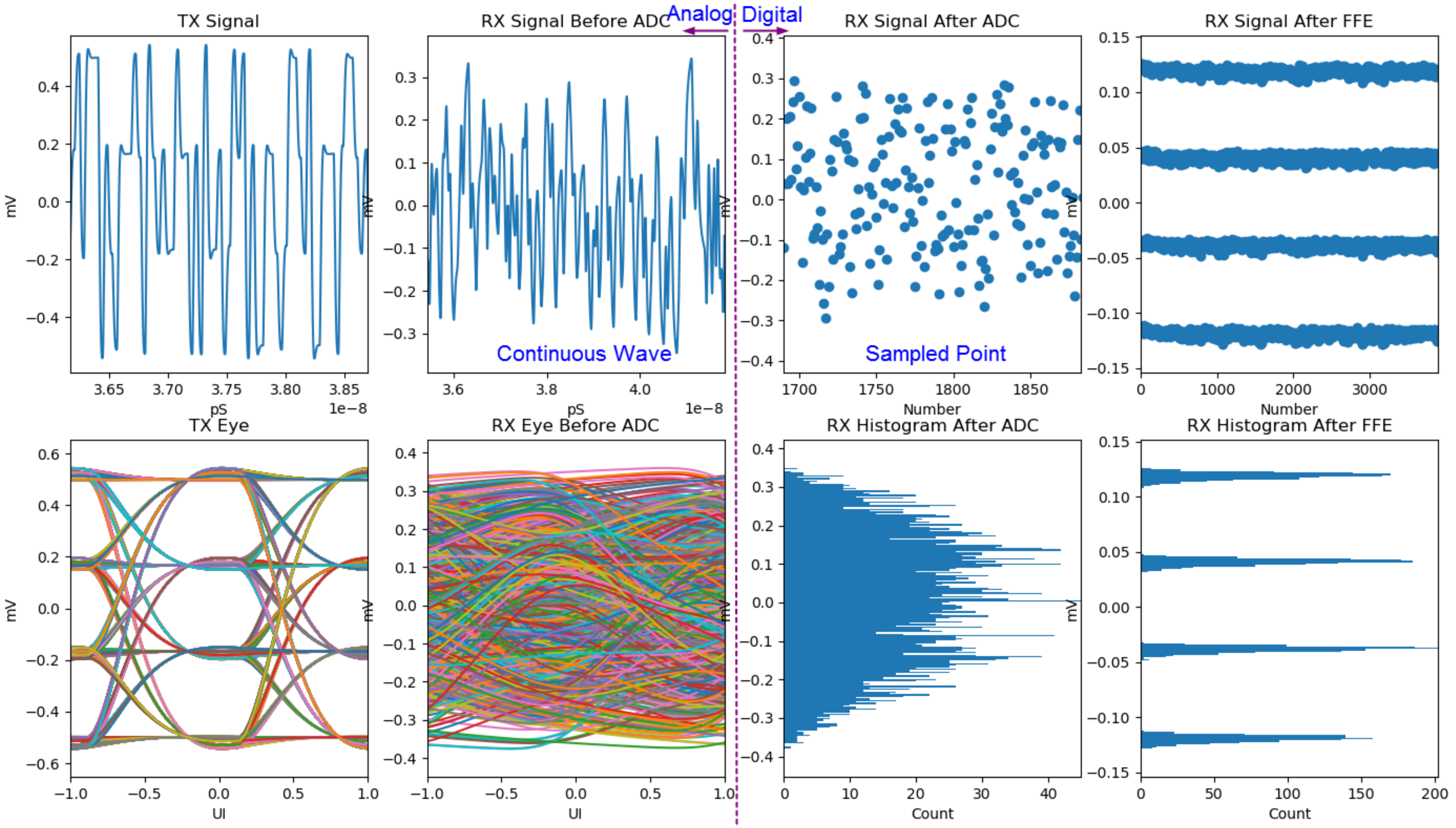


Frequency Domain Simulation

Multi-Taps FFE can do fine tuning of gain and phase

Digital Based FFE

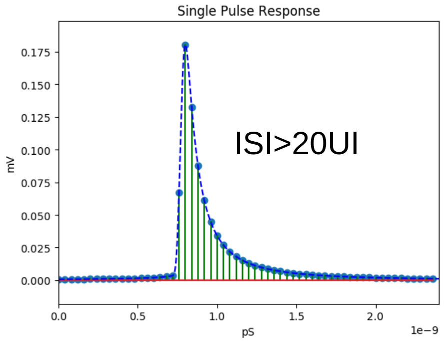
TX(NO EQ) → Channel(LOSS=13dB) → RX(ADC+FFE,1 pre+3 post)



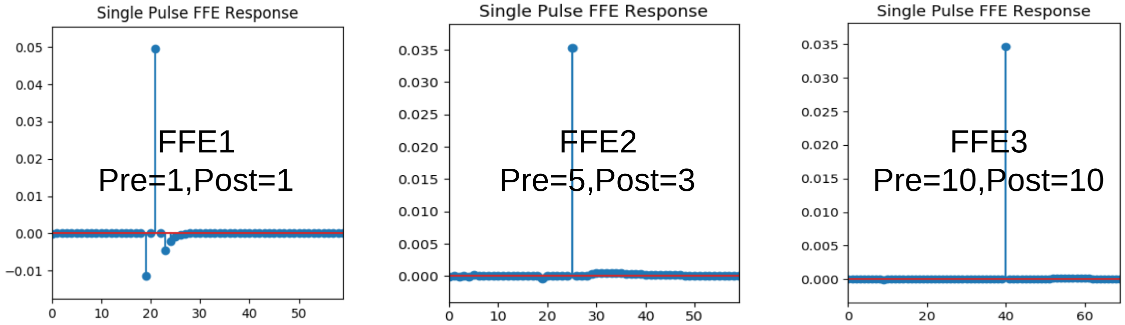
TX Signal RX Input Signal ADC Sampled Signal Equalized Signal

How many FFE taps are enough?

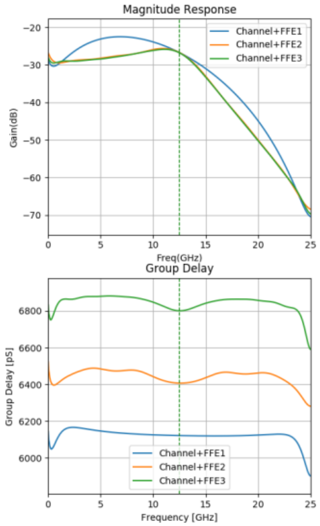
TX(NO EQ) → Channel(LOSS=26dB) → RX(ADC+Digital FFE)



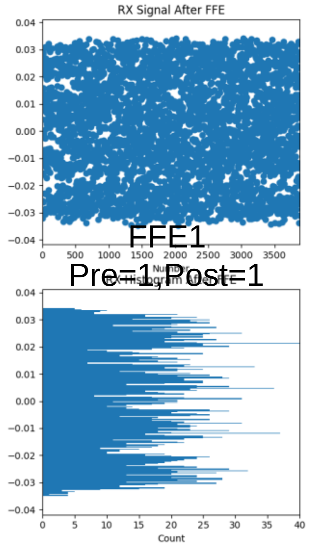
SPR



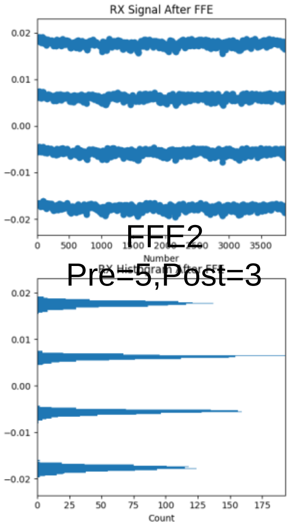
Equalized SPR with Different FFE



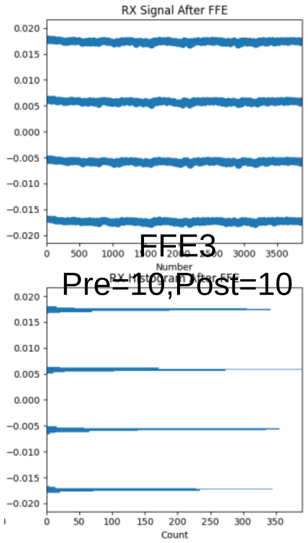
Frequency Response Compare



Bad Signal

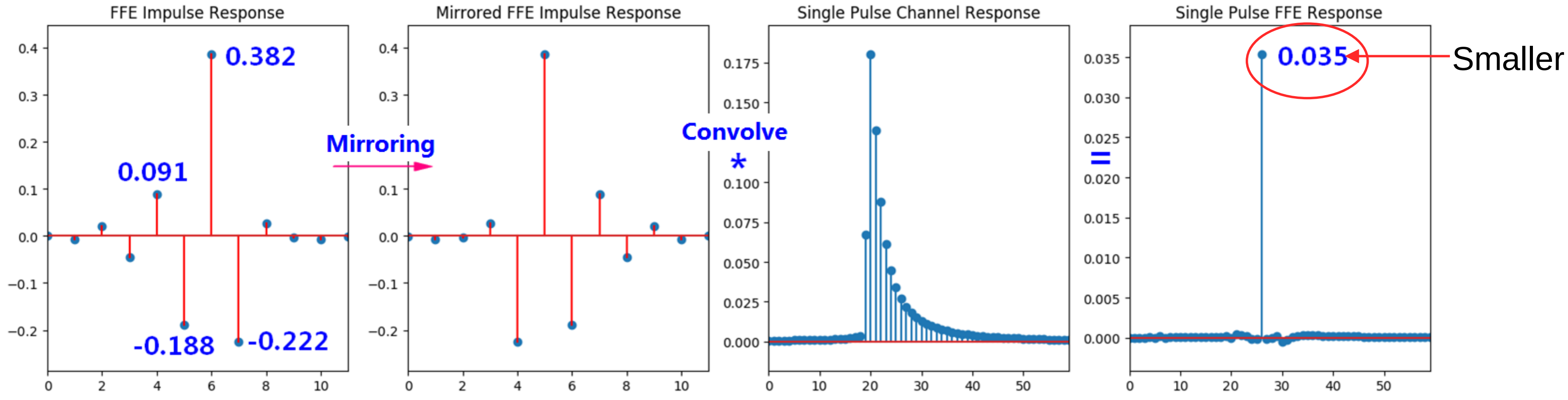


Better Signal



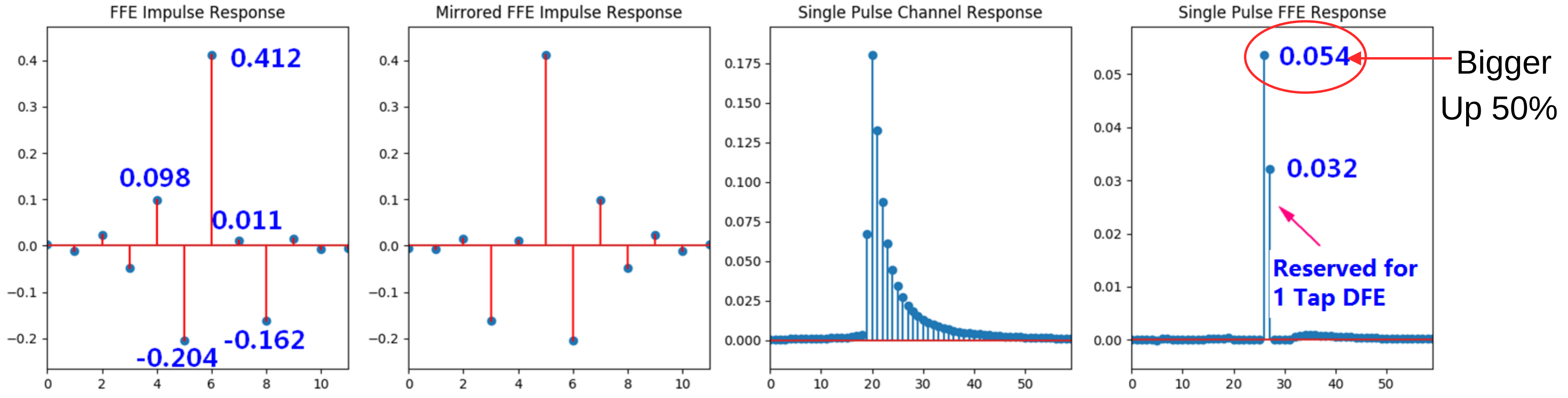
Best Signal

The Unique Value of DFE



Smaller

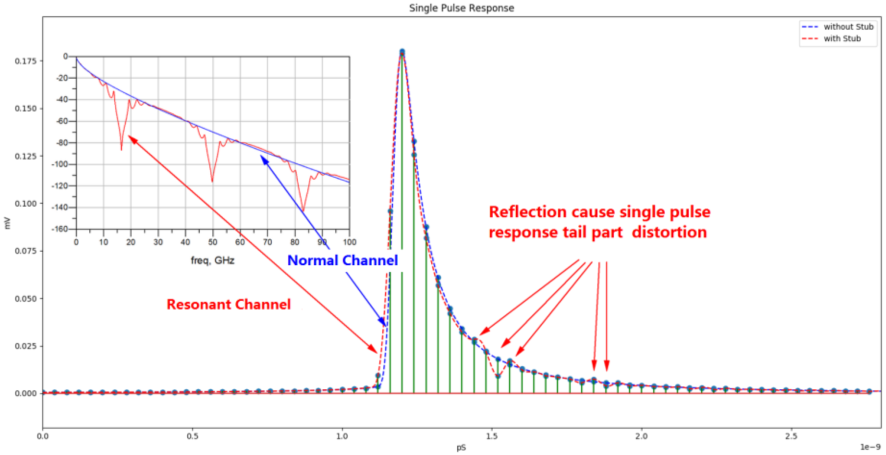
Without DFE: smaller main cursor value



Bigger
Up 50%

With 1 Tap DFE: bigger main cursor value

The Dead Zone of FFE

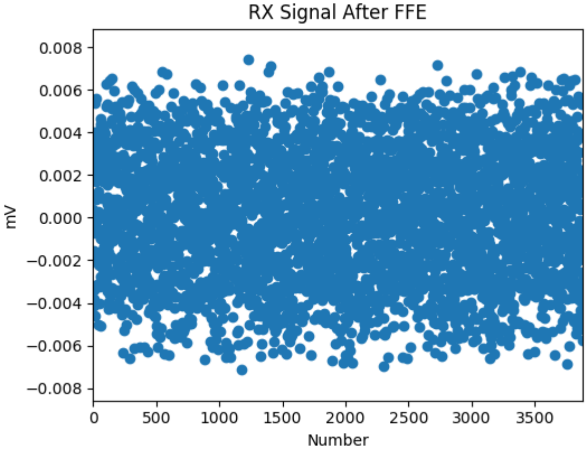


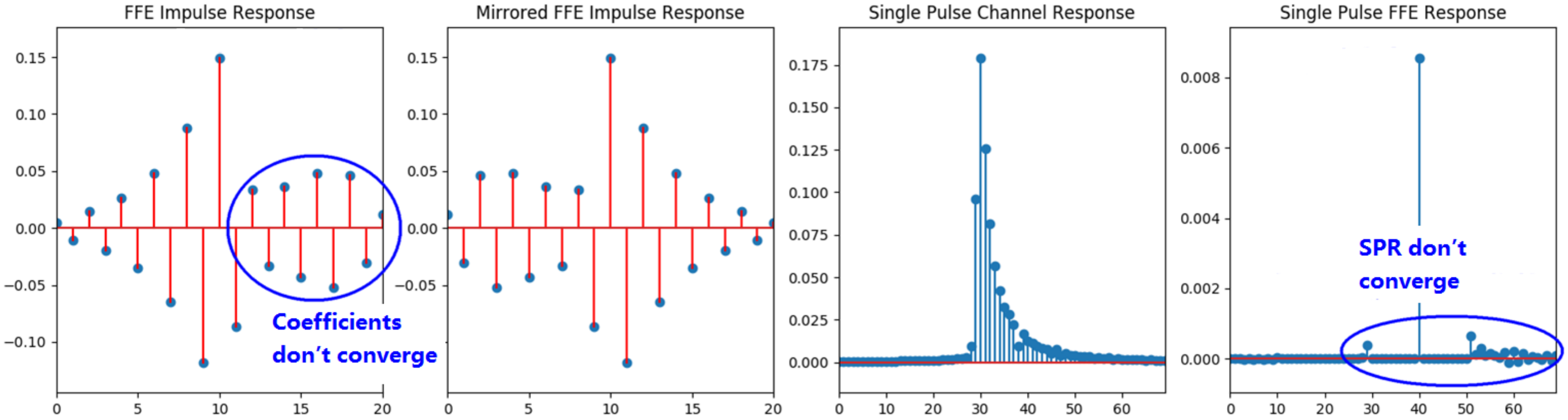
Reflection cause single pulse response tail part distortion

Normal Channel

Resonant Channel

SPR Compare



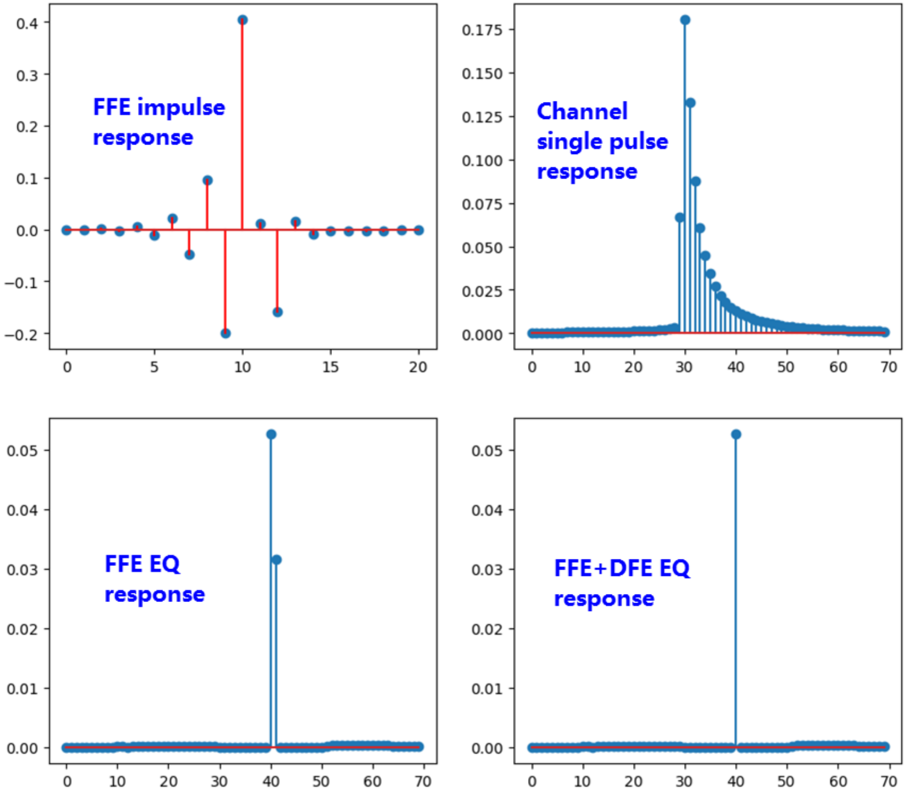


Coefficients don't converge

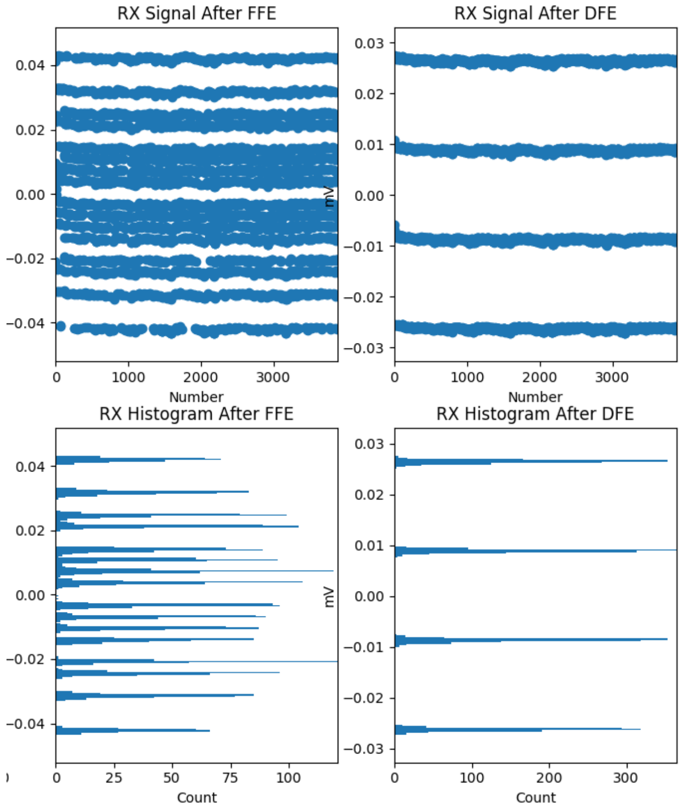
SPR don't converge

FFE Can ‘t Recover Signal from Resonant Channel

Multi-Tap FFE + 1 Tap DFE Simulation



Single Pulse Response



Full Channel Simulation

By adding1-tap DFE, the amplitude of equalized signal increases by 50%. For high-loss long-distance channel, RX with DFE is very important.

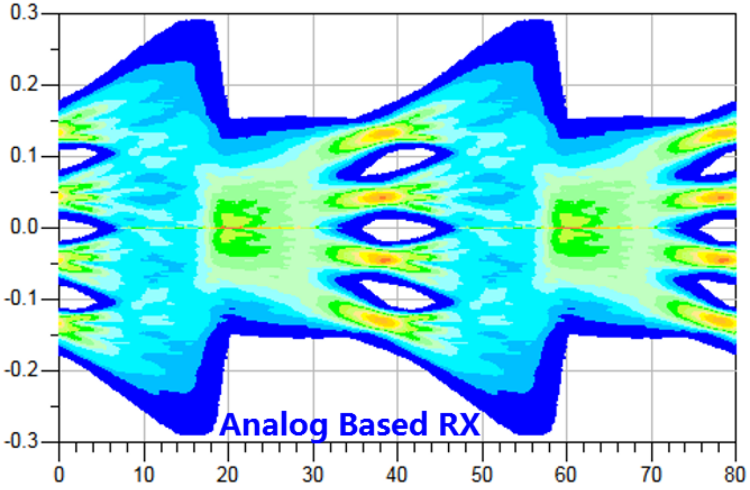
PAM4 Serdes Simulation with IBIS-AMI

```
AMI_GetWave (double *wave,
 long wave_size,
 double *clock_times,
 char **AMI_parameters_out,
 void *AMI_memory)
```

Time Domain Waveform

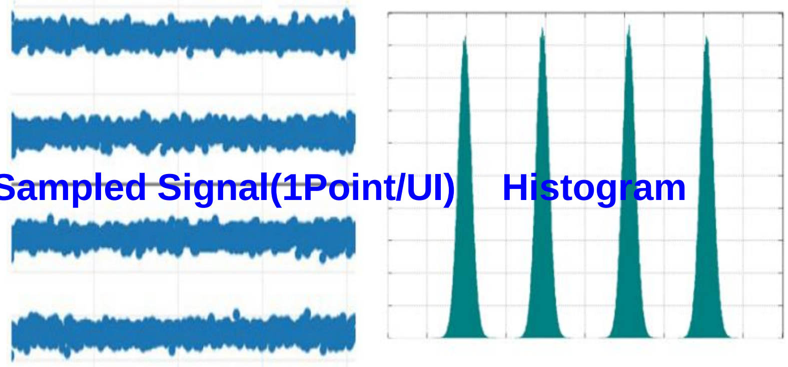
IBIS-AMI API

✓



Analog Based RX

✗



Digital Based RX

Summary

- **With the arrival of the PAM4 Serdes, more receivers change from analog architecture to digital architecture**
- **Digital based RX can leverage DSP technology, but RX becomes more complicated**
- **The current IBIS-AMI specification is suited for analog based RX, but lacks support for the digital architectures**
- **IBIS-AMI is a type of “black box” model that hides the signal of the internal nodes**
- **Need a more general PAM4 simulator to support digital RX (adc, adaptive dsp, cdr, snr, ser, ber, fec, etc.)**
- **This presentation illustrates the need**

Thank you

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