Embedded DDR4 Design Simulation

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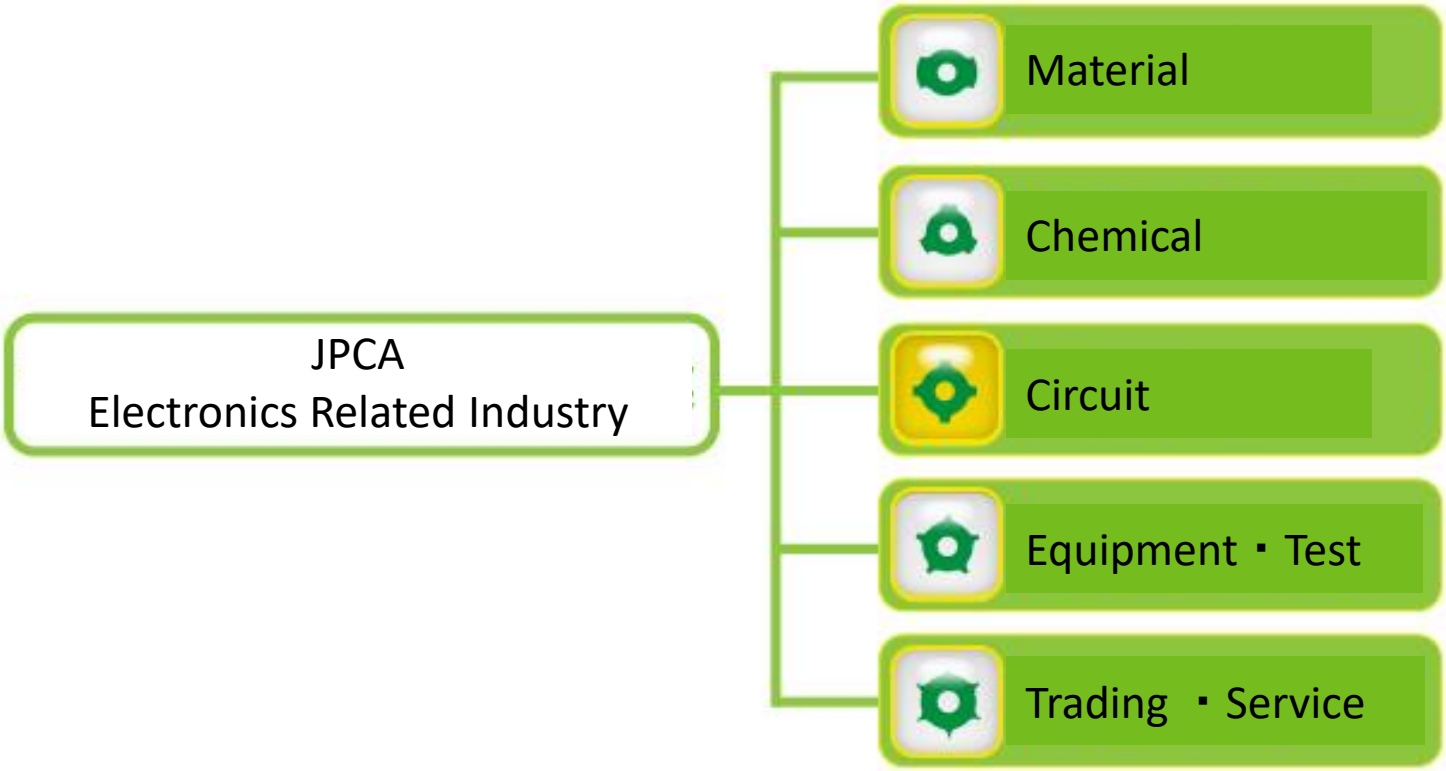
Contents

- JPCA/JPCA Design Academy
- JPCA DDR4 Project
- Simulation Results and Measurements
- Package Length Specification

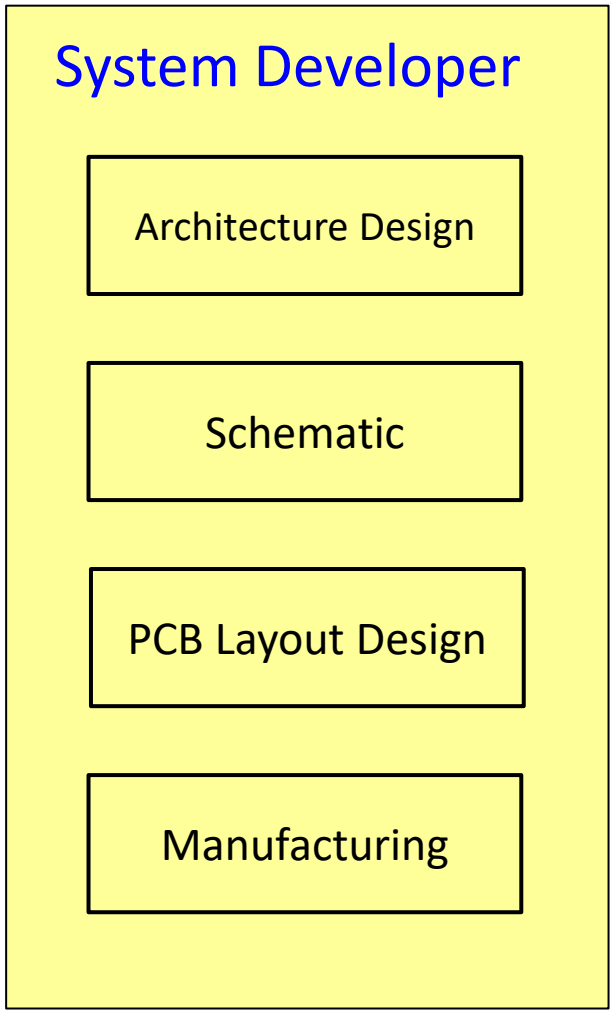
JPCA

- Japan Electronics Packaging and Circuit Association



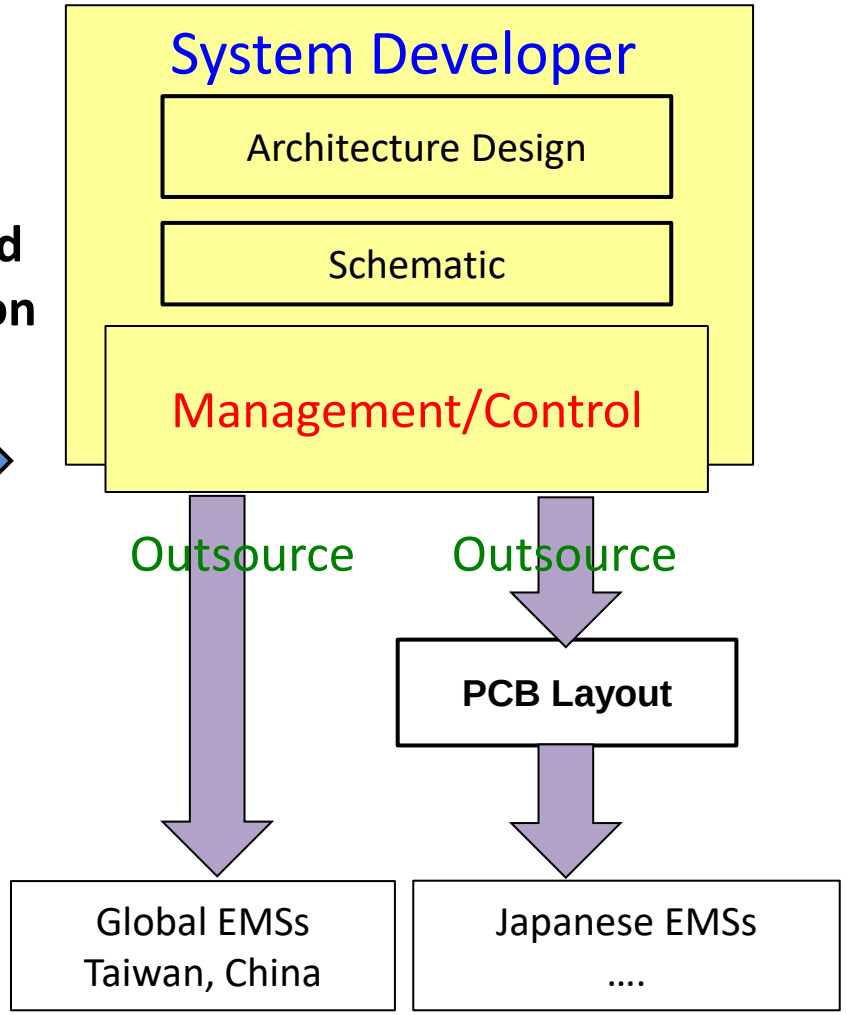
Japanese PCB Design/Manufacturing

Past Japanese Development



Selection and Concentration

Current Japanese Development



Who Is Concerned about Design Rules?

System Developer

- High Speed Circuit Design
  - Many people needed to satisfy difficult issues
  - Difficult to satisfy all

PCB Design/Manufacturing Related Issues

- Via design
- Line/Space
- Layer Stack-up
- PCB Material
- Line width
- Standard, Specification
- Skew
- Jitter
- Power Integrity
- Signal Integrity
- On Die Terminator
- I/F Topology

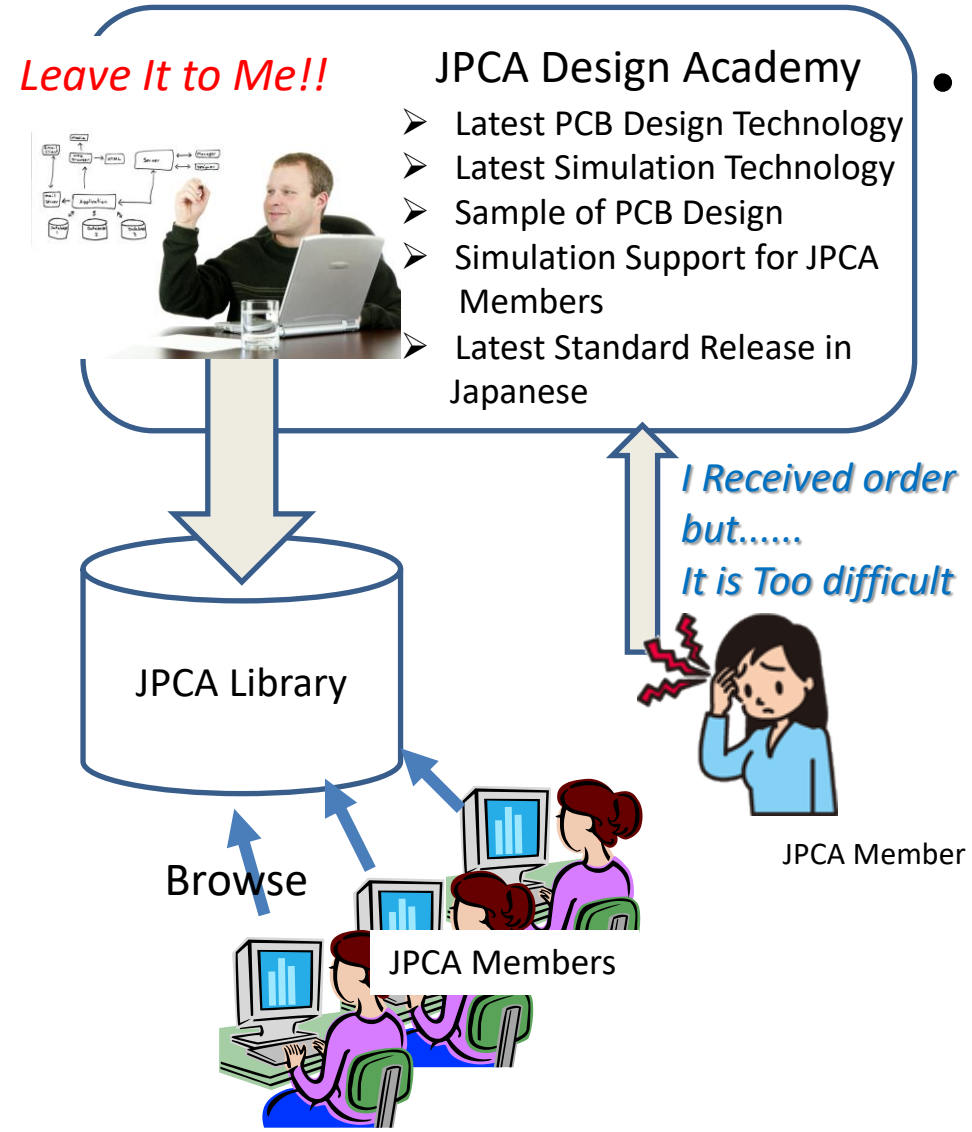
Consignment All

Design Bureau

We have to correct
all information
and check all by ourselves...

System Developer:
Please refer IC's PCB Design Guide （^-^;）
And so on, give me simulation report

JPCA Design Academy

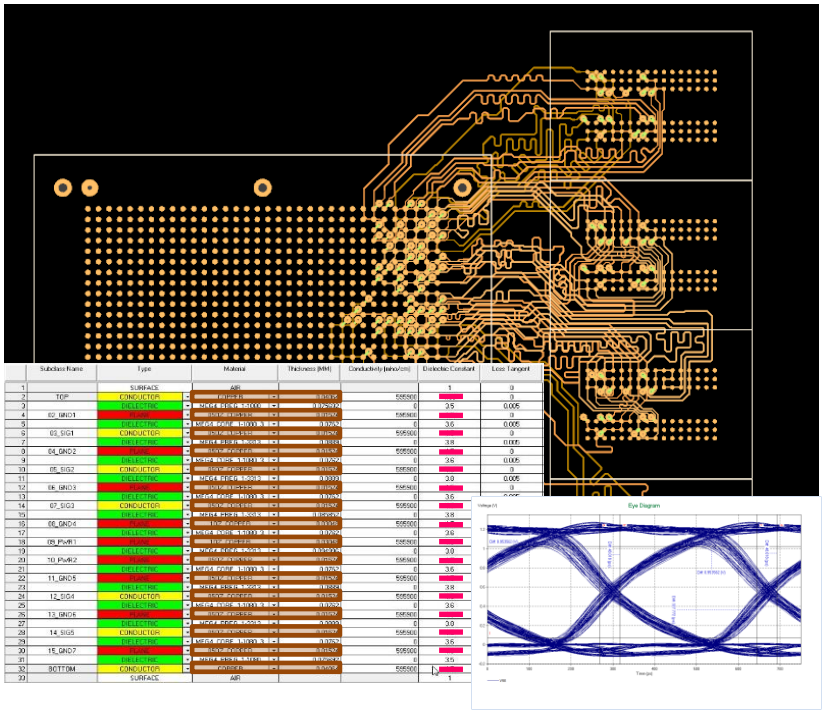


- Found JPCA Design Academy
  - PCB Design Review
  - High-Speed Design Guideline
  - Design/Simulation Consulting
  - Simulation Tools
  - Simulation Engineer Training
  - Transfer Technical Documentations in Japanese

DDR4 Design Project

- JPCA Design Academy's Project

ASIC Vender's Reference Design

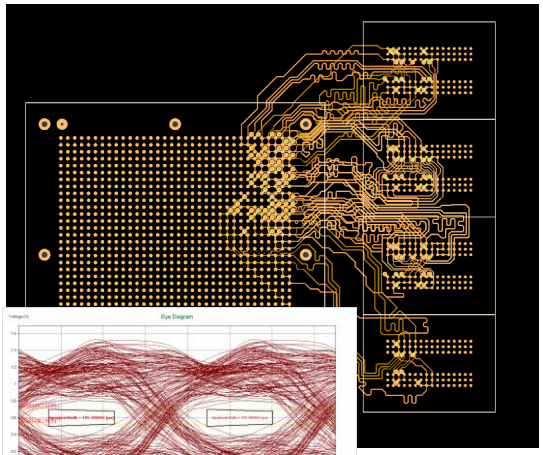


Reference Design
- Megtron 6
- 16 Layers
- Constraint

Change Condition

- Material FR4
- Line / Space
- Via size
- Cross Section

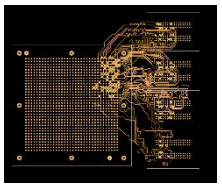
User's Requirements



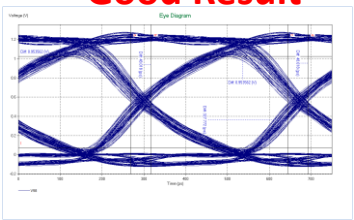
Cannot Apply the Same Design

Change Layout

Propose !



Good Result



* Satisfy the Manufacturing Requirements
* Satisfy the System Developer's Requirements

DDR4 Design Project

- Step 1:　2015
  - ASIC Vender's Reference Design
    - Review the JEDEC DDR4 Specification
    - Review the Reference Board Rule/Topology
    - PI/SI Simulation
    - Measurement
    - Release the DDR4 Design Guide

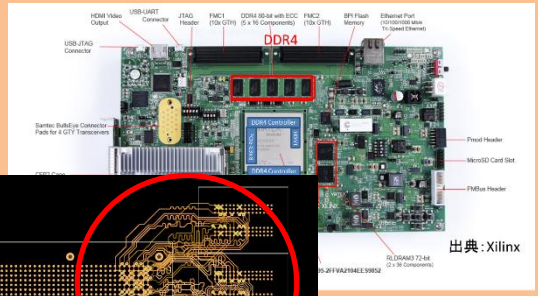
DDR4 Design Project

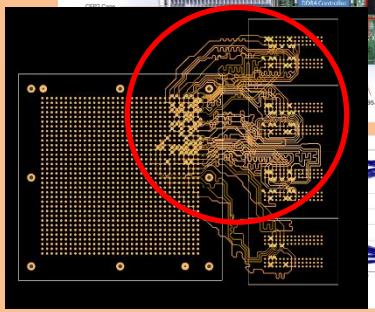
- Step 2:　2016
  - 3 Japanese PCB Manufacturers Design Board (Case1, Case2, Case3)
  - Use JPCA Design Academy's DDR4 Design Library (Guide)
    - 3 Different Stackup
    - 3 Different Design
    - Use the Same Schematic
    - Use the Same Design Guide
    - Now on going Design, Simulation
    - Will Measure
    - Will Release Design Guide Rev. 2

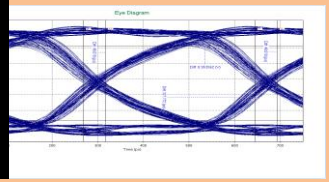
Step 2

JPCA Design Academy

DDR4 Library





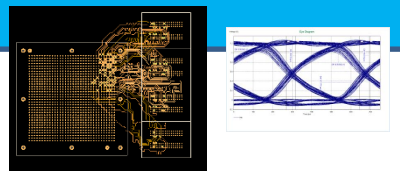


1. DDR4 System Structure
2. Basic Topology, Design Rule, , ,
3. Basic PCB's Design Guide (Via, Stackup, , ,)
4. SI Simulation Sample/Methodology
5. PI Simulation Sample/Methodology

A's PCB Parameter

Optimized Library

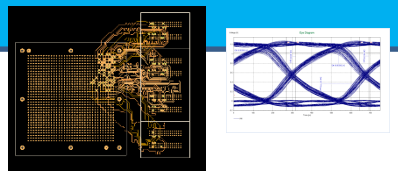
PCB Manufacturer A



B's PCB Parameter

Optimized Library

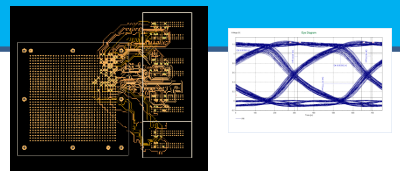
PCB Manufacturer B



C's PCB Parameter

Optimized Library

PCB Manufacturer C



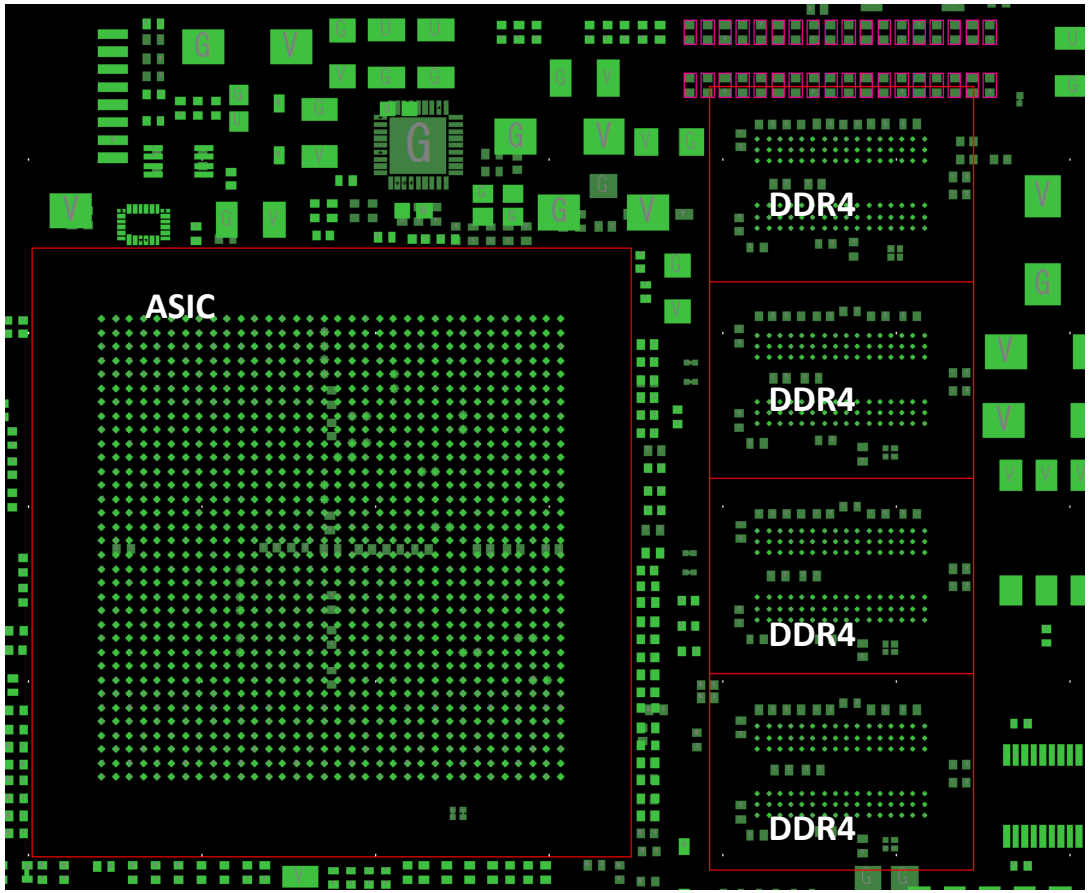
DDR4 Design Project

- Step 3:　2017~
  - Driver DDR4 Design Guide Rev.2
  - Design Consulting
  - Simulation Consulting

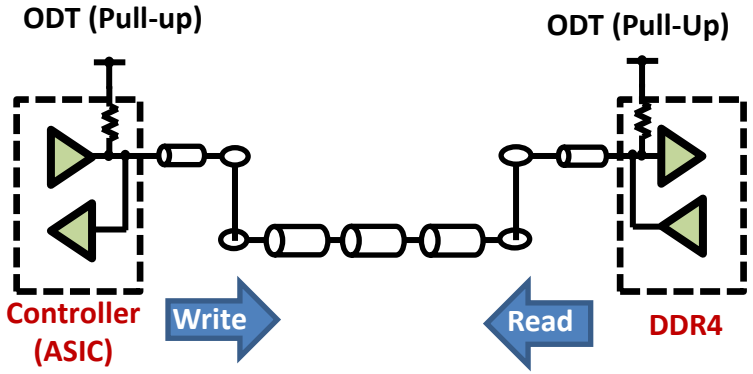
- Challenge New Technology (New Project) ?

Trial Boards

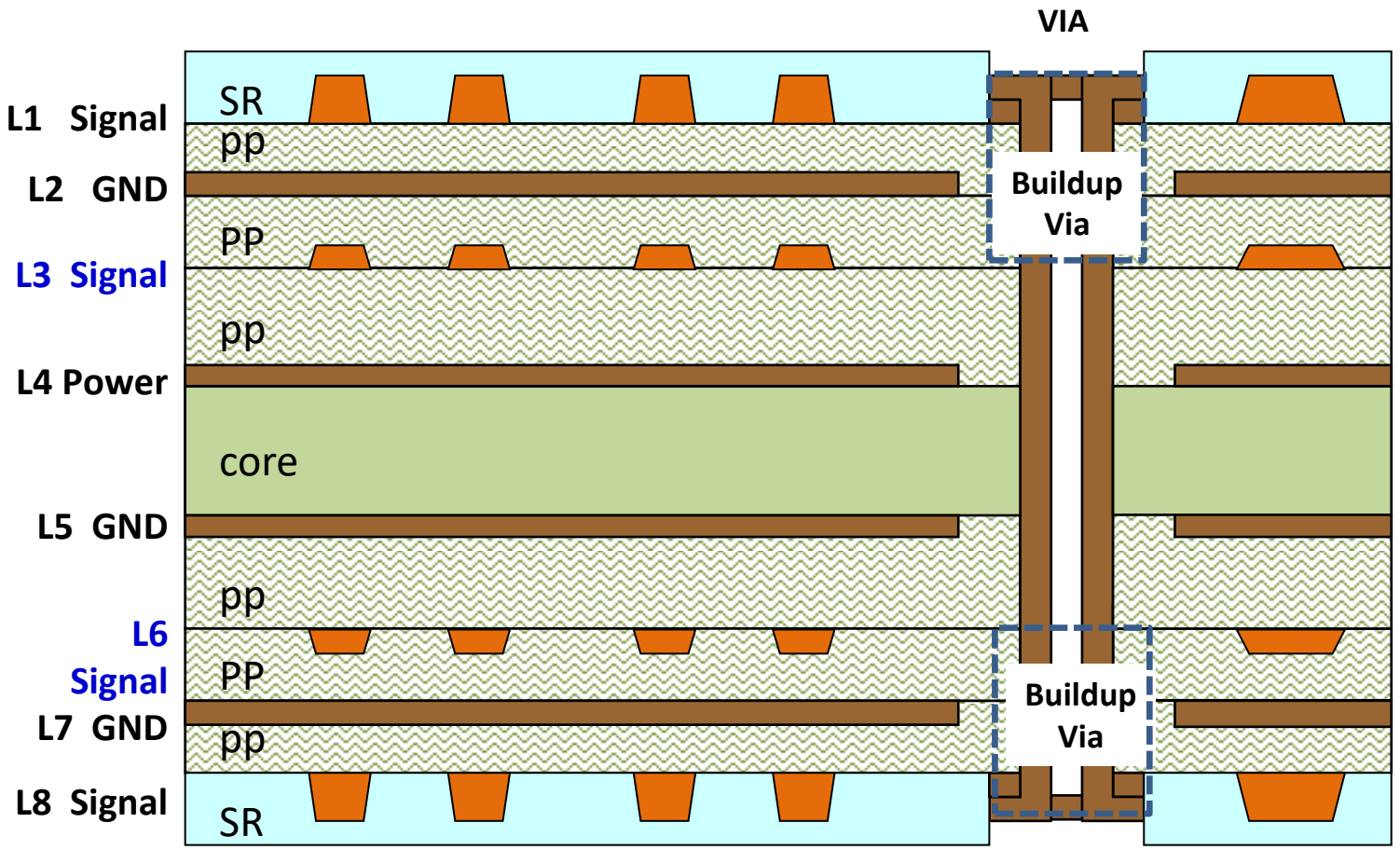
Reference Board



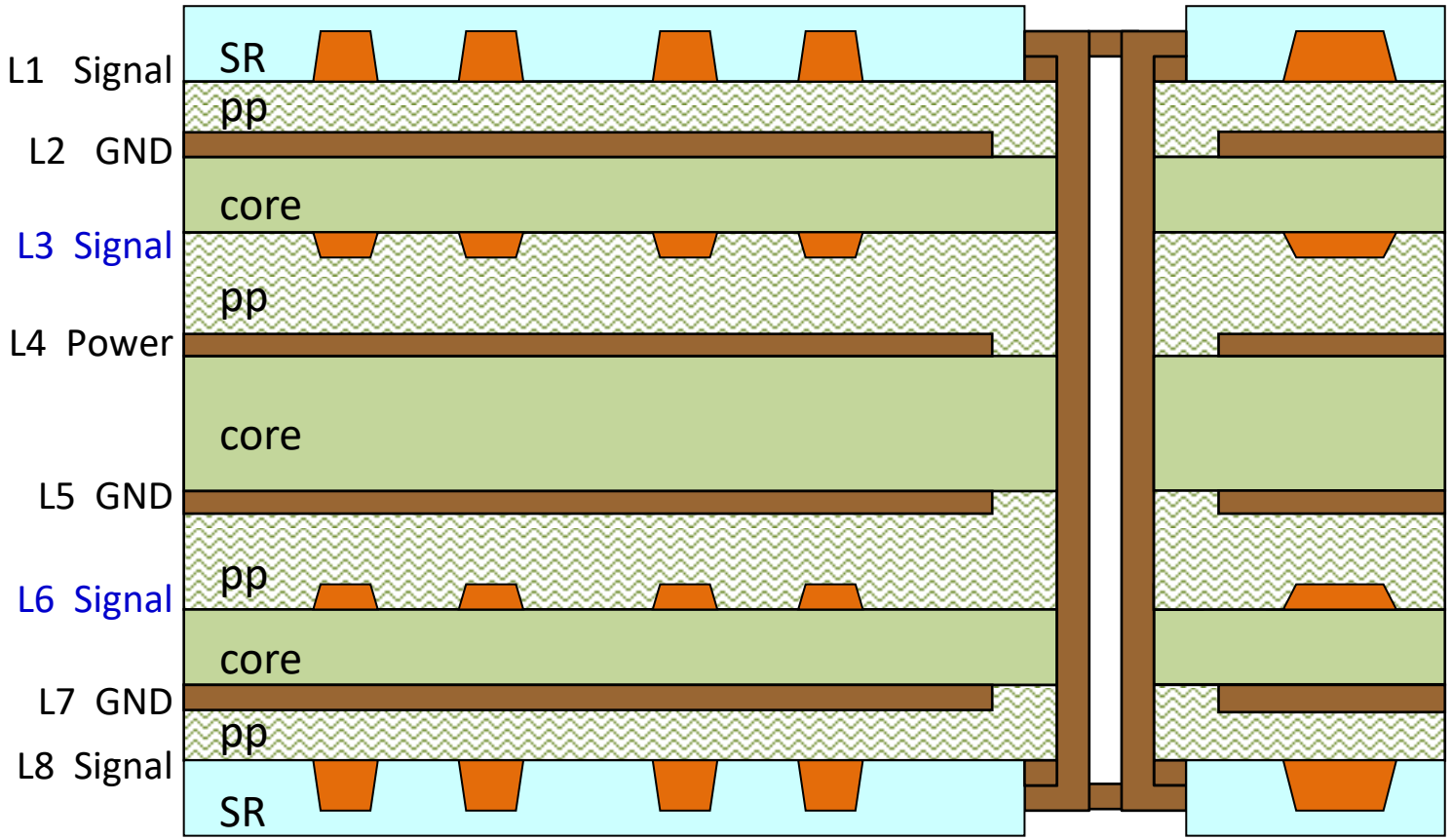
Topology of DQ



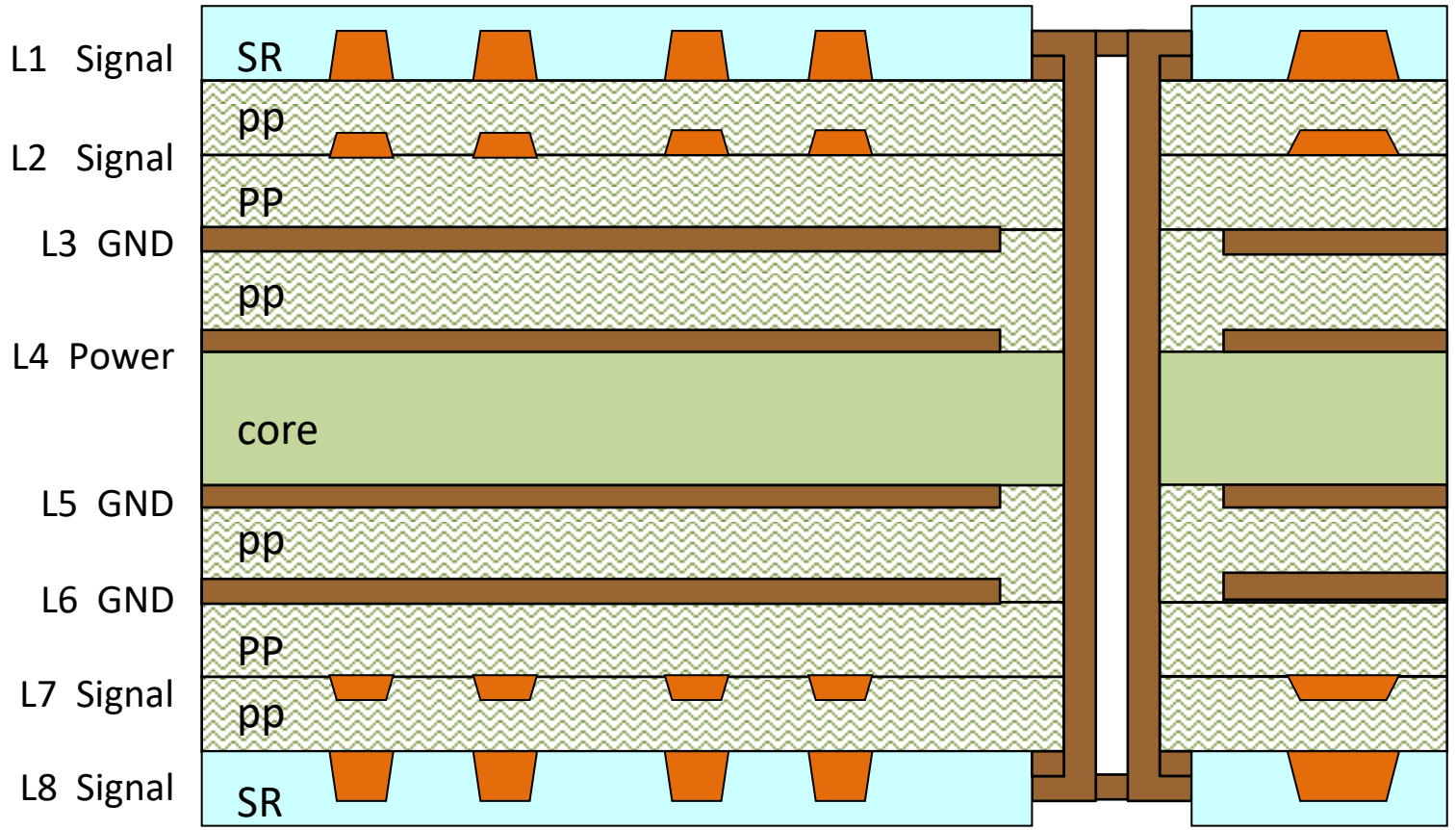
Case1: 10 Layers/Buildup (4-2-4/IVH)



Case2: 8 Layers/Through

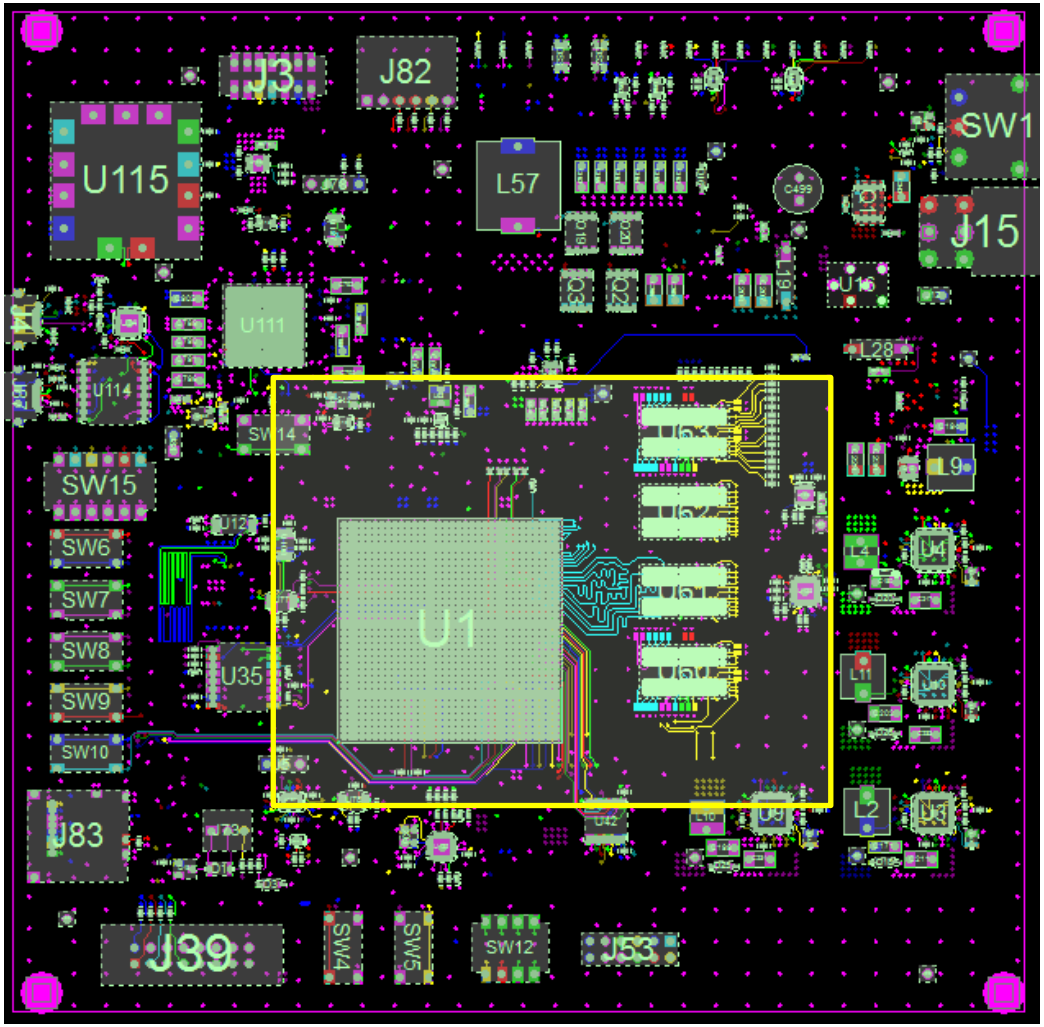


Case3: Buildup 10 Layers (4-2-4)



Case1: Trial Board

Top



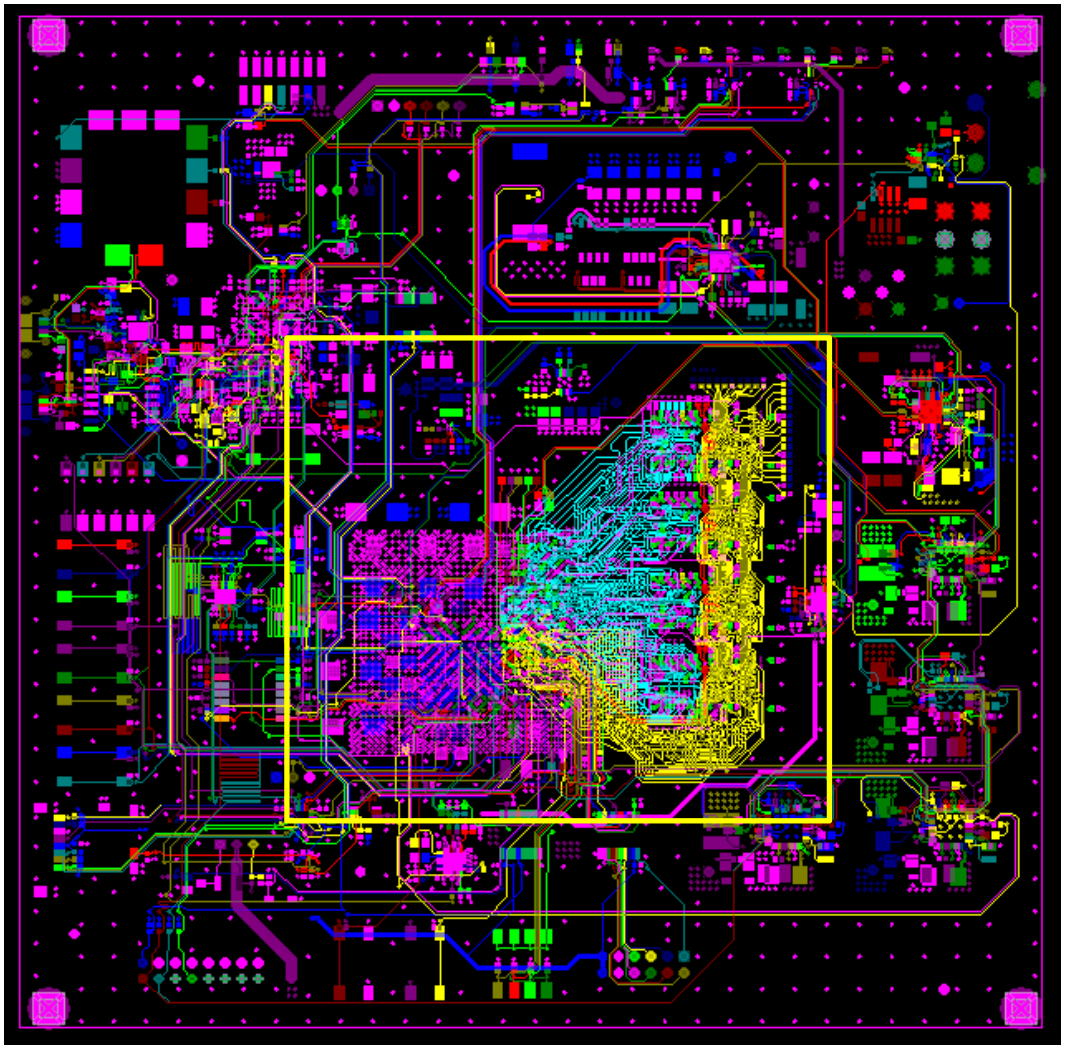
DDR4 x 4

U60, U61, U62, U62

Kintex UltraScale

U1

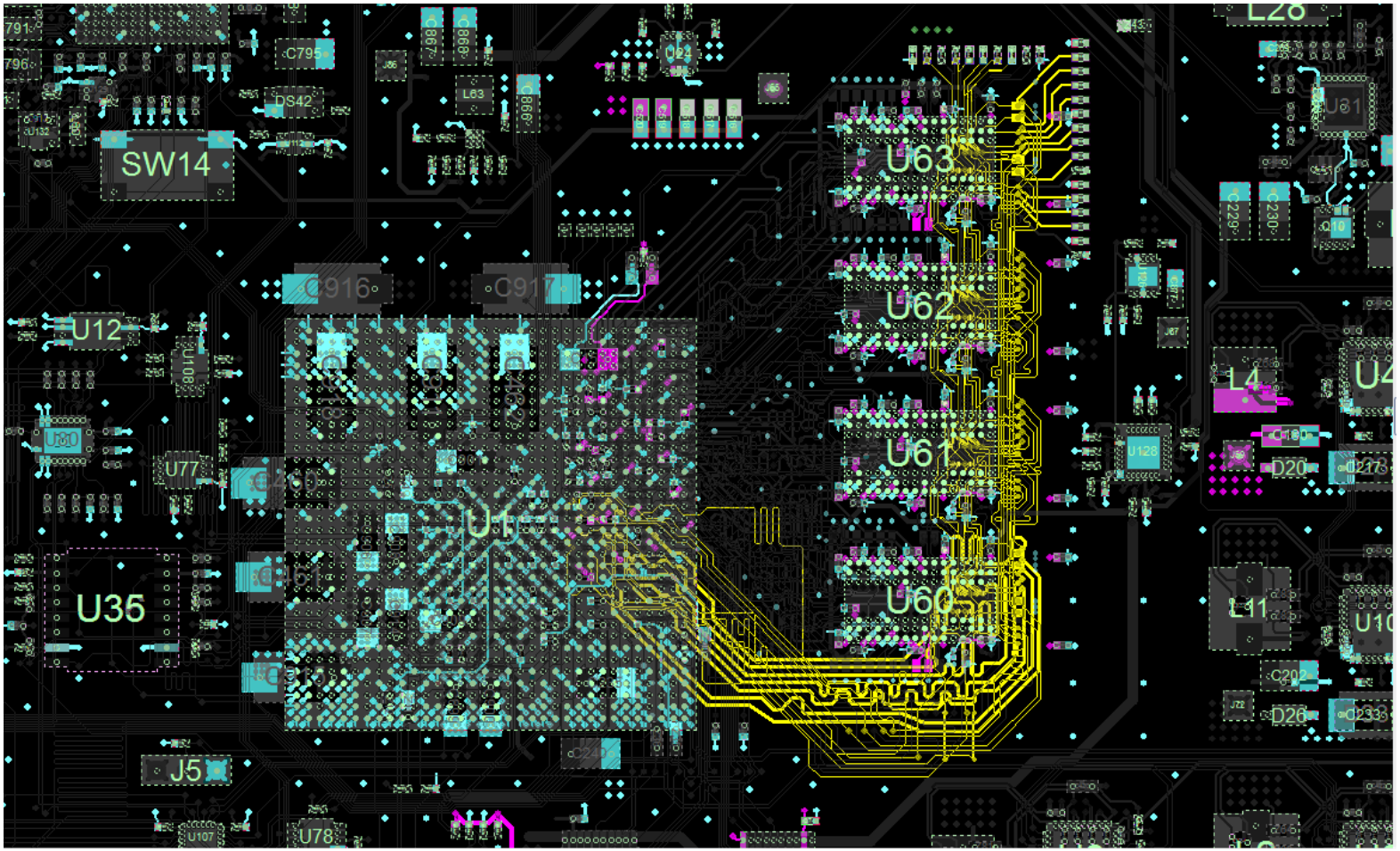
DDR4 all Signal



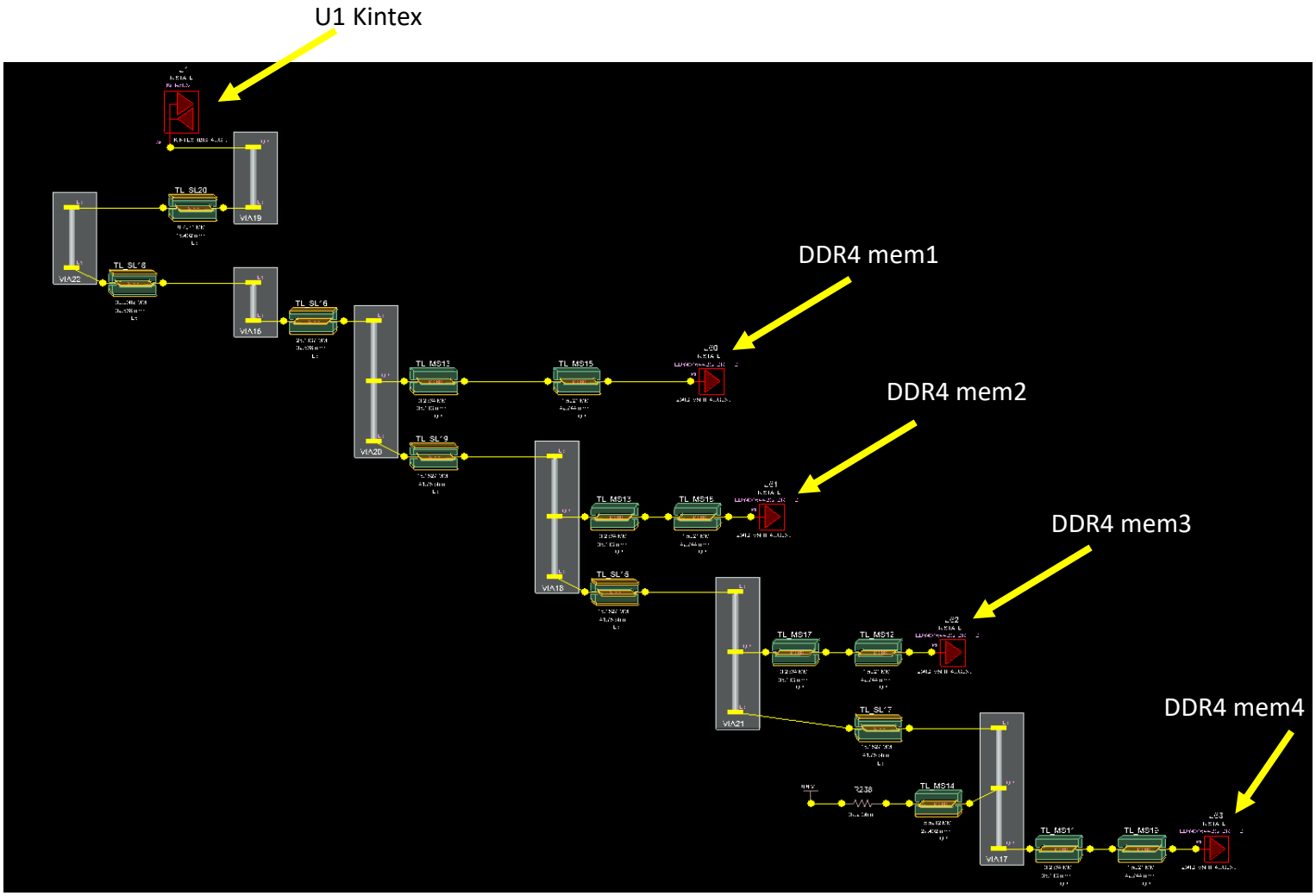
DDR4 Memory x 4
16bit x 4 = 64bit

Kintex UltraScale
Controller

Address Lines



Address Topology



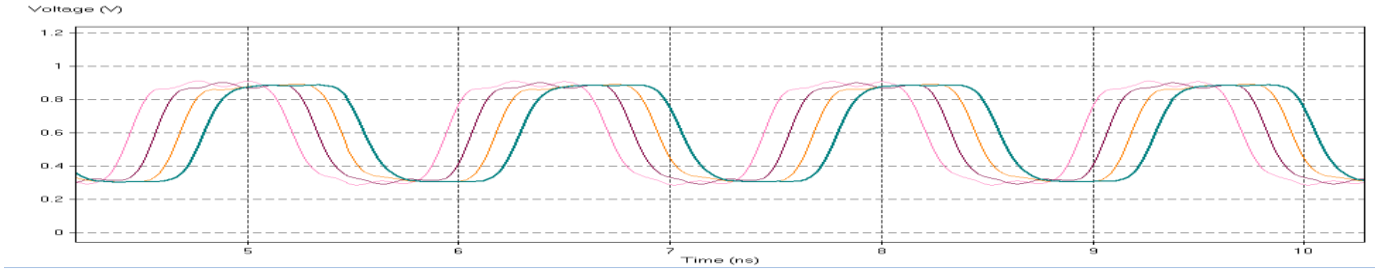
Package Delay

Delay_Max(pS)	Delay_Min(pS)	Length_Max(mm)	Length_Min(mm)
212.797	210.680	31.889	31.904
162.510	160.893	24.353	24.364
164.813	163.173	24.698	24.710
149.230	147.745	22.363	22.373
148.715	147.235	22.286	22.296
176.310	174.556	26.421	26.433
161.790	160.181	24.246	24.256
124.500	123.261	18.657	18.666
174.675	172.937	26.176	26.188
81.307	80.498	12.184	12.190
157.946	156.374	23.669	23.680
81.175	80.367	12.165	12.170
97.875	96.901	14.667	14.674
76.931	76.165	11.529	11.534
101.537	100.526	15.216	15.223

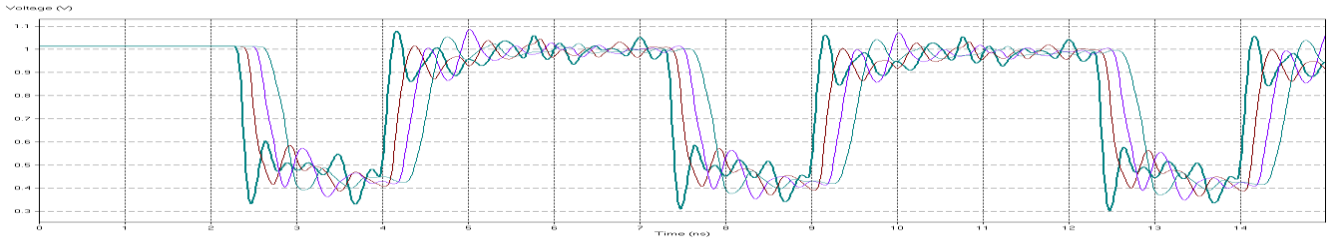
- Sample of Package Delay table is shown as above
  - longest is 31.889mm
  - Shortest is 11.529
  - Diff: 20.36mm = 135.8ps (6.67ps/mm)
- It's required to include PKG routing length at
  - board layout stage (matched timing)
  - IO selecting stage using SI simulation (skew investigation)

U60

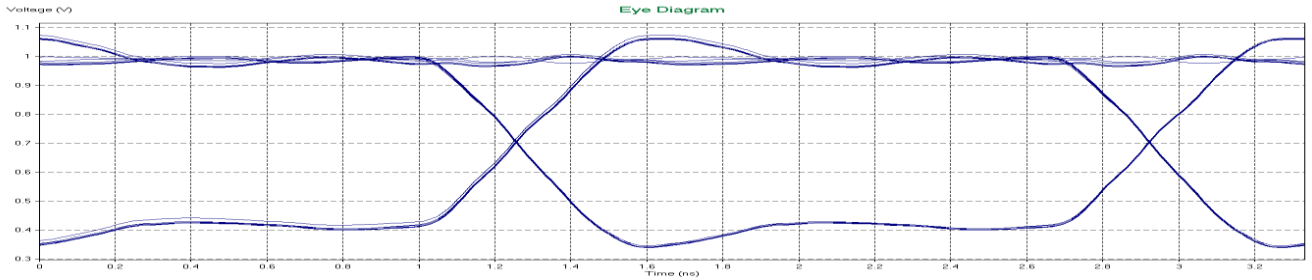
Address 0



Ideal Plane
at U60,U61,U62,U63

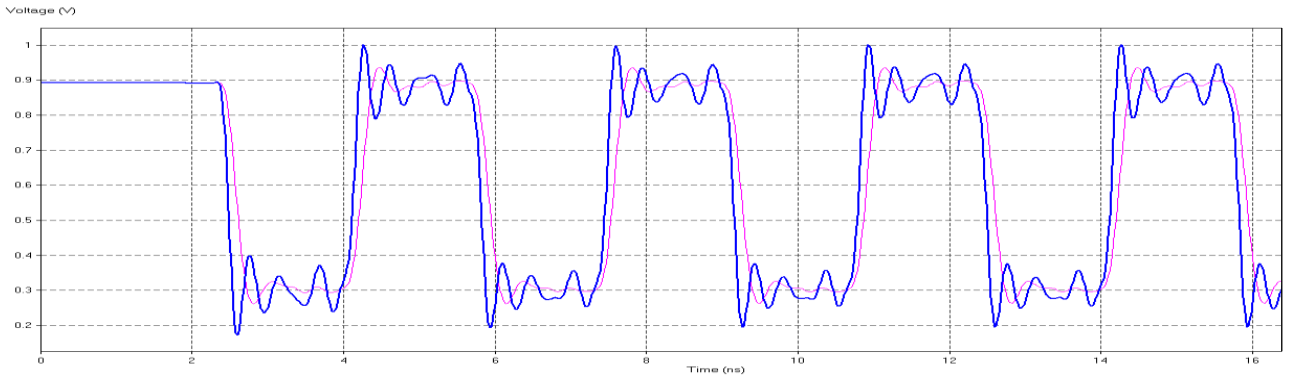


Plane model ON
On Die model Off
Pkg model Off



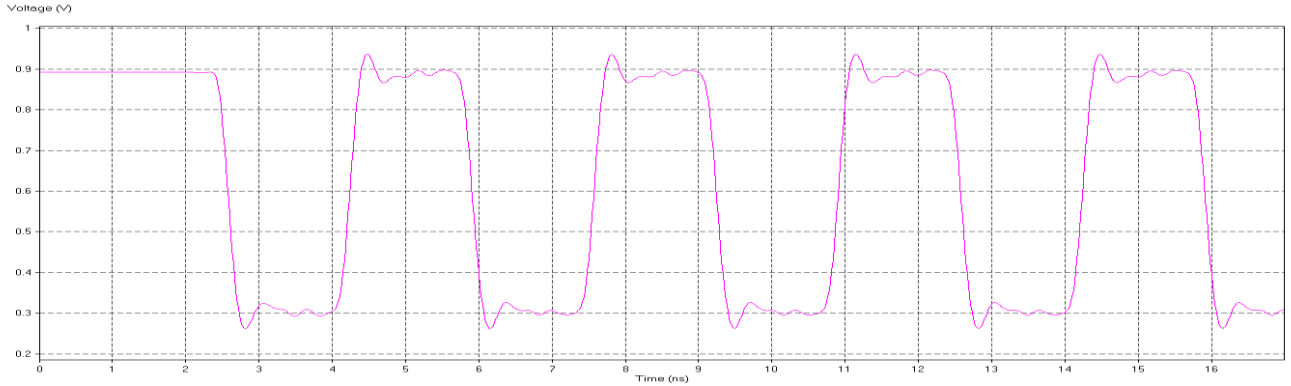
Address 10 at U63
On Die model ON
Pkg model Off

Address: On Die & Pkg model



On Die model Off

Pkg model Off

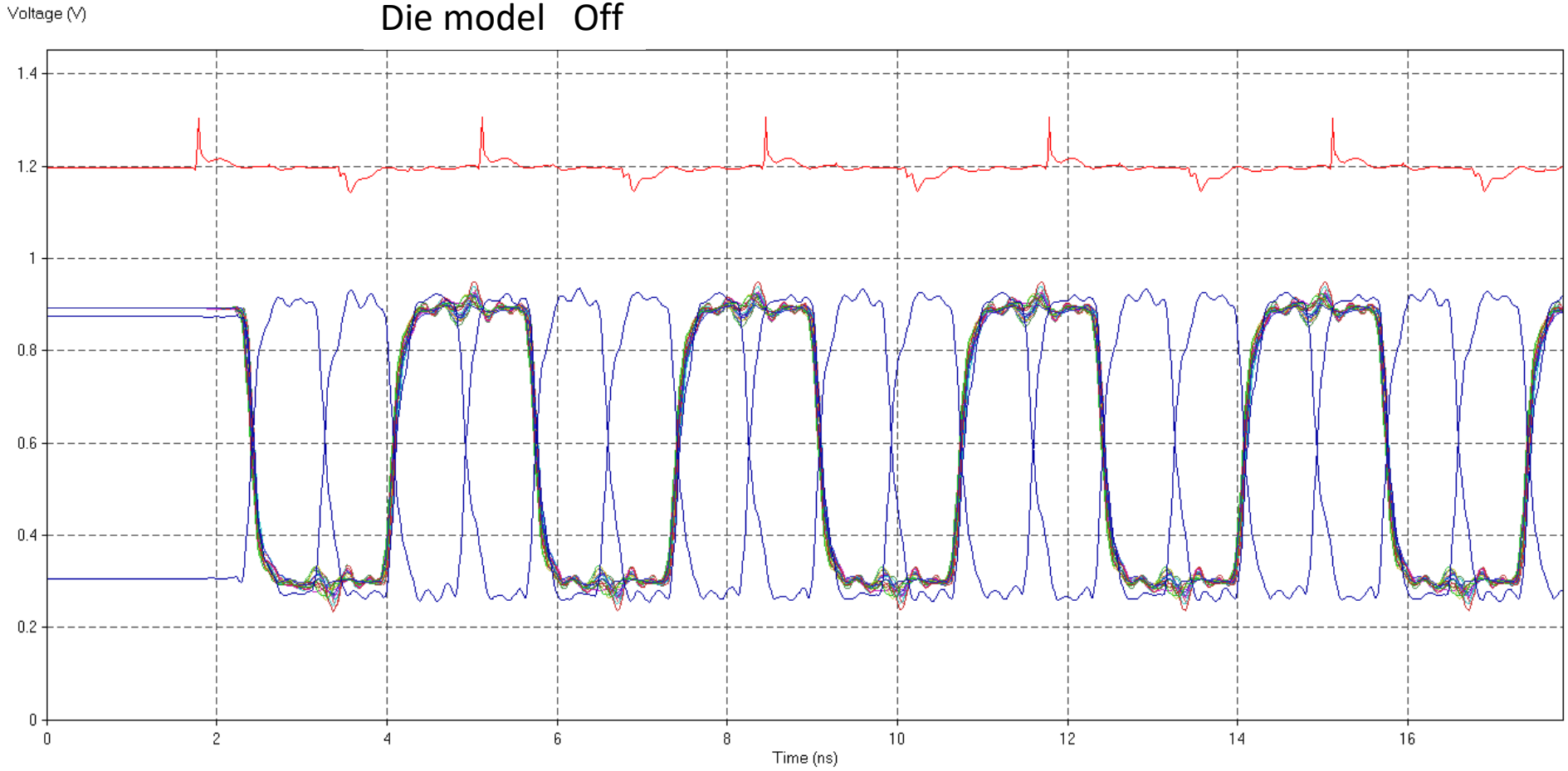


On Die model ON

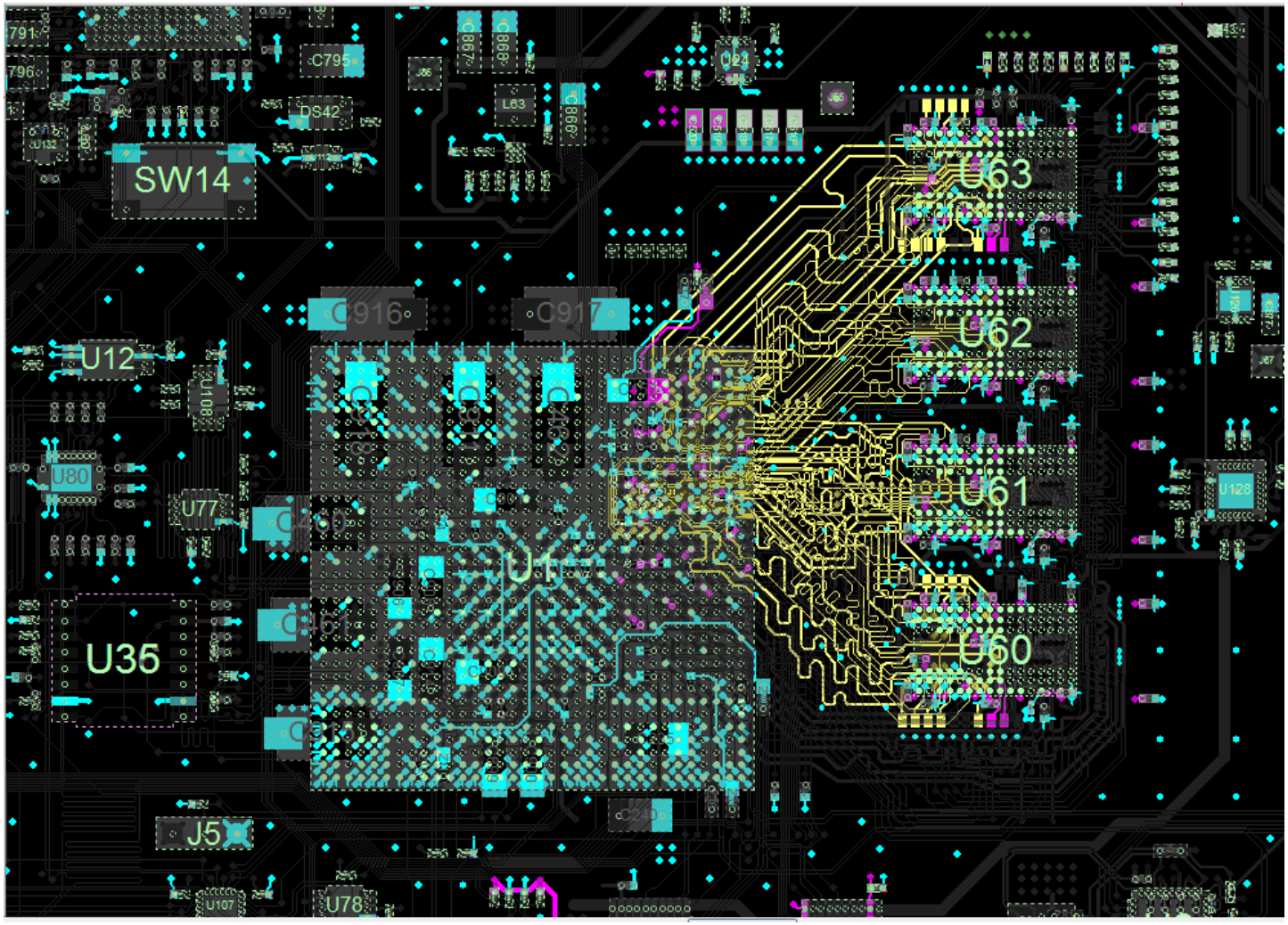
Pkg model ON

Address, Clock and Power

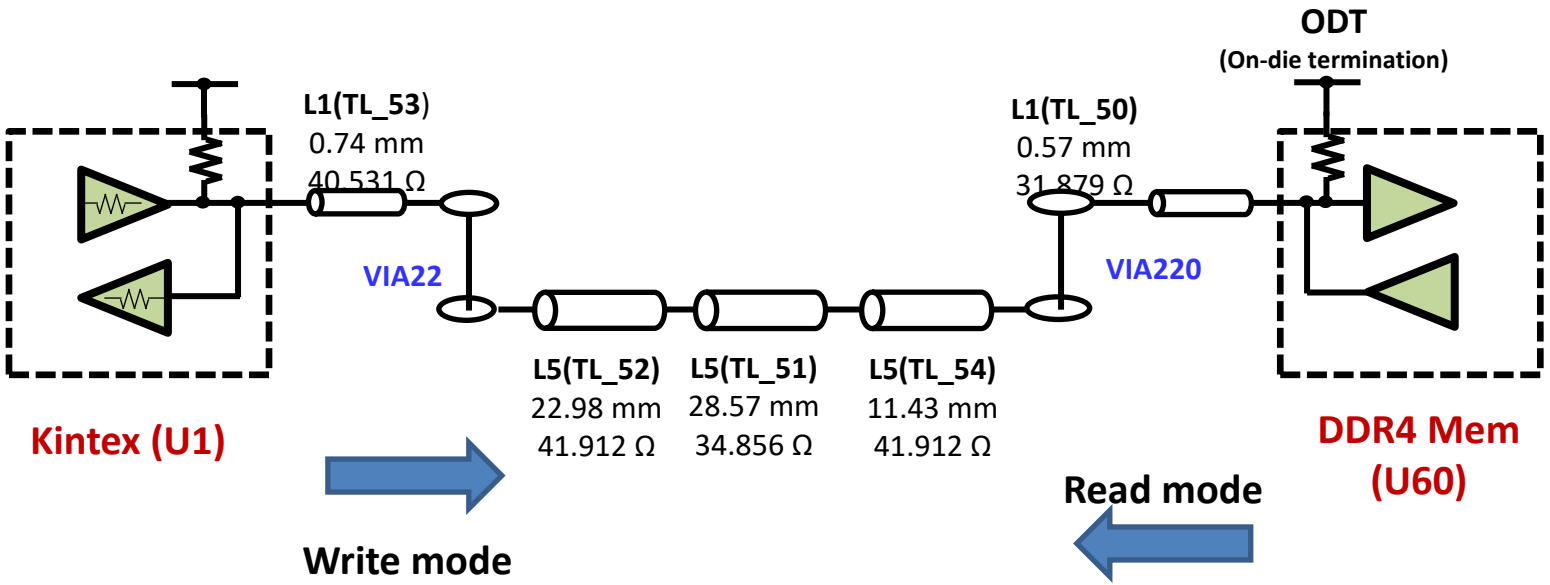
PKG model ON
Die model Off



DQ Lines


SW14
U63
U62
U61
U60
U12
U35
U80
U77
U78
J5
C916
C917
C795
DS42
L63

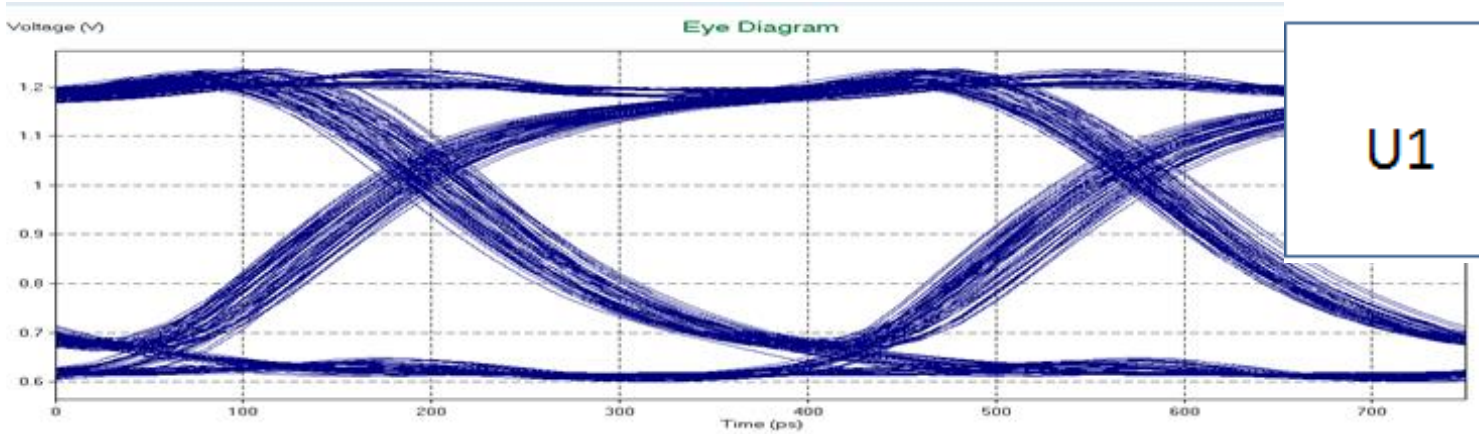
DQ0 Topology



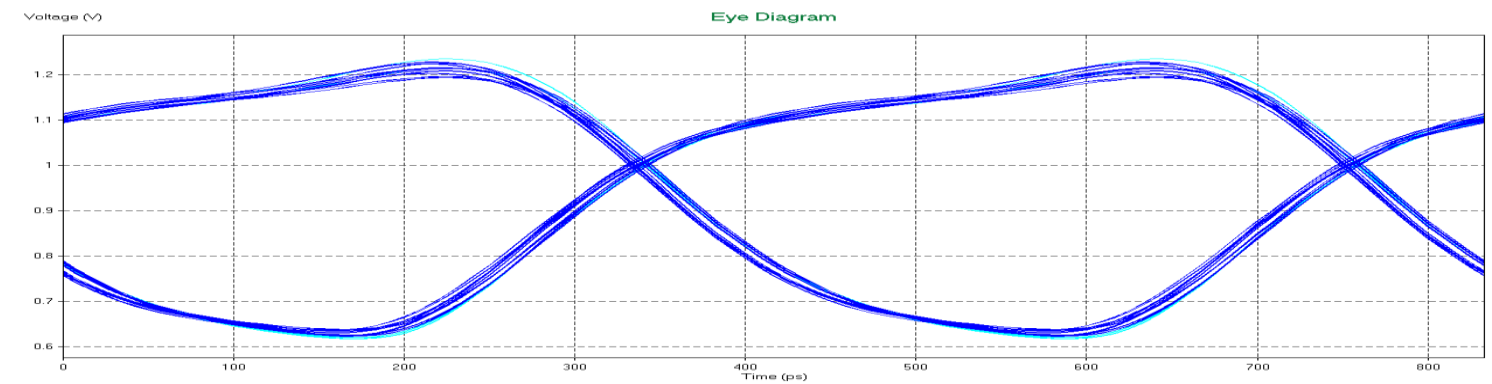
Simulation Results（DQ0-7,DM0)

ODT34Ω

Package model Off　(PCB delay only)

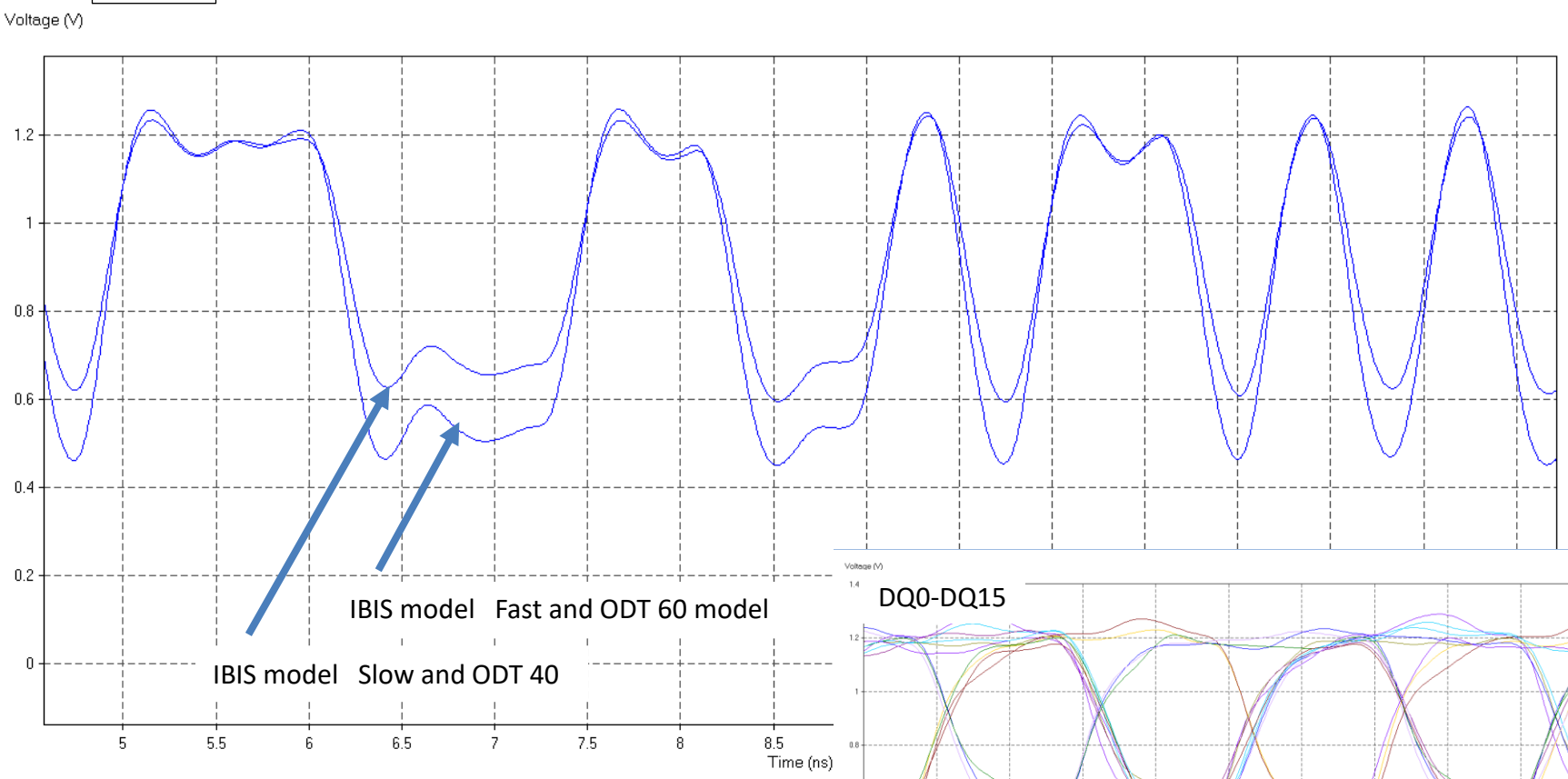


Package model ON　(Pkg skew should be added to PCB delay)



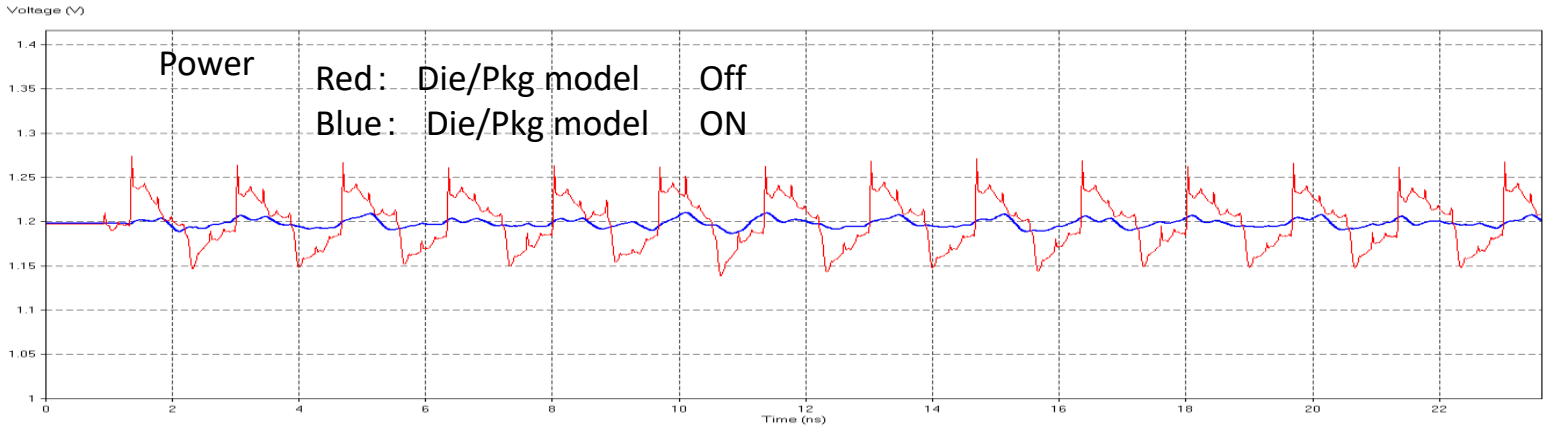
Different DQ0 Results Depend on IBIS Models

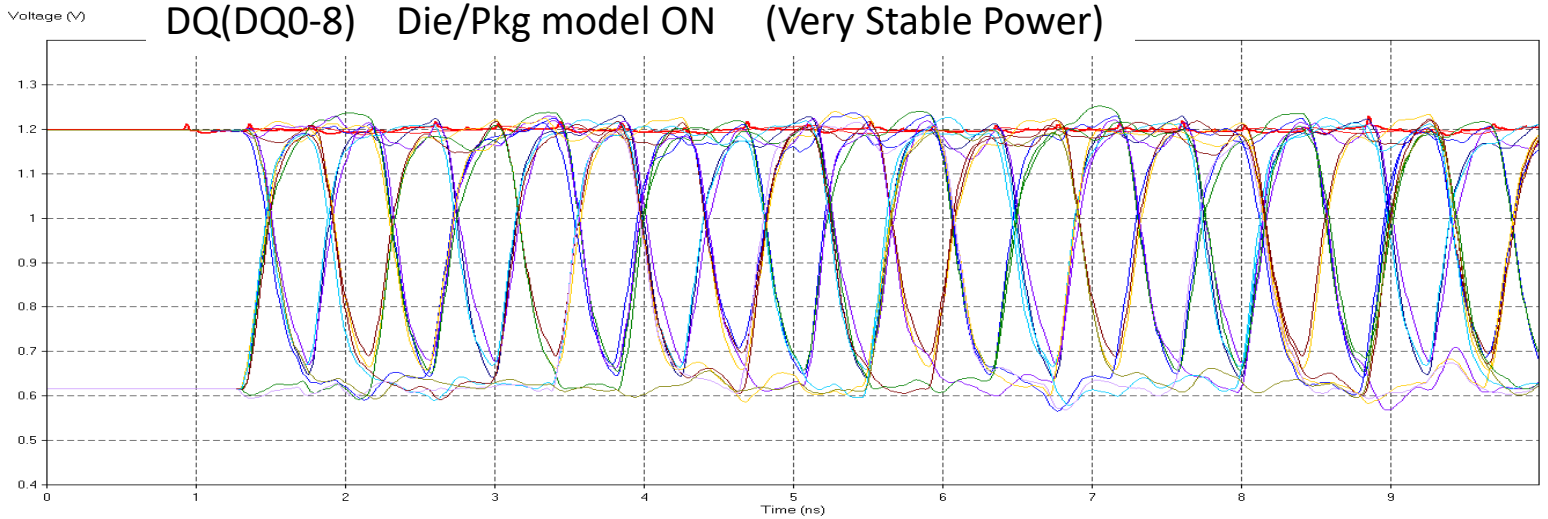
U60



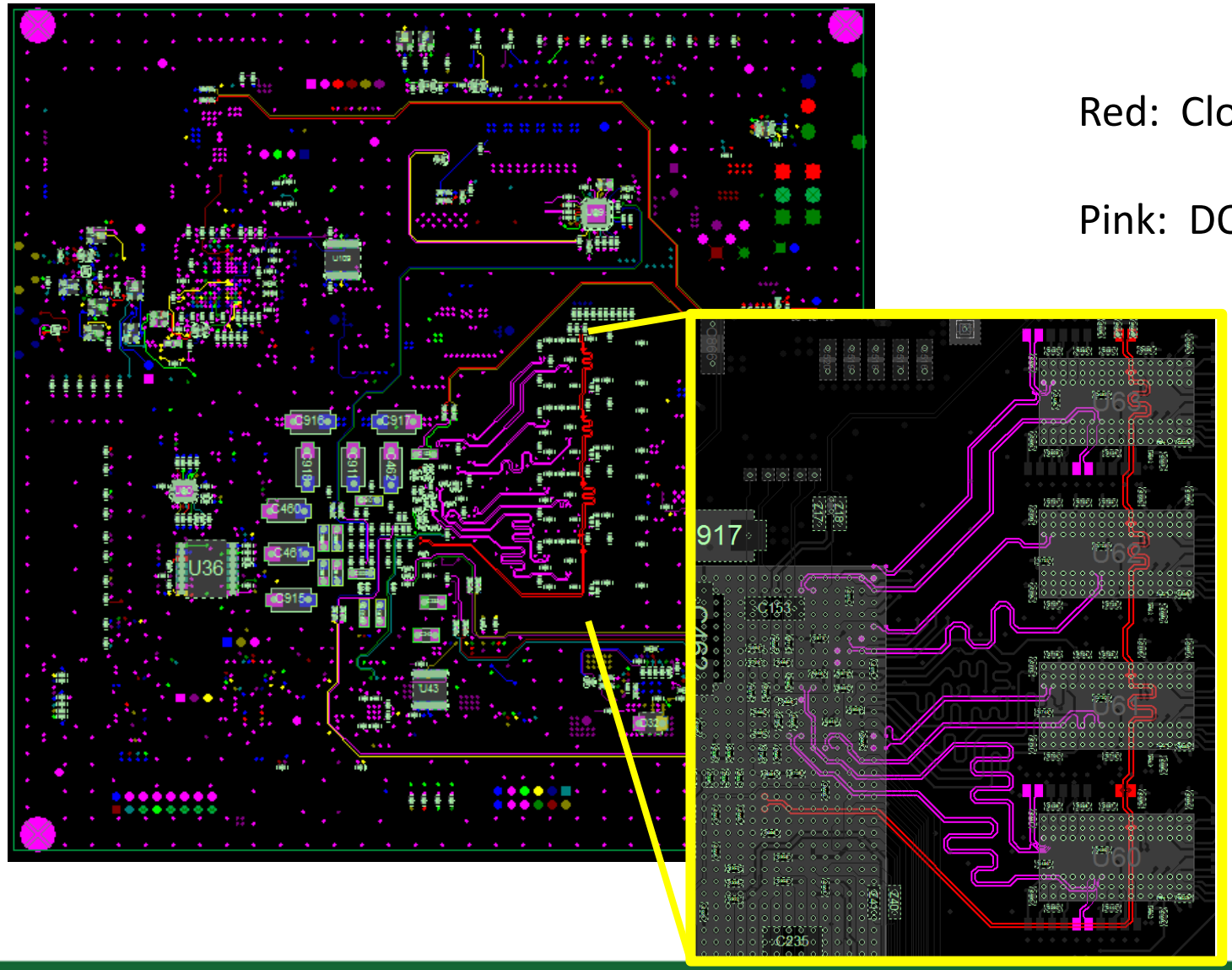
On-Die model ON
Pkg model Off

DQ: Die/Pkg Model





Bottom: Differential Signals

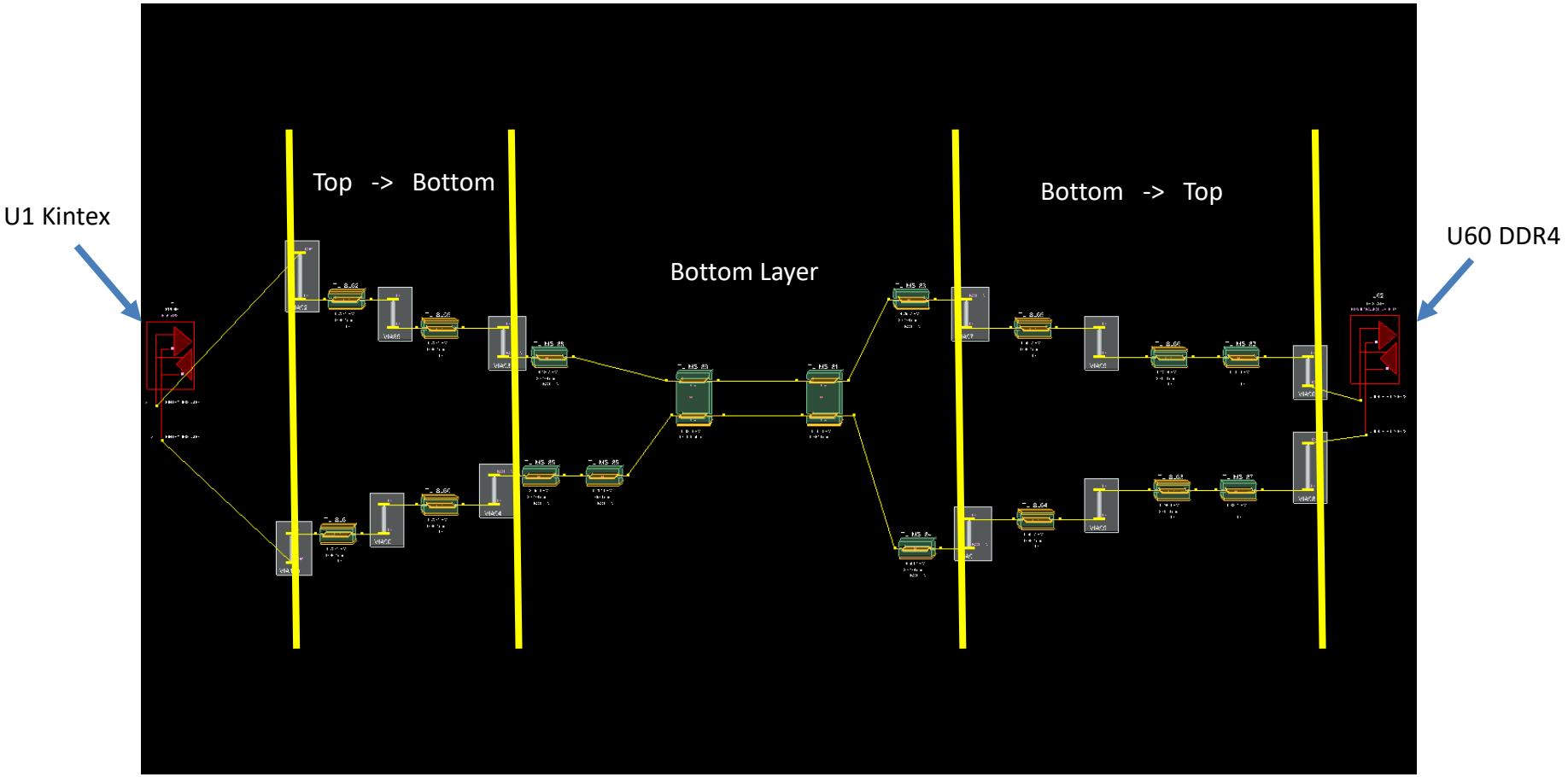


Red: Clock Line

Pink: DQS

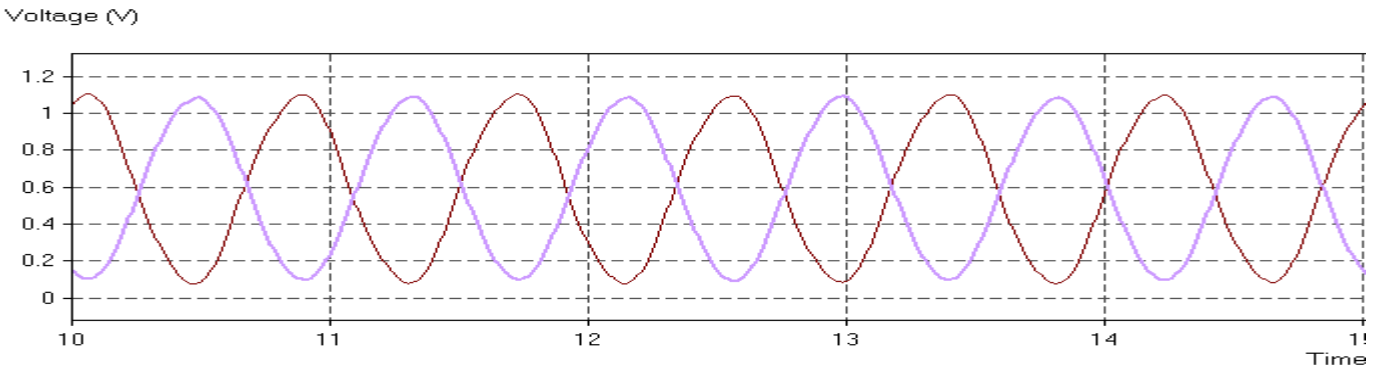
DQS Topology

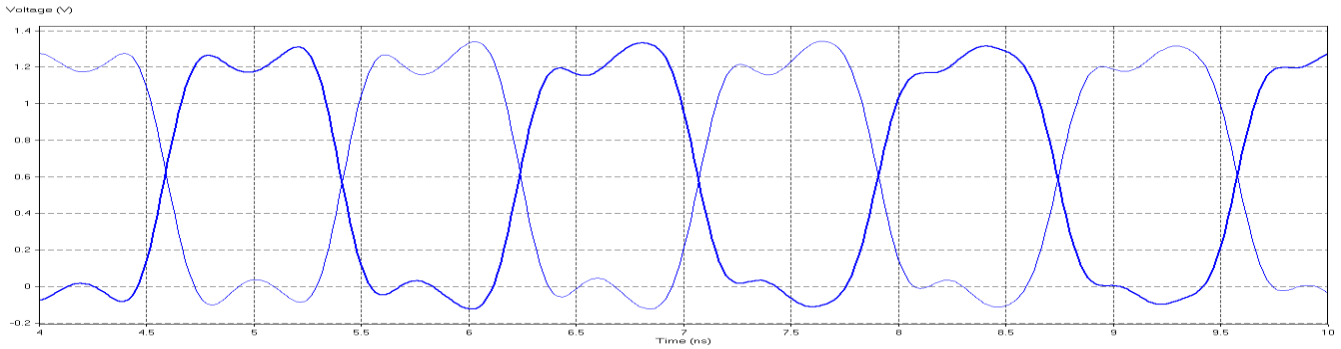
All Differential Signals are brorken out from Top Layer to Bottom Layer.



Clock, DQS

On-Die model ON
Pkg model Off

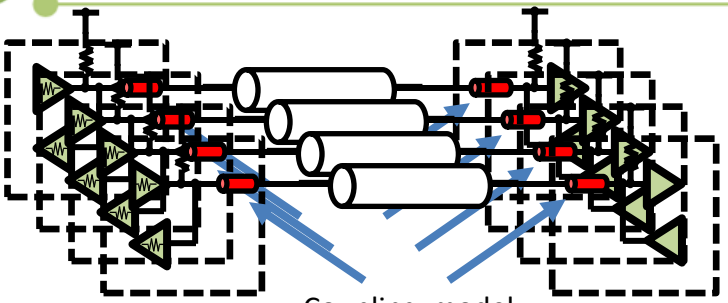




Z Impedance

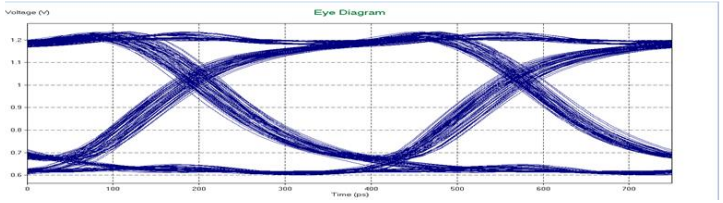
VDD1.2V　DDR4 Power Plane

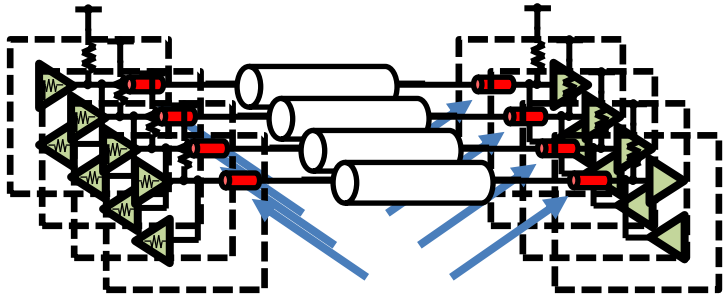
Coupling or Skew Analysis?



Coupling model

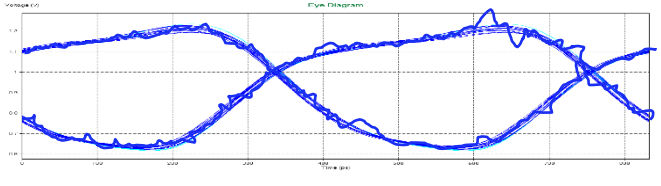
simulation

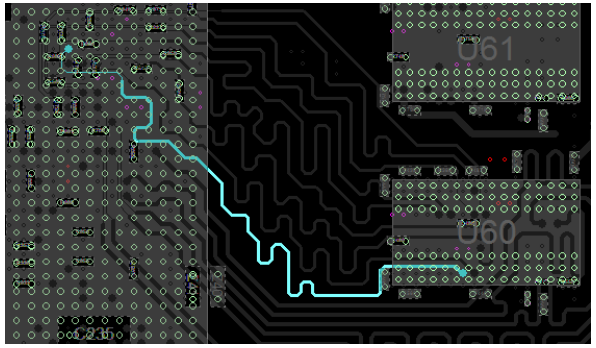




Package Skew per bit

simulation





Package length is required to add to:

1. PCB matched length routing
2. Pkg Skew investigation
3. Pkg model with coupling effect + Pkg delay simulation

Required Specification

- Pkg signal coupling simulation with Pkg skew effect is required for recent DDR4 bus simulation
- Current IBIS model:
  - Length could be added in to [Pin Numbers] section
  - Coupling model could be specified in [Define Package Model] section
  - ➢ But both coupling with length effect couldn't be allowed at one simulation.
  - ➢ Length should be specified in [Define Package Model]
    - ➢ [Length Matrix] Sparse_Matrix

      [Row] A1

      A1 8.7e-11 (unit Second)

END