Is Typical Analysis Enough? What Is Corner Condition?

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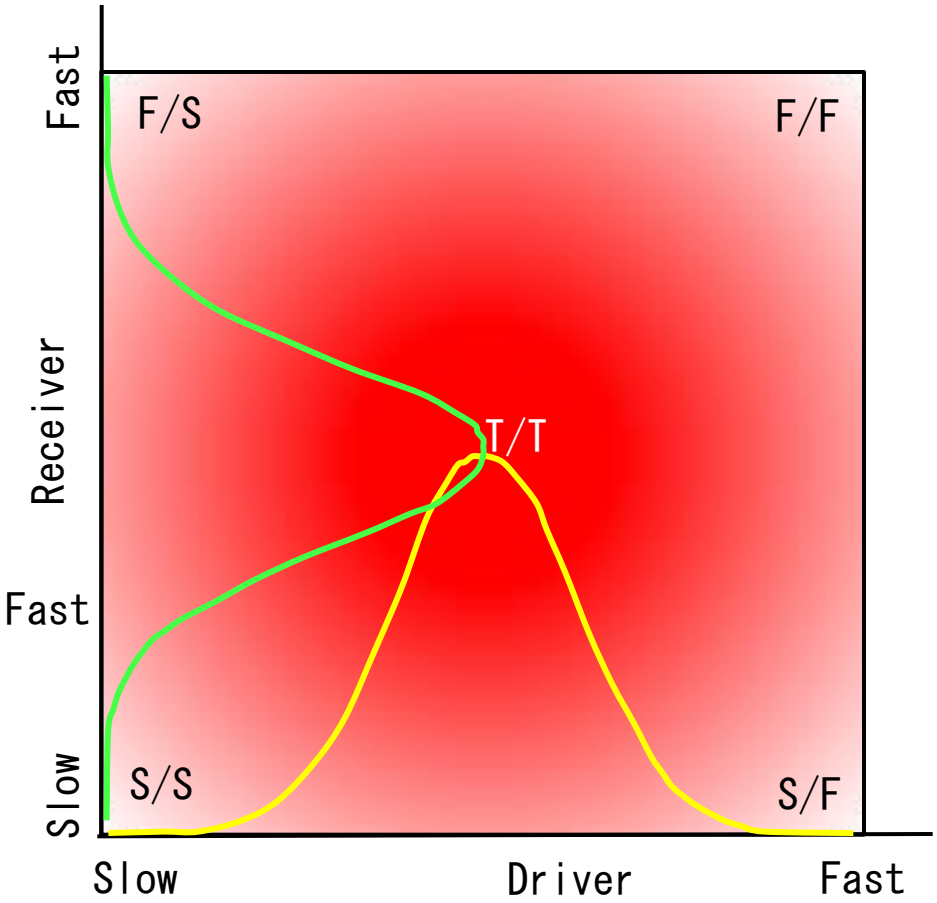
Outline

- Typical versus Worst Case
- Would Typical Analysis be enough?
- What would be the Worst Case?
- Would Worst Case Analysis be (necessary/required)?
- How to judge Sign-Off
- Concerns for IBIS-AMI

Tolerance of IC Characteristics

- Driver: Slow - Fast
- Receiver: Slow - Fast

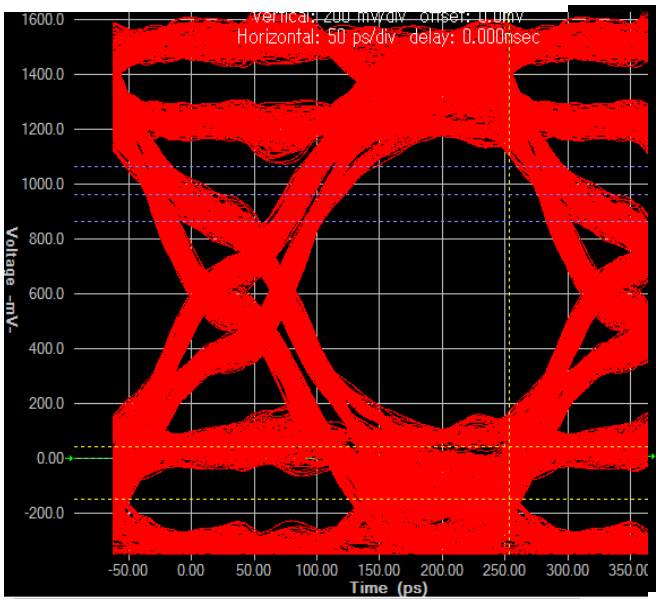


Typical Versus Corner

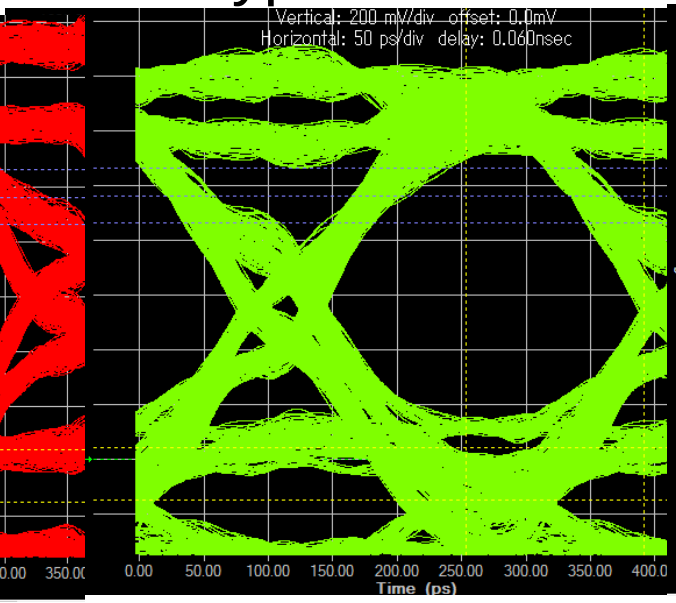
- IO Model
  - Fast/Typical/Slow
  - Driver: Output Impedance, Ramp
  - Receiver: Threshold Voltage
- C_Comp, Package L/C/R
- Vcc Voltage
  - +- 5% to 10% from Vtyp
- IC Temperature

Typical Versus Corner

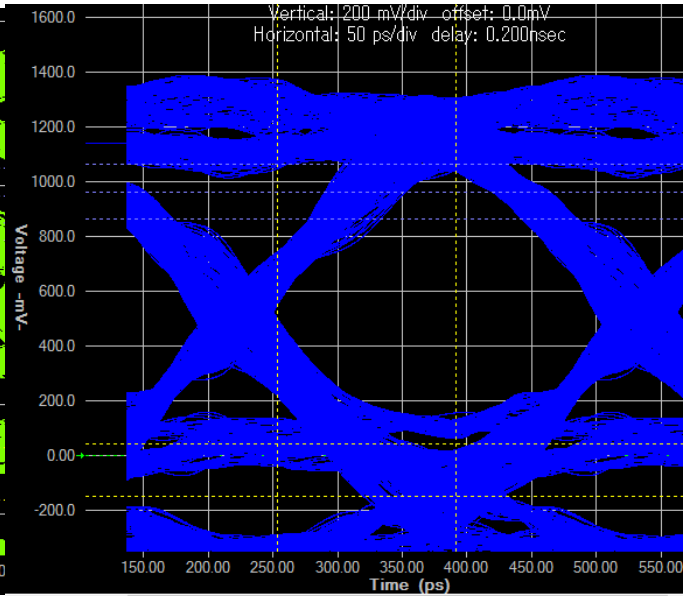
- Fast



Typ



Slow



- DDR4 2400
  - Driver: DQ
  - Receiver: DQ

Corner of IBIS

- Package Model

```
[Package]
|              typ          min          max
R_pkg          414.33m       389.21m      442.82m
L_pkg          1.95nH        1.49nH       2.26nH
C_pkg          0.43pF        0.35pF       0.80pF
|
[Pin]          signal_name   model_name   R_pin        L_pin        C_pin
A1             VDD           POWER
A2             VSSQ          GND
A3             NF            NF_INPUT     392.29m      1.53nH       0.43pF
A7             NF            NF_INPUT     439.07m      1.75nH       0.48pF


[Diff Pin] inv_pin vdiff   tdelay_typ        tdelay_min        tdelay_max
|
3    4             150mV    -1ns              0ns               -2ns
```

Corner of IBIS

- IO Model

```
|                                typ                 min                 max
|
|C_comp                          0.920pF             0.870pF             0.970pF
C_comp_pullup                    0.4600pF            0.4350pF            0.4850pF
C_comp_pulldown                  0.4600pF            0.4350pF            0.4850pF
|
[Model Spec]
| Timing spec test load voltage corners
Vref                             1.2000V             1.1400V             1.2600V
|
```

Corner of IBIS

- IO Model (I-V)

```
[Pulldown]
|
|    Voltage            I(typ)              I(min)              I(max)
|
     -1.20000000E+00    -2.37454740E-02     -2.68204090E-02     -2.14946320E-02
     -1.06548000E+00    -2.28772684E-02     -2.64700110E-02     -2.06319538E-02
```

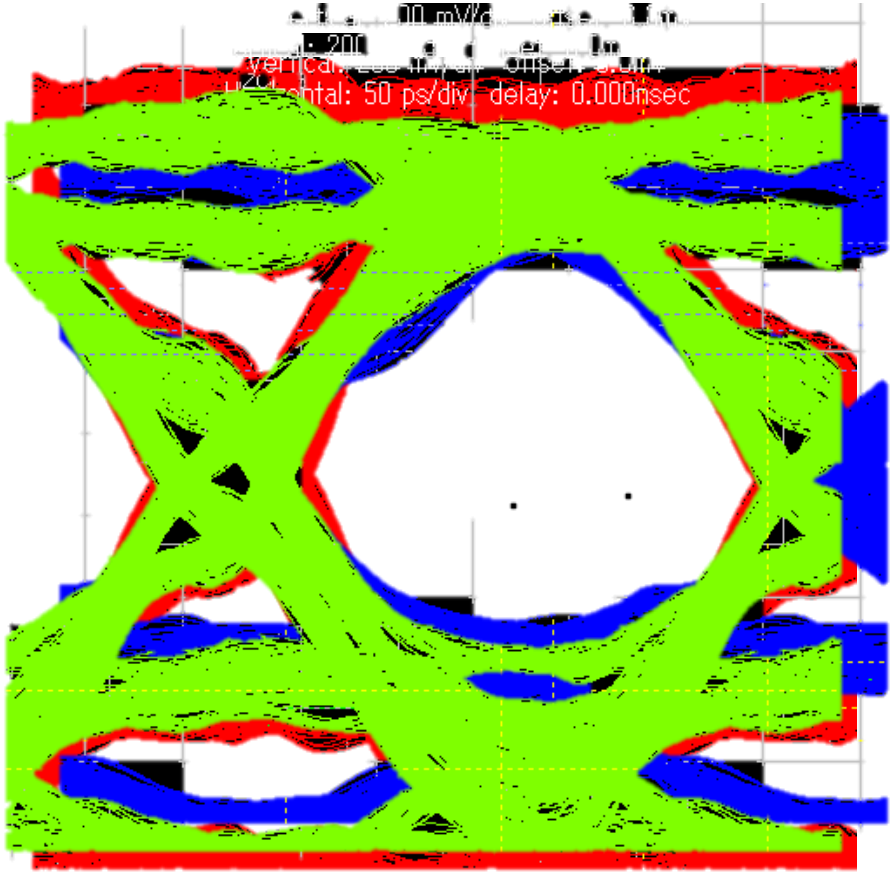
Corner of IBIS

- IO Model (V-T)

```
[Ramp]
R_load = 50
|          typ                          min                          max
dV/dt_r 4.1235E-01/6.4489E-11    3.8046E-01/8.4106E-11    4.4653E-01/5.2562E-11
dV/dt_f 4.5987E-01/6.2372E-11    4.3947E-01/7.9203E-11    4.6741E-01/4.9982E-11
|**************************************************************************
[Falling Waveform]
V_fixture = 1.2V
V_fixture_min = 1.14V
V_fixture_max = 1.26V
R_fixture = 50Ohm
C_fixture = 0F
|
|    Time                V(typ)              V(min)              V(max)
     0.00000000E+00      1.19999848E+00      1.13999700E+00      1.25999947E+00
     5.00000000E-12      1.19999849E+00      1.13999700E+00      1.25999948E+00
     1.00000000E-11      1.19999849E+00      1.13999700E+00      1.25999948E+00
```

Typical Versus Corner

Fast Typ Slow



Corner Setting

- Comment in IBIS Model

```
|
|Corner Settings
The corner settings:
Model Type       Temp   VCCIO    VCCINT    Process corner
|
1.2V LVTTL/LVCMOS
Typical          25C    1.2V     1.1V      Nominal
Minimum          85C    1.14V    1.05V     Slow
Maximum          0C     1.26V    1.15V     Fast
|
1.5V LVTTL/LVCMOS
Typical          25C    1.5V     1.1V      Nominal
Minimum          85C    1.425V   1.05V     Slow
Maximum          0C     1.575V   1.15V     Fast
```

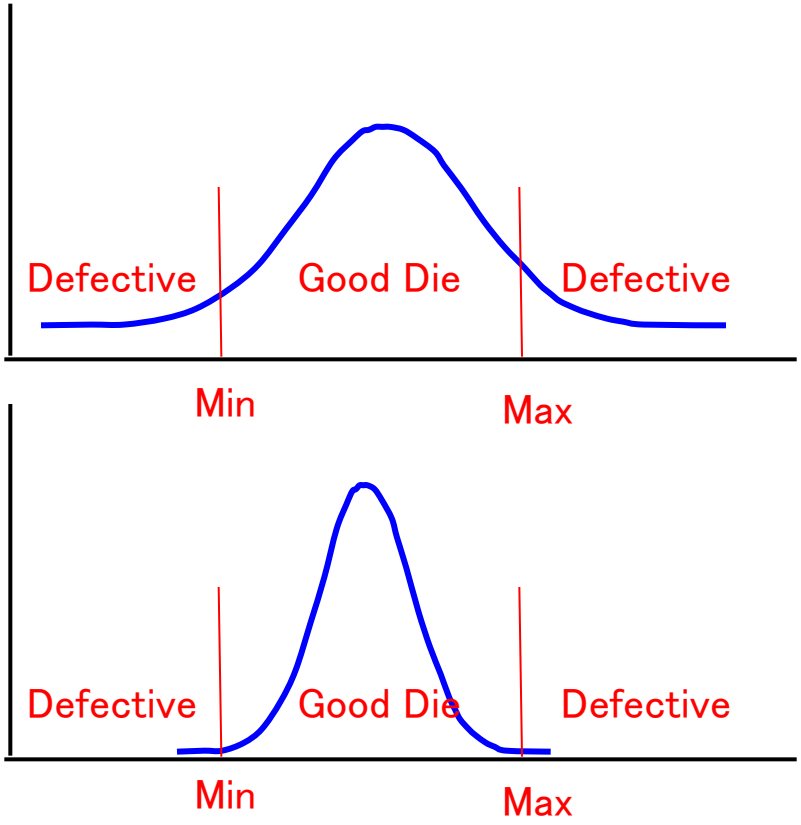
Yield Ratio of IC

- New Technology, Sample Shipment
  - 40~60% ?
- Early Lot
  - 50~80%
- Mass Production
  - 80%~

- Cause of Failure
  - Lattice Defect
    - Die Size
  - Process Error Rate
    - Fast/Slow

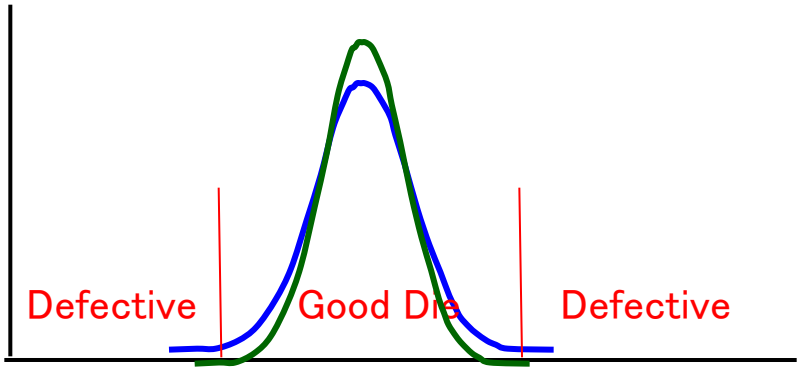
Proficiency of Process

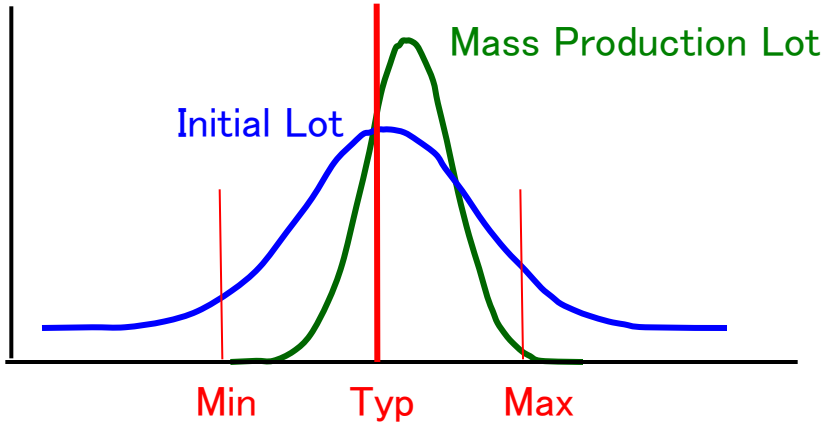
- Improve Yield Rate
  - Early Lot
  - Mass Production Lot
- Use Same IBIS Model



Typical Volume Characteristics?

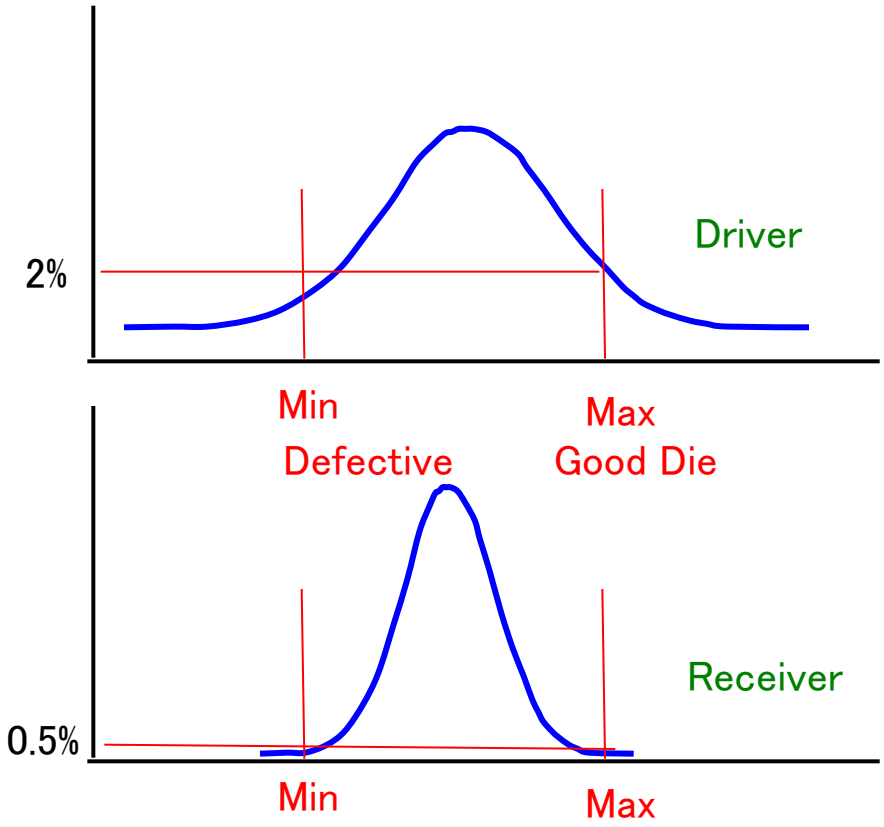
- How Differ from Early Lot and Mass Production Lot ?
  - Tune-up the Process to Increase Yield Rate
- Requires Real Characteristics Curve





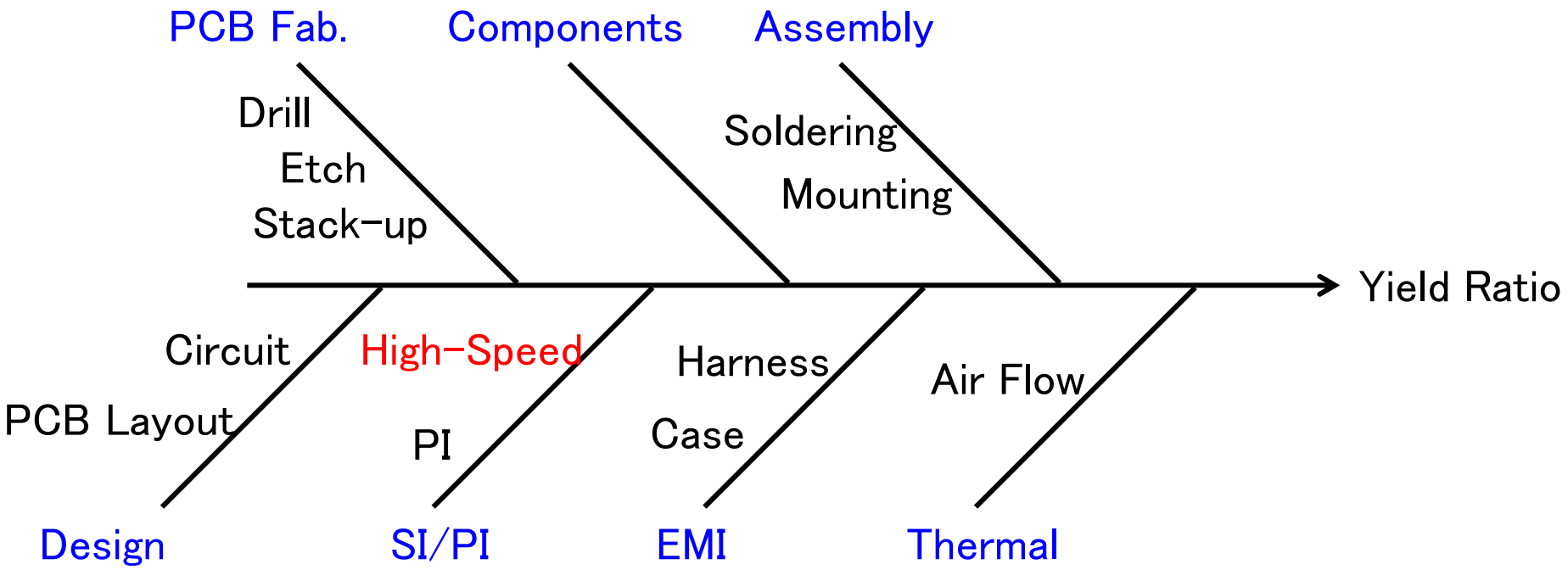
Very Few FF/SS Case

- When Driver's Fast Rate=2%, Receiver's Fast Rate=0.5%
  - FF Rate = 0.01%



Elements of PCB Error

- Many Factors for Error
  - Fix the Effective Factor First
  - What is the Most Effective Source?
- What % Error is Acceptable for SI Reliability?



Conclusion

- Typical Analysis is not Sign-off Analysis
- Corner Analysis is necessary for Sign-off
- In some case, Corner Analysis is Over Design
- If the Corner Analysis can be performed with minor change, those changes should be made.
- If the Corner Analysis by major design change and increased cost, these changes need to be reviewed.
- IC's Yield rate, Fast/Slow rate is unknown
  - IC Fabrication details are confidential.
- Know-how
  - Correlation between Simulation and Measurement
  - Analyze PCB Fab. Error Rate and Error Factors