

Meeting Date: November 18, 2016

Meeting Location: Tokyo, Japan

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Aurora System	Dian Yang
Avant Technology	Jyam Huang, Chloe Yang
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Lattice Semiconductor	Dinn Tran, Maryam Shandazi
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	John Lin, Alan Sun
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	Jie Pan, Weizne Li, Liang Wu, BL Qian, Fang LV
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Toshiba Information Systems Corp.	Yasuyuki Inaba*, Satoshi Yamaguchi*, Masashi Hirai*
Toshiba Memory Systems Co.	Kanehara Kenichi*, Kouichi Ookawa*
Toshiba Microelectronics Corp.	Jyunya Masumi*
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VIA Technologies	Terence Hsieh, Jerry Hsu, Justin Hsu
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Zhejiang Uniview Technologies	Weiqi Chen, Jiayun Dai

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
December 2, 2016	628 078 024	IBISfriday11

For teleconference dial-in information, use the password at the following website:

https://sae.webex.com/sae/j.php?MTID=m0a07ee0ddc25e28af96b4bbad3c17f4b

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Asian IBIS Summit took place on Friday, November 18, 2016 at the Akihabara UDX building in Tokyo. About 106 people representing 69 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/nov16c/

Shogo Fujimori (Fujitsu Advanced Technologies and JEITA IBIS Promotion Working Group Chair) welcomed everyone and explained the meeting agenda and logistics.

Mike LaBonte welcomed participants on behalf of the IBIS Open Forum and convened the meeting, noting that only technical presentations would be on the agenda, and there would be no voting.

Mike continued by thanking the co-sponsors: the major organizational sponsors JEITA and the IBIS Open Forum and also the co-sponsors ANSYS, Cadence Design Systems, Cybernet Systems, Keysight Technologies, Mentor Graphics Corporation, MoDeCH, Toshiba Corporation and Zuken.

IBIS CHAIR'S REPORT

Mike LaBonte (Signal Integrity Software (SiSoft), USA)

Mike LaBonte presented updates on work in progress in the ATM, Interconnect and Quality task groups. This includes an IBIS 6.2 release, backchannel support, C_comp model enhancements, redriver flow enhancements, and an interconnect modeling BIRD. Several BIRDs have been approved for IBIS 6.2 while some are still in progress. The IBIS Open Forum has 22 members and regular teleconference and Summit meetings. The China regional forum is a new group affiliated with IBIS.

IBIS PROMOTION WORKING GROUP REPORT

Shogo Fujimori (Fujitsu Advanced Technologies, Japan)

Shogo Fujimori showed the location of the IBIS Promotion Working Group within the JEITA/EC Center committee organization. The objective of the working group is to promote IBIS simulation. Activities include defining IBIS simulation procedure guidelines, hosting an IBIS seminar, helping with logistics of the IBIS Summit in Japan and maintain IBIS quality documents. The group hosted an IBIS basics seminar in June 2016 and an IBIS-AMI seminar before the IBIS Summit. Surveys of the seminar attendees show that experienced engineers are interested in IBIS-AMI, a lot of beginners attended the IBIS basic seminar, one third of attendees use IBIS-AMI models, experienced engineers resolve issues in cooperation with EDA and/or device vendors, and model availability is still a major problem.

DIFFERENTIAL MODELING FLOW WITH SERIES MODEL IN VERILOG-A

Wei-hsing Huang* and Sanjeev Gupta** (*SPISim, USA and **Sigintegrity Solutions, India)

Wei-hsing Huang presented. Half/true differential buffers are modeled including a series model for the effects of differential current and differential capacitance. The rigid syntax of the series

model can lead to many inaccuracies. Replacing the series model with a Verilog-A model using [External Model] syntax streamlines the modeling flow, improves V-T extraction accuracies, and removes the rigid series model syntax. A modeling flow for creating the Verilog-A model was presented.

IS TYPICAL ANALYSIS ENOUGH? WHAT IS CORNER CONDITION?

Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda presented an overview of typical conditions versus corner conditions of IO models including the affected keywords in IBIS. He noted that the yields of ICs change between early silicon and mass production. Process characteristics may also shift during the same timeframe. He also noted there are very few fast and slow process cases. He concluded that typical analysis is not enough for sign-off analysis, which requires analysis of corners. In some cases, corner analysis results in over design. If corner analysis shows the need for minor changes in the system design, those changes should be made. If corner analysis shows the need for minor design changes and increased costs, those changes should be reviewed. Fast/slow process yield rates are usually unknown since the fabrication details are confidential. Seeing correlation between simulation and measurement is useful, and so is analyzing PCB fabrication error rates and error factors.

Shogo Fujimori said there are very few cases in which the voltage is different between the driver and the receiver in an actual PCB. However, in the IBIS format the power supply voltage also differs with min, max and typ. He asked if these constraints on the IBIS format also make corner analysis difficult. Maeda-san answered that there are voltage differences between each pin due to IR drop. Therefore, corner analysis is necessary.

EMBEDDED DDR4 DESIGN SIMULATION

Yukio Masuko* and Shinichi Maeda** (*Japan Electronics Packaging and Circuit Association, **KEI Systems, Japan)

Yukio Masuko introduced the Japan Electronics Packaging and Circuit Association (JPCA). The JPCA Design Academy provides simulation support for members and translates the latest standards into Japanese. Masuko-san detailed a DDR4 design project that started with an ASIC vendor's reference design. Three new PCBs were designed using different stackups, and design guides are in development. Details of the three designs were shown as well as simulation results for Address/Command, Clock and Data signals. Masuko-san noted that simulation including package coupling to show package skew effects is required for DDR4 bus analysis. A matrix of package trace electrical lengths would be useful to add to [Define Package Model].

Yu Yamada asked if 64 DDR4 bits must be simulated for a worst case power aware simulation. Shinichi Maeda replied that 32 bits are sufficient, because DDR4 has an invert output feature, so the maximum simultaneous switching bits is 32.

Tadashi Arai asked what the "on-die model" was. Masuko-san said it was the internal model of the chip connections from the chip vendor, in a power aware IBIS model.

QUALITY CHECKS FOR POWER AWARE IBIS MODELS

Ashish Gupta and Rameet Pai (Cadence Design Systems, India) [Presented by Takuya Moriya (Cadence Design Systems, Japan)]

Takuya Moriya introduced power aware IBIS models. Some quality checks can be performed to correlate IBIS model simulation with SPICE netlist simulation results. The first quality check is simulation with sinusoidal noise injected into the power rail to measure jitter sensitivity. The second quality check is simulation with/without power and ground rail parasitics. Each case did not correlate well in simulation. For the first case, jitter occurs due to changes in I/O buffer delay, which is a function of the supply voltage. Power supply noise induced jitter (PSNIJ) is modeled by simulating the model three times with only +/- 5% voltage variation, overlapping the results to generate an eye diagram. The IBIS simulation matched better to the SPICE netlist simulation results. For better matching of the second case, an RC model of the on-die power supply decoupling had to be added to the IBIS model. A table of delay versus voltage variation could be included in an IBIS model to improve the EDA tool simulation results.

Someone asked if the magnitude of noise (200mV p2p @ 100MHz, 50mV p2p @ 1GHz) is reasonable for an actual PCB. Moriya-san responded that these values are for the simulation only.

Yumiko Sugaya asked if the C_series in slide 21 should be frequency dependent. Moriya-san said the values as shown should be suitable for simulation.

VERIFICATION OF PDN DESIGN WITH POWER AWARE IBIS MODEL

Masaki Kirinaka and Akiko Tsukada (Fujitsu Interconnect Technologies Limited, Japan)

Akiko Tsukada presented. Four methods were shown for verifying a circuit board PDN design. The first method is to apply a design guide for the placement of decoupling capacitors. The second method is to check the PDN impedance compared to a target impedance, although the frequency range of the target impedance is uncertain. The third method is to compare the PDN impedance of an evaluation board. The fourth method is to compare the PDN impedance of the board design to the PDN impedance of the PDN impedance of an evaluation board. The fourth method is to compare the PDN impedance of the board design to the PDN impedance of an evaluation board.

A power aware IBIS model can be used for absolute verification of the I/O power PDN. Simulations were done to look at various modeling effects. The package PDN model format influences the VDD noise and signal waveform results. An S-parameter model for the package is more accurate than an LCR model. For a package including on-package capacitors, it is necessary to model it with an S-parameter. The frequency range of the S-parameter also influences the accuracy of the power noise analysis.

For core power PDN verification, additional information is needed such as current waveforms and an on-die core power decoupling capacitance model.

IBISCHK6 V6.1.3 AND EXECUTABLE MODEL FILE CHECKING

Bob Ross (Teraspeed Labs, USA)

Mike LaBonte presented. New ibischk6 version 6.1.3 executables are available that resolve BUGs 174-180. The executable names include 32 and 64-bit operating system designations. An enhancement is executable model file checking per BUG179 for [Algorithmic Model] executable lines. Executable files are checked for the existence of required functions based on .ami file Reserved_Parameters settings.

TOUCHSTONE CONVERSION WRAPPER

Anders Ekholm (Ericsson, Sweden)

Anders Ekholm presented. The tschk2 Touchstone file parser can be used to convert Touchstone models to Touchstone 2 models using the –canonical option. Using this option strips out any comments from the original Touchstone file which may contain useful port information. Anders wrote a Perl script named TS1toTS2 that solves this issue. The script is available on the IBIS Open Forum website.

IBIS MODEL – THE THANKWORTHY TECHNOLOGY

Kazuhiko Kusunoki (WADOW, Japan)

Kazuhiko Kusunoki presented some history of IBIS. He asked the audience to discuss if they were satisfied with IBIS and to discuss the future of IBIS.

Shinichi Maeda commented that checking IBIS models is a must. Everyone should read the comments in an IBIS file, the readme file and other documentation, and test simulations should be run.

Shogo Fujimori commented that the availability of IBIS models for automotive devices was insufficient, and he expected more to be supplied.

Yu Yamada said IBIS models always had to be checked upon receipt, and that training was needed to do this. There are difficulties comparing IBIS models with measurements. Only certain engineers have the knowledge, and it is difficult to spread that within a company.

IBIS provider Tadashi Arai commented that it is true that chip vendors have a cost to make IBIS models. SPICE models are generated for "free" as a subsequent product of chip development, while IBIS requires resources to be generated. This is especially true for representing modern complex buffer behaviors, using IBIS-AMI and/or power-aware keywords. The vendor needs to spend a lot of time and workload for those. He said there is a concern that LSI vendors might not provide all IBIS models free of charge, suggesting that users should convey that IBIS models are important to them, so that model providers will put more resources into producing good IBIS models. FPGA vendors have more motivation to produce IBIS models than for custom ICs.

He said it was not easy for model makers to produce accurate models as described in the IBIS Accuracy Handbook. Most IBIS providers don't have a formal qualification process, and that is why many IBIS models have the "not guaranteed" disclaimer. System makers are required to

produce evidence of quality to comply with the Product Liability Act, and it is important to decide who is responsible for the accuracy of simulation results.

Kusunoki-san commented that users are encouraged to claim the importance of IBIS. Once it is recognized by IBIS providers, they will be happy to spend money to provide good and accurate IBIS model.

Yukio Masuko said many vendors outsource IBIS model creation, and that was driving up the cost. They tend to provide SPICE for use by semiconductor companies, but not to system companies.

A key point made by Kusunoki-san was that IBIS models are expensive to make, especially compared to SPICE models that are automatically generated in seconds, and AMI is even more expensive.

CLOSING REMARKS

Mike LaBonte thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 5:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held December 2, 2016.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to one of the task group email lists: <u>ibis-macro@freelists.org</u>, <u>ibis-interconn@freelists.org</u>, or <u>ibis-quality@freelists.org</u>.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/ http://www.ibis.org/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/ http://www.ibis.org/bugs/tschk/bugform.txt The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/ http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

		Standards				
Organization	Interest Category	Voting Status	November 4, 2016	November 11, 2016	November 14, 2016	November 18, 2016
ANSYS	User	Inactive	Х	-	-	Х
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	Х	Х	Х	Х
Cisco Systems	User	Inactive	-	Х	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Active	-	Х	Х	Х
GLOBALFOUNDRIES	Producer	Inactive	Х	-	-	-
Huawei Technologies	Producer	Inactive	-	Х	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
IBM	Producer	Inactive	Х	-	-	-
Intel Corp.	Producer	Active	Х	Х	Х	-
IO Methodology	User	Active	Х	Х	Х	-
Keysight Technologies	User	Inactive	Х	-	-	Х
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Inactive	Х	-	-	Х
Micron Technology	Producer	Inactive	Х	-	-	Х
Signal Integrity Software	User	Active	Х	Х	Х	Х
Synopsys	User	Inactive	Х	Х	-	-
Teraspeed Labs	General Interest	Inactive	Х	-	-	-
Xilinx	Producer	Inactive	-	-	-	Х
ZTE	User	Inactive	-	Х	-	-
Zuken	User	Inactive	-	-	-	Х

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- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings
- Interest categories associated with SAE standards ballot voting are:
 - Users members that utilize electronic equipment to provide services to an end user.
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 - General Interest members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.