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Verification of PDN Design with Power Aware IBIS MODEL

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Agenda

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- The Present verification methods of Board PDN design and Expectation to Power Aware IBIS Model
- Challenges for Verification with Power Aware IBIS MODEL
- Verification with Power Aware IBIS MODEL Summary
- For the Core power PDN verification

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The Present verification methods of Board PDN design and Expectation to Power Aware IBIS Model

- Method1) Apply the Design Guide of IC Maker to the Board design
- Method2) Check with the Target Impedance
- Method3) Compare with the Impedance of Evaluation board of IC Maker
- Method4) Compare with the Impedance of Existing Equipment's board
- Expectation for Power Aware IBIS Model

Method1) Apply the Design Guide of IC Maker to the Board design

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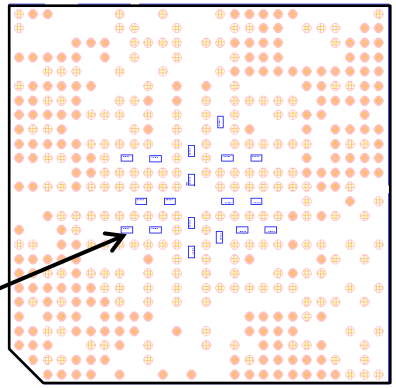
Apply the Design Guide to the Board design. The design is good.

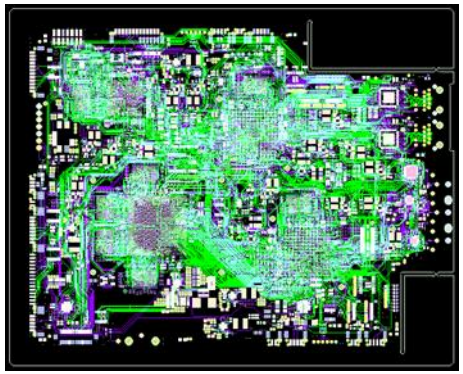
Design Guide example

Capacitor conditions:

Capacitance	Size	quantity
0.1uF	0603	20
4.7uF	1005	1
22uF	1608	1



Apply



Board design
for the verification

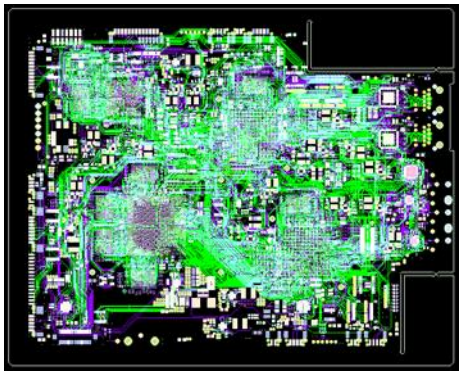
Method2）Check with the Target Impedance

If the PDN Impedance of Board design is lower than the Target Impedance, the design is good.

IC Datasheet

Parameter	Symbol	Min	Nom	Max	Unit
Power Current	Idd	-	-	3000	mA
Supply Voltage	Vdd	1.31 Vdd-3%	1.35	1.39 Vdd+3%	V

Check

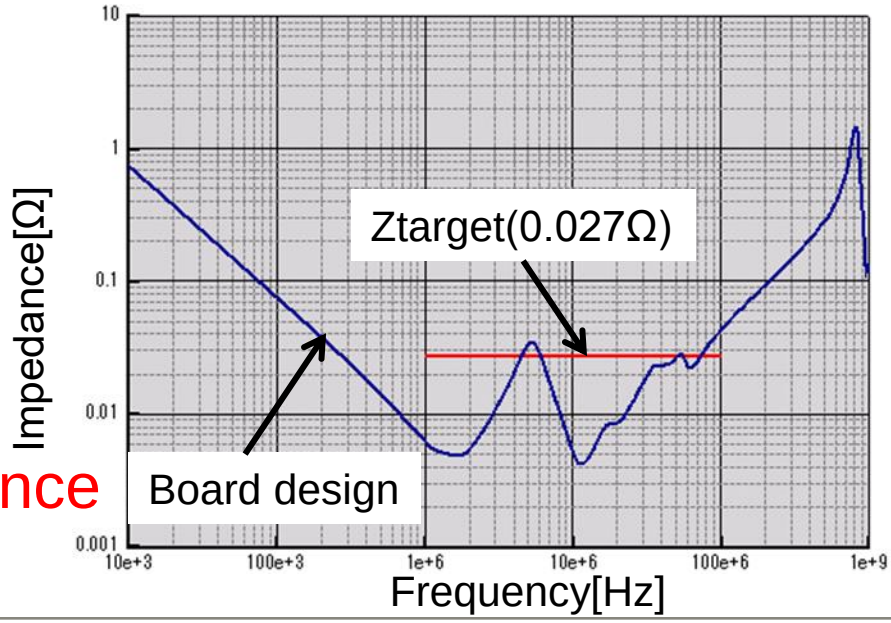


Board design for the verification

Target Impedance

$$\text{Ztarget} = \frac{\text{Vdd} \times 3\%}{\text{Idd} \times 50\%}$$

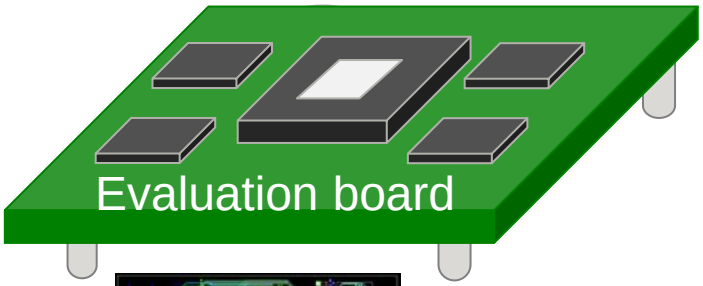
$$= \frac{1.35 \times 0.03}{3 \times 0.5} = 0.027\Omega$$



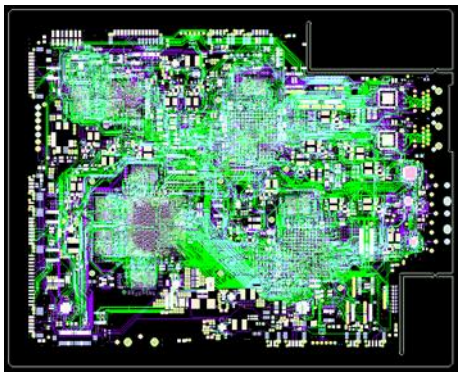
Frequency range of Target Impedance is uncertain

Method3) Compare with the Impedance of Evaluation board of IC Maker

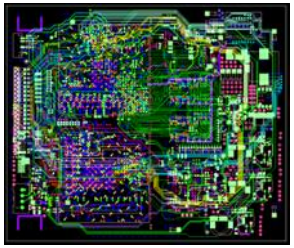
If the PDN Impedance of Board design is lower than the PDN Impedance of Evaluation board, the design is good.



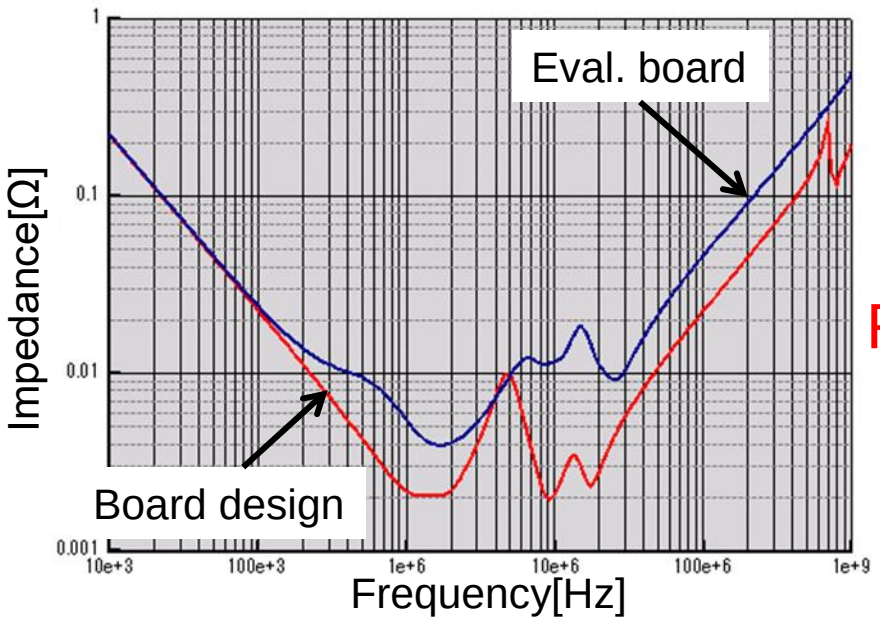
Comparison



Board design for the verification



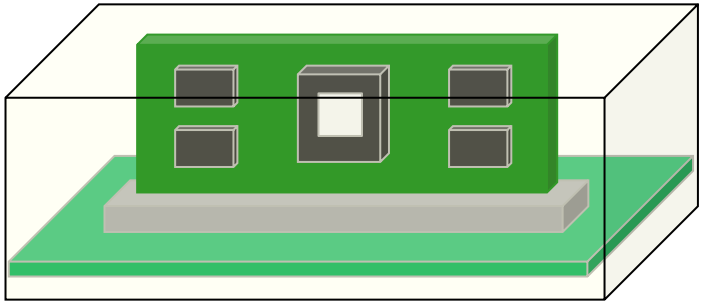
Design of Evaluation board



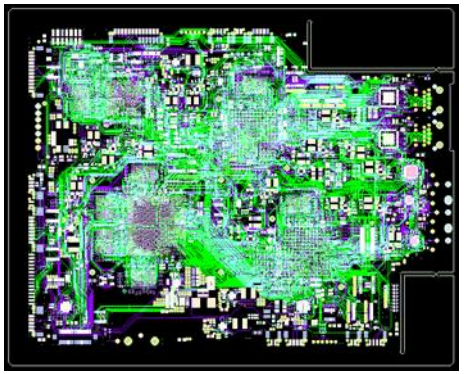
Relative verification

Method4) Compare with the Impedance of Existing Equipment's board

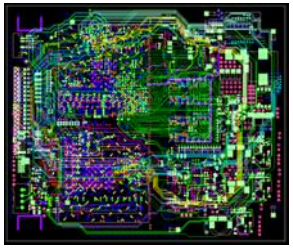
If the PDN Impedance of Board design is lower than the PDN Impedance of Existing Equipment's board, the design is good.



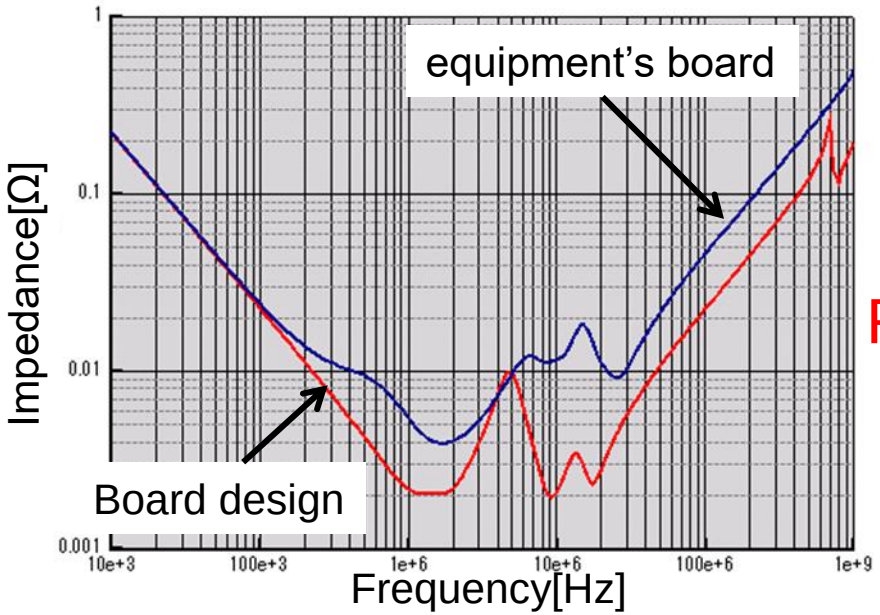
Comparison



Board design for the verification



Design of existing equipment's board



Relative verification

Expectation for Power Aware IBIS Model

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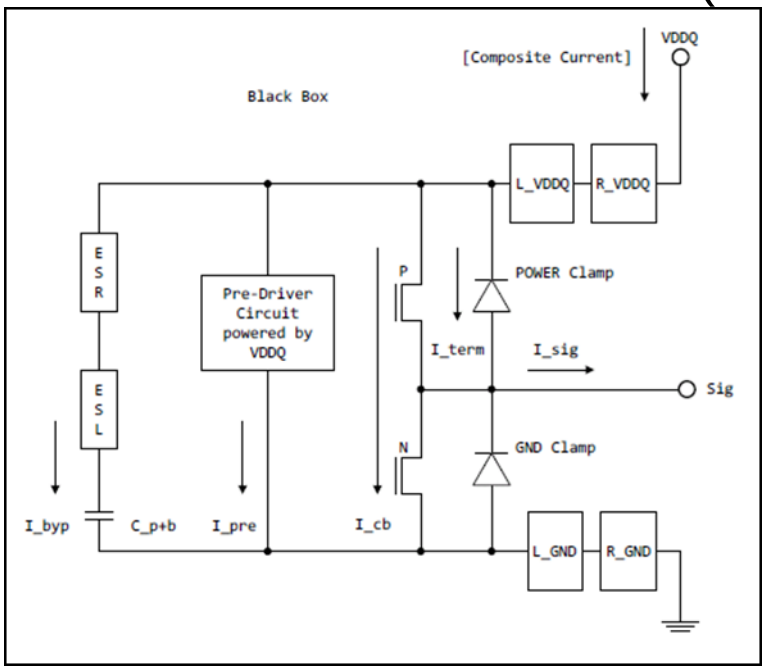
Power Aware IBIS (IBIS 5.0) Model Spec.



Source: “IBIS Ver6.1”

Power Aware IBIS Model Keywords and relating subparameters

- [Composite Current]
- [ISSO PU]
- [ISSO PD]
- C_comp_pullup
- C_comp_pulldown
- C_comp_power_clamp
- C_comp_gnd_clamp

Modeling the IO Power current including PDN of the Die

Absolute verification of IO power PDN is enabled

Challenges for Verification with Power Aware IBIS MODEL

- Power Noise Simulation Model
- Power Noise difference between IBIS 4.2 and IBIS 5.0
- Power Noise difference by the Package PDN Model

  IBIS [Define Package Model] (LCR) versus S-param model
- Power Noise difference by the Package Decoupling Capacitor
- Power Noise difference by the Package S-param model frequency range

Power Noise Simulation Model

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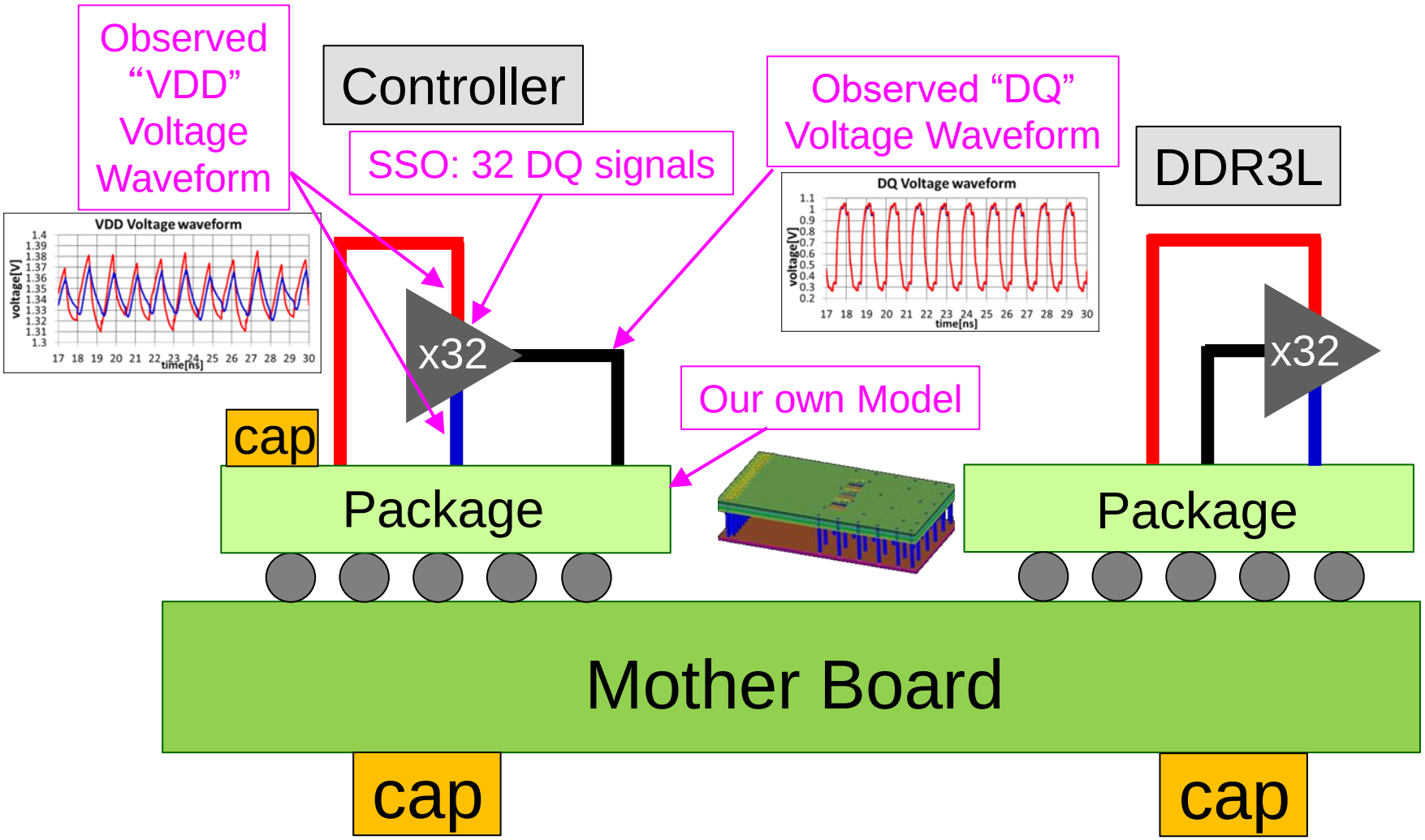
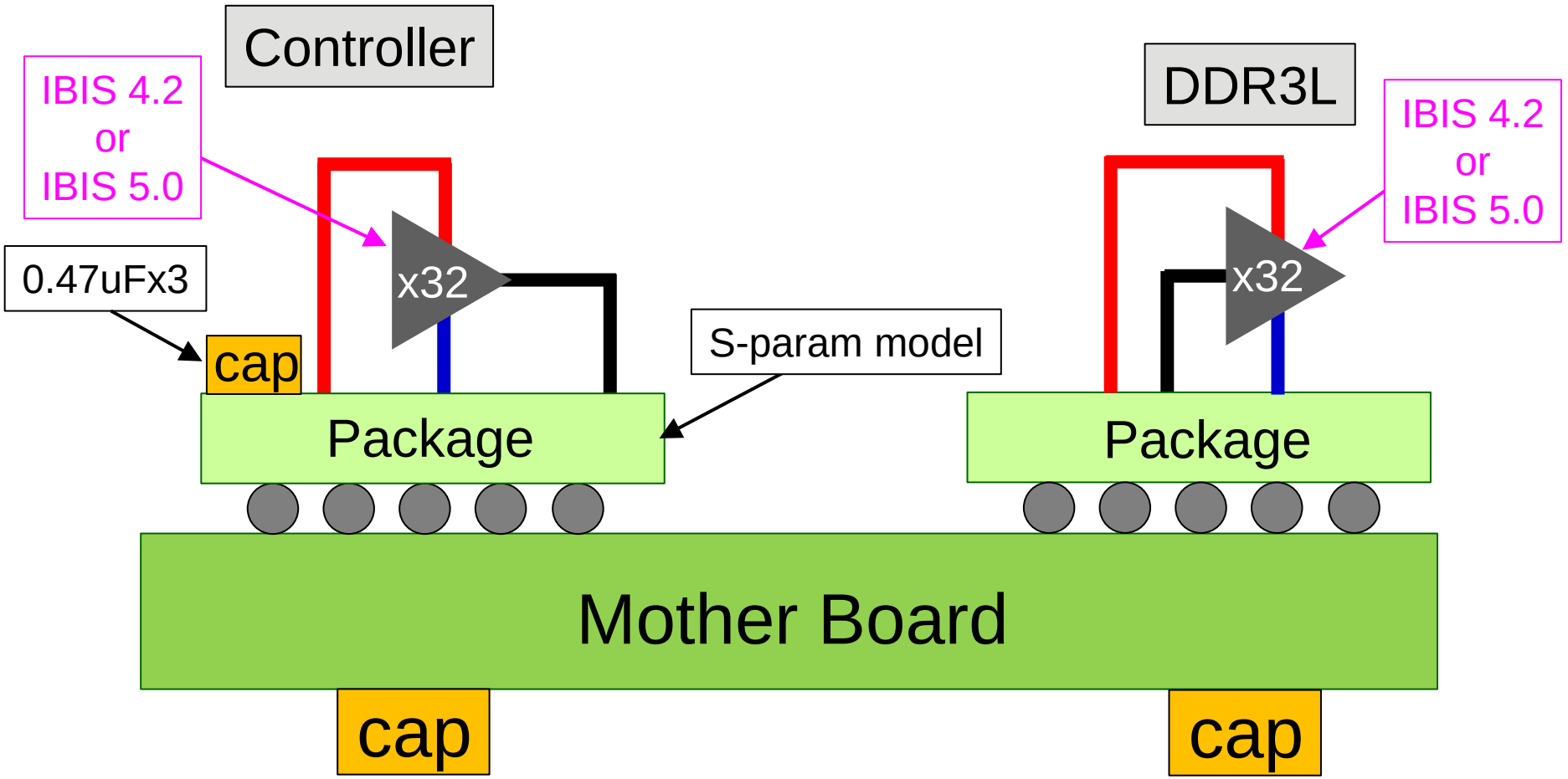
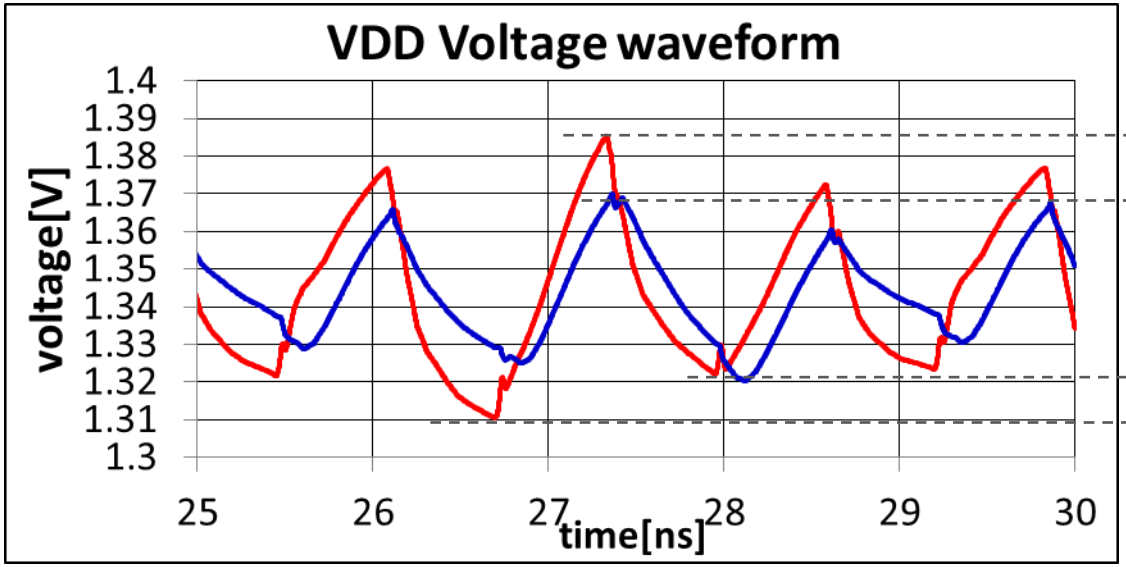
DDR3L-1600

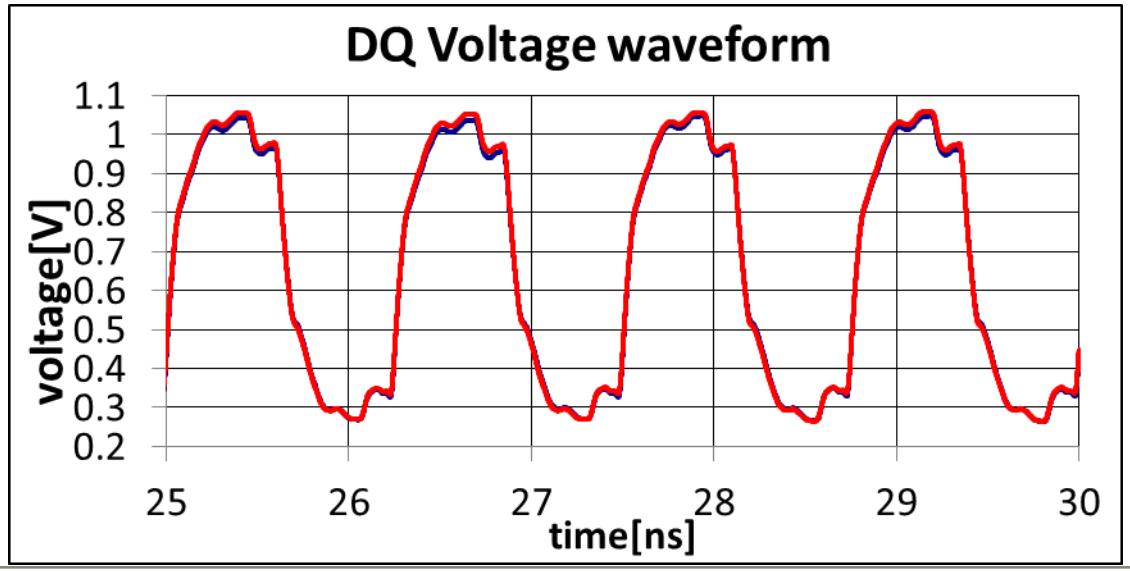


Power Noise difference between IBIS 4.2 and IBIS 5.0



Power Noise difference between IBIS 4.2 and IBIS 5.0

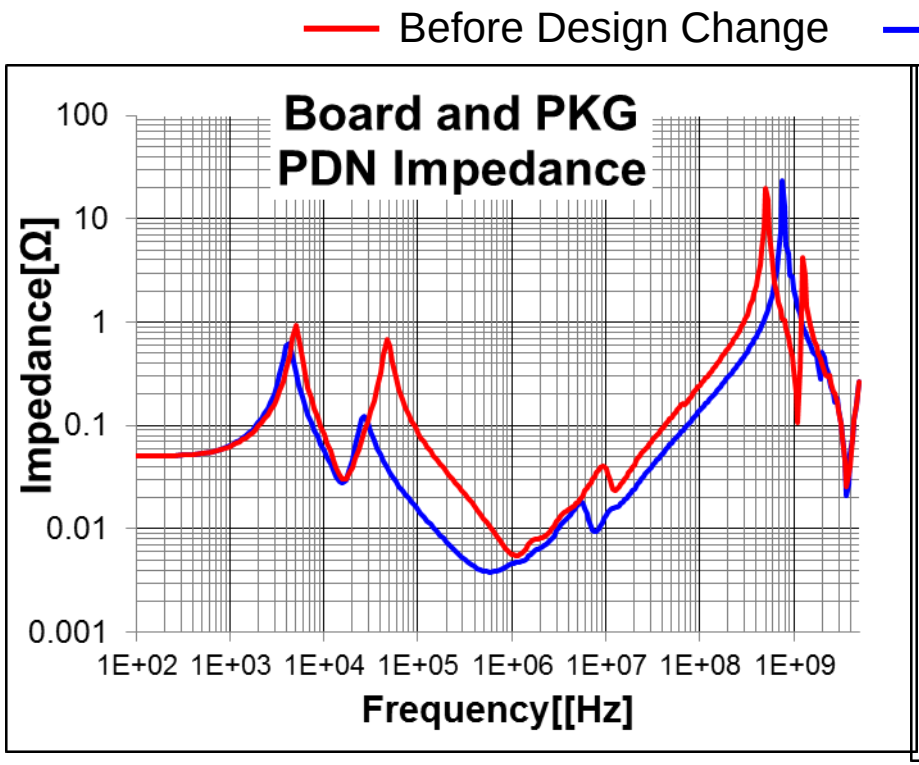


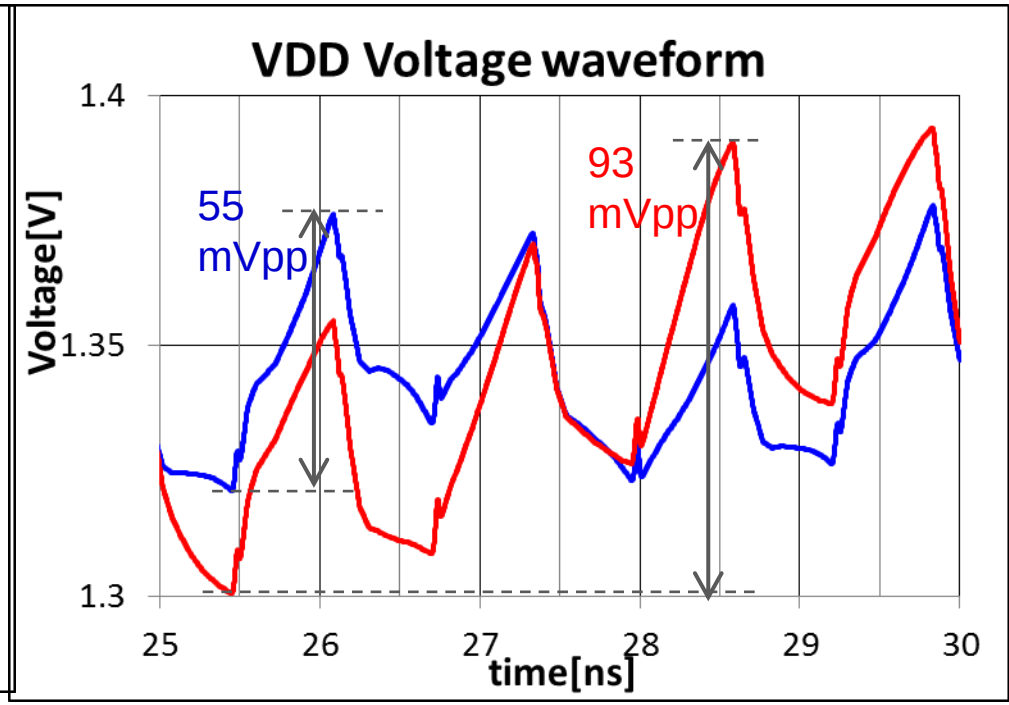


IBIS 5.0 has a larger Power noise.

Power Noise difference between IBIS 4.2 and IBIS 5.0

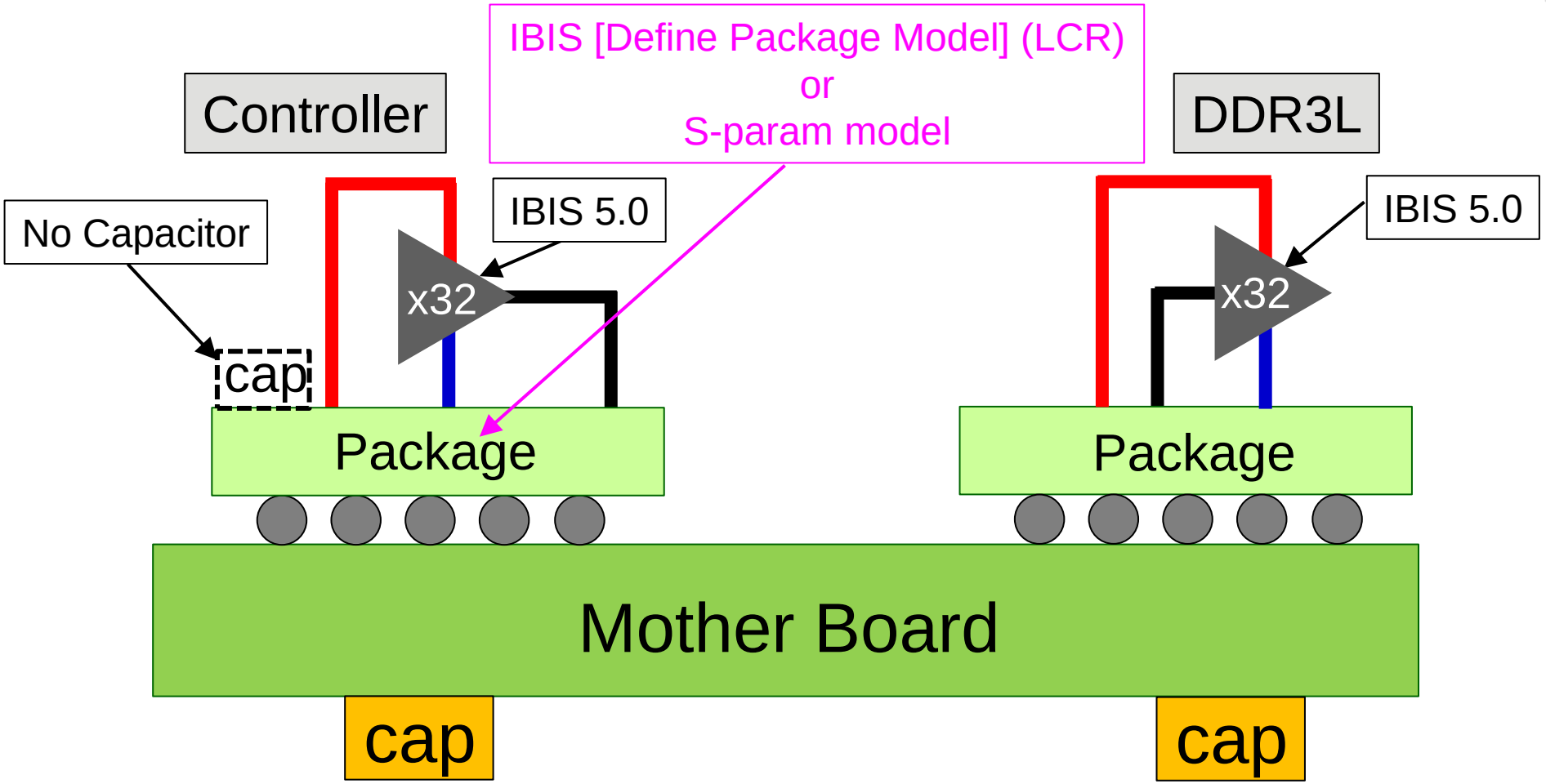
- In IBIS 5.0, the IO Power current including PDN of the Die is modeled.
- Therefore the accuracy of Power noise simulation is improved.
- Enable to change Board PDN design with Power noise simulation result.





Power Noise difference by the Package PDN Model

IBIS [Define Package Model] (LCR) versus S-param model



Power Noise difference by the Package PDN Model

IBIS [Define Package Model] (LCR) versus S-param model

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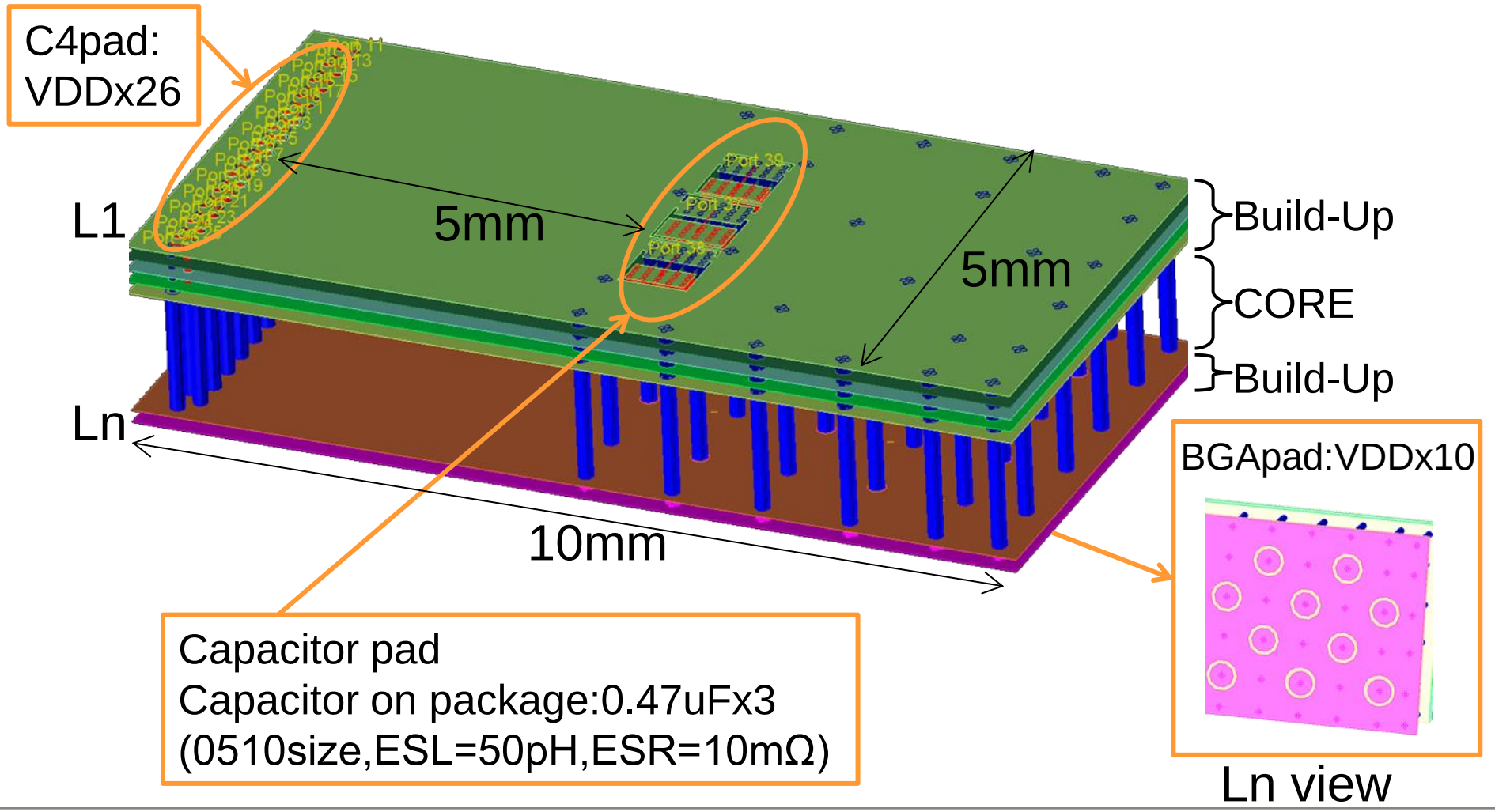
Package model for IO Power

We made this model by assuming PKG PDN of IO.



Power Noise difference by the Package PDN Model

IBIS [Define Package Model] (LCR) versus S-param model

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Making Method Of IBIS [Define Package Model] (L11,C11,R11 for ALL VDD/ GND pin)

Package model

↓

S-param Extraction

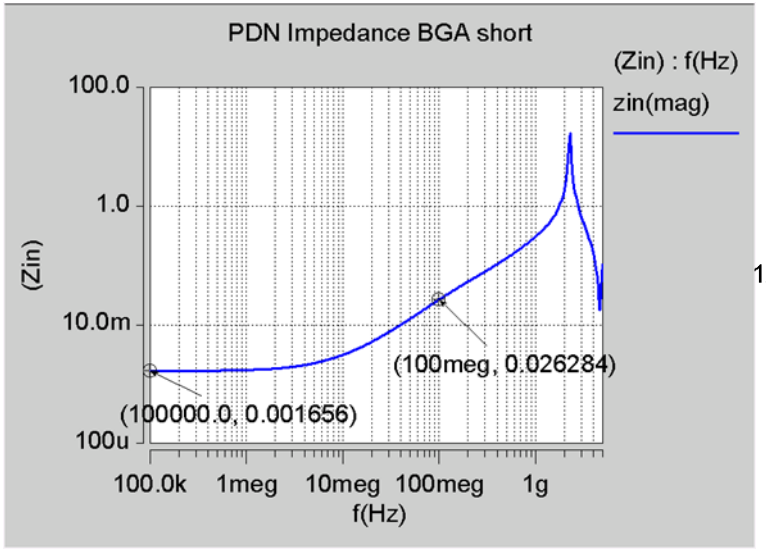
↓

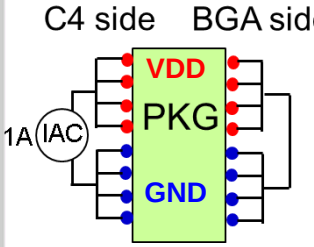
Impedance Analysis

↓

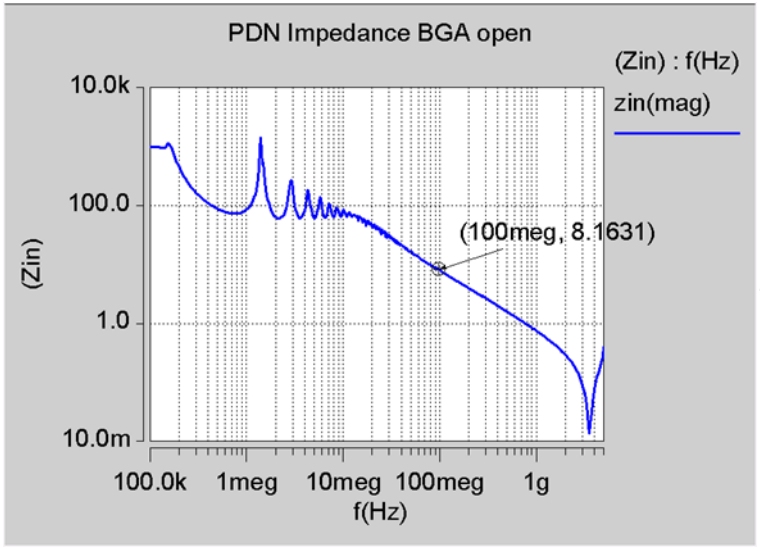
L,C,R Calculation

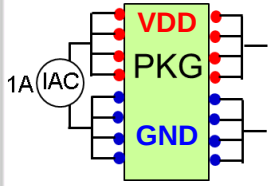
```
[Define Package Model] DDR3L_VDDIO
[Manufacturer] FICT
[OEM]
[Description] Controller PKG MODEL
 for DDR3L SSO Simulation
[Number of Pins] 100
|
[Pin Numbers]
A1  | VDD_1p35
      | included 10 VDD pins
|
[Model Data]
|
[Inductance Matrix] Sparse_Matrix
|
[Row]  A1
A1    42e-12
|
[Capacitance Matrix] Sparse_Matrix
|
[Row]  A1
A1    195e-12
[Resistance Matrix] Sparse_Matrix
|
[Row]  A1
A1    1.7e-03
|
```





L=42[pH]
R=1.7[mΩ]



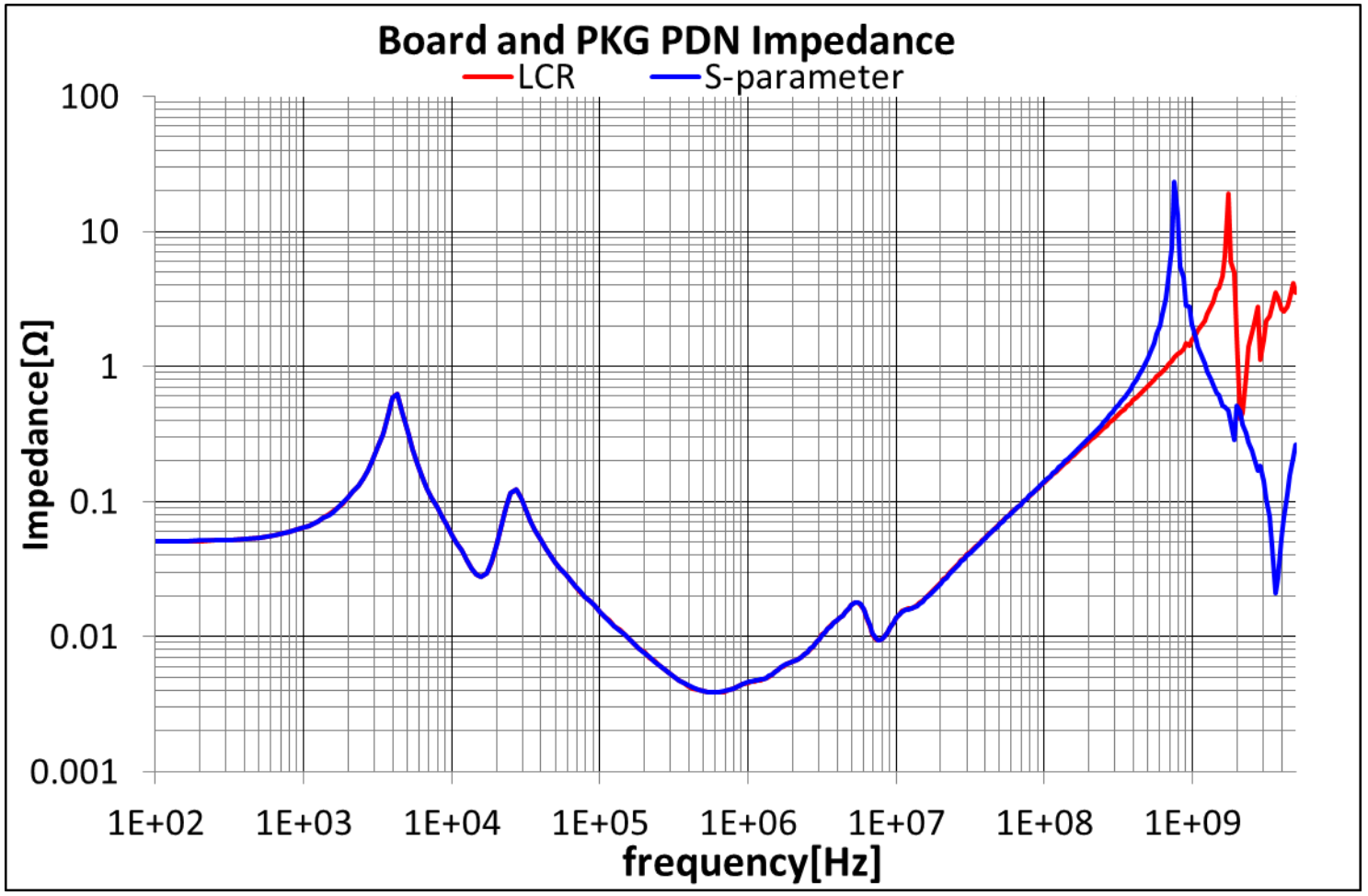


C=195[pF]

Power Noise difference by the Package PDN Model

IBIS [Define Package Model] (LCR) versus S-param model

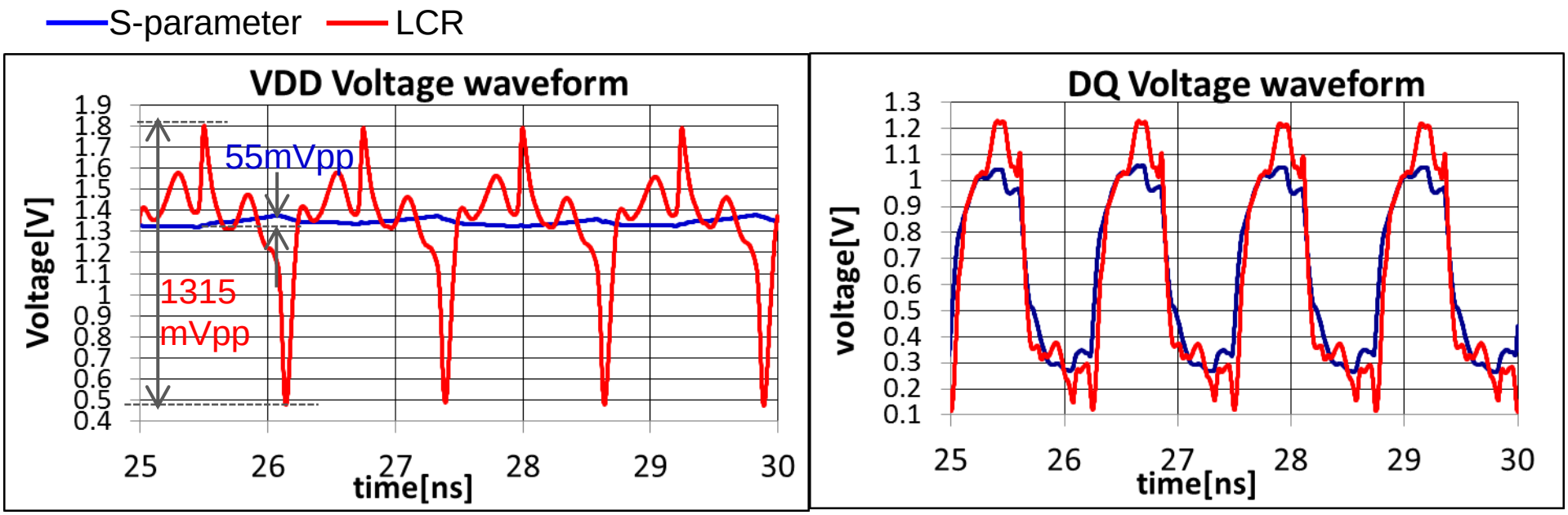
Impedance differences appear at greater than 300MHz in two models.



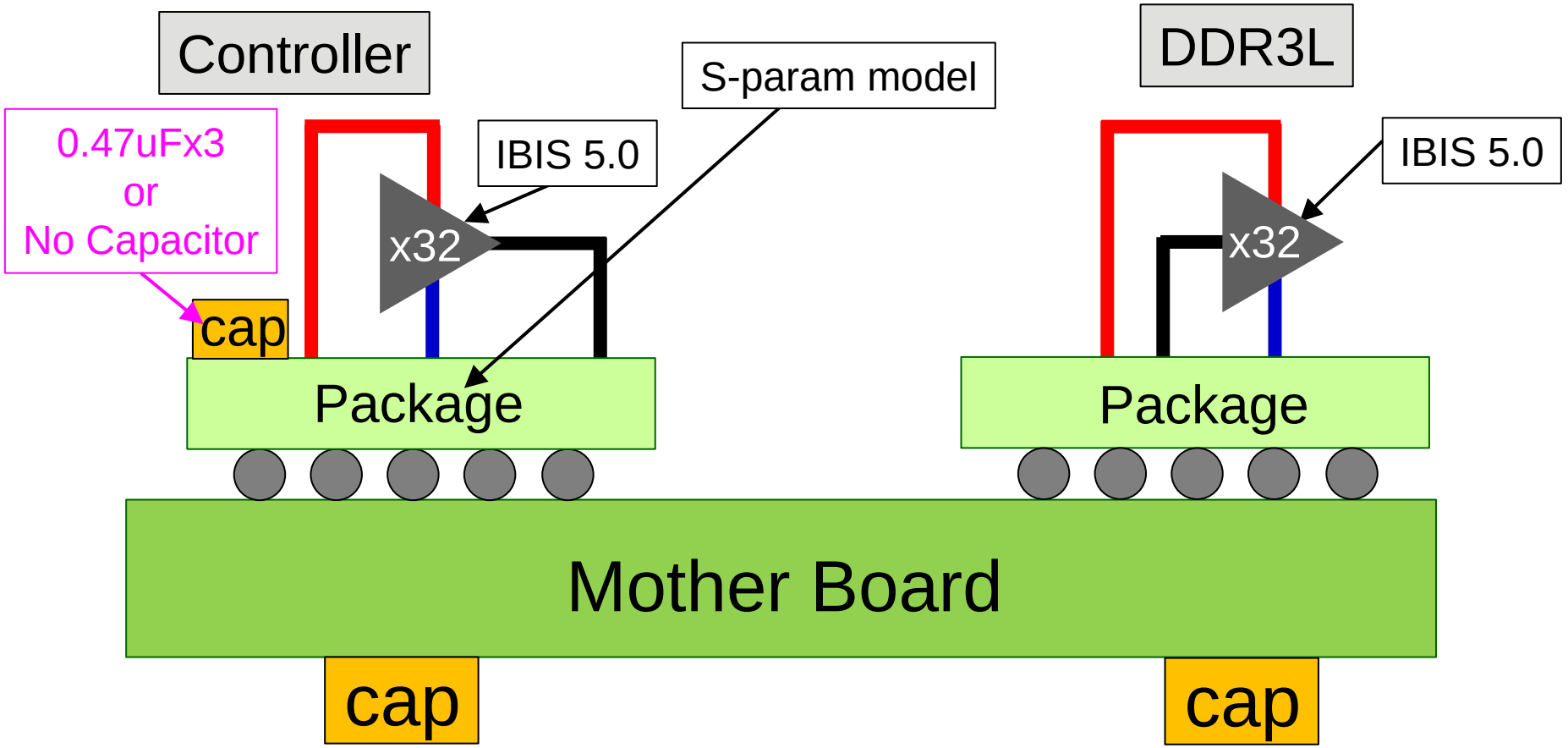
Power Noise difference by the Package PDN Model

IBIS [Define Package Model] (LCR) versus S-param model

- Impedance differences influence VDD Voltage waveform and DQ Voltage waveform.
- S-param model is higher accuracy than LCR model.

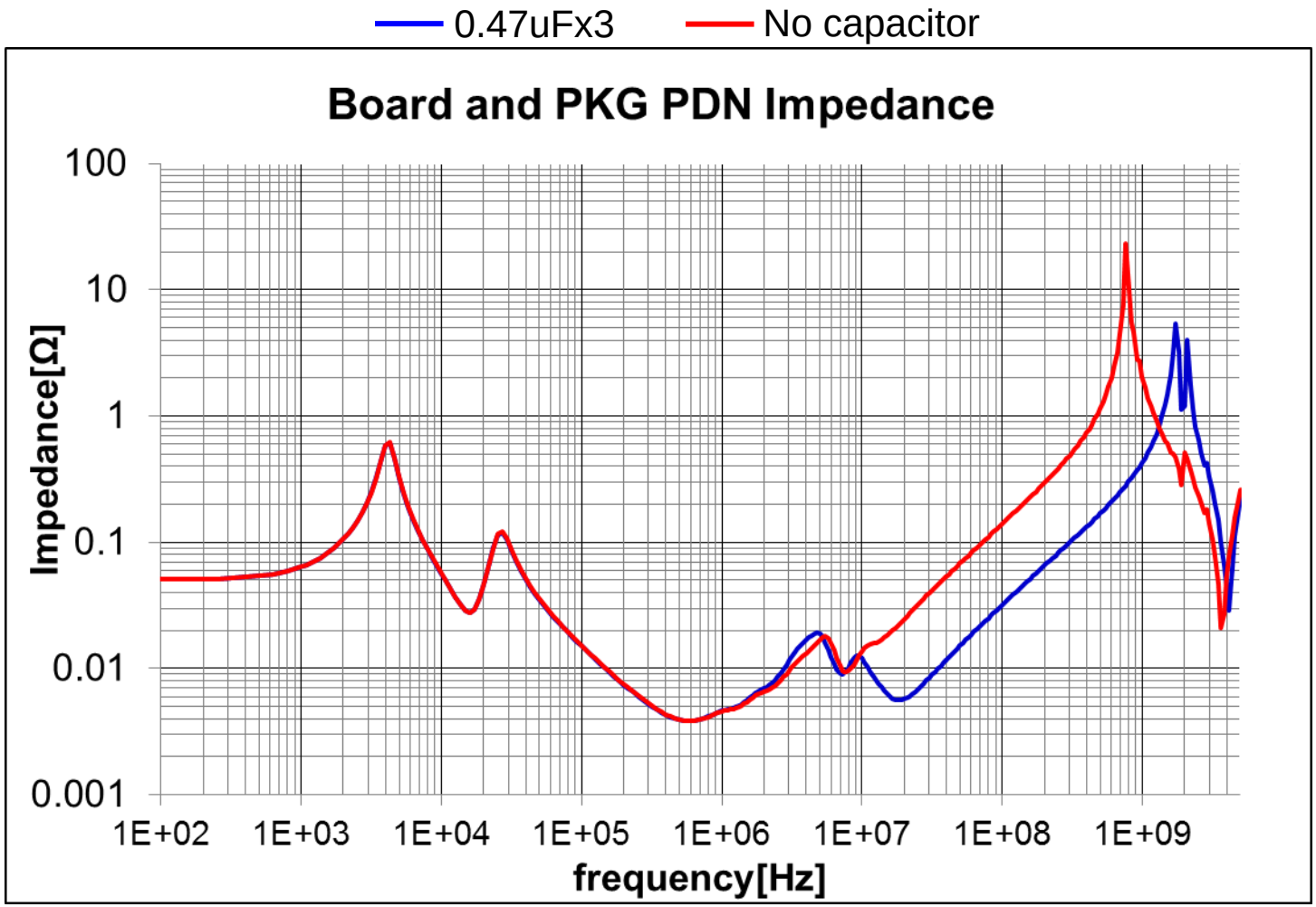


Power Noise difference by the Package Decoupling Capacitor



Power Noise difference by the Package Decoupling Capacitor

Impedance differences appear at greater than 10MHz in two cases.



Power Noise difference by the Package Decoupling Capacitor

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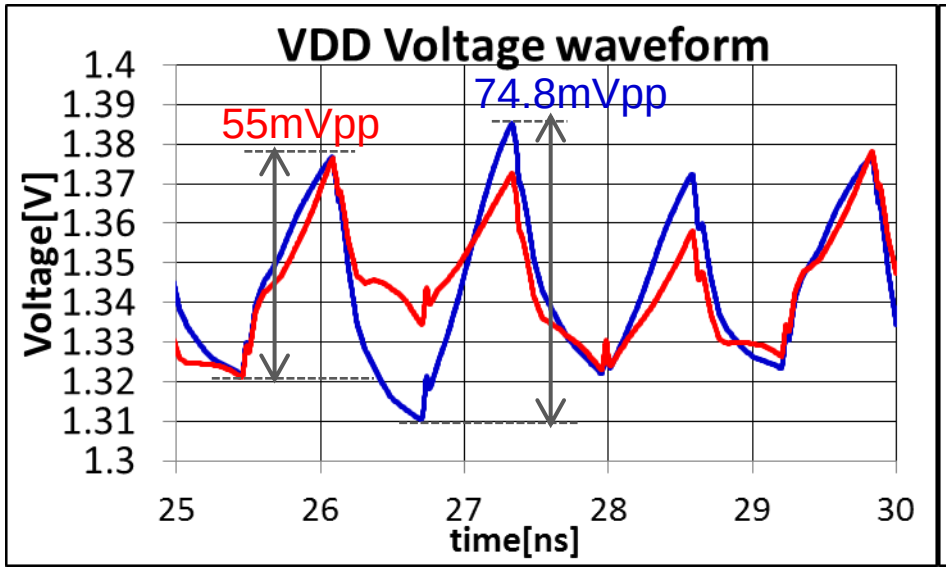
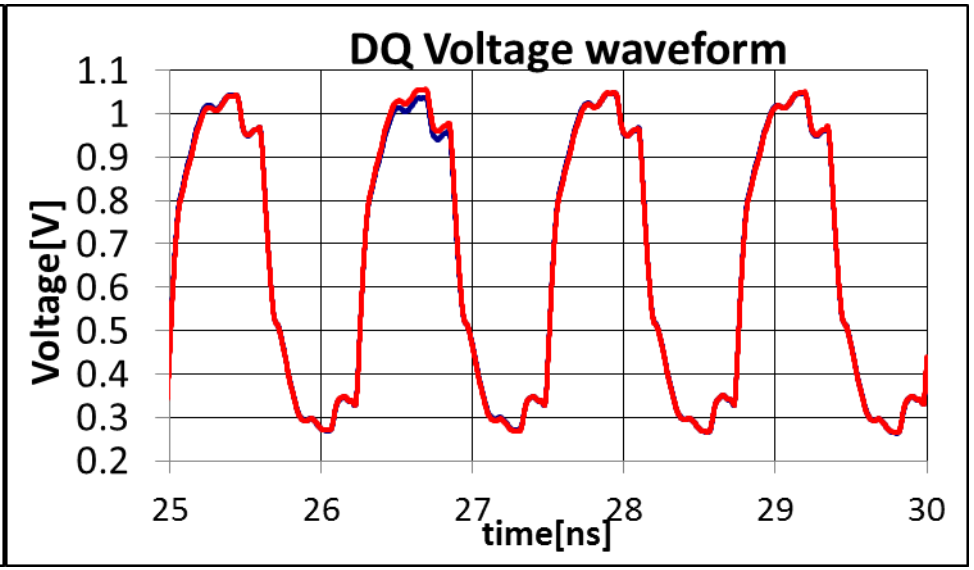
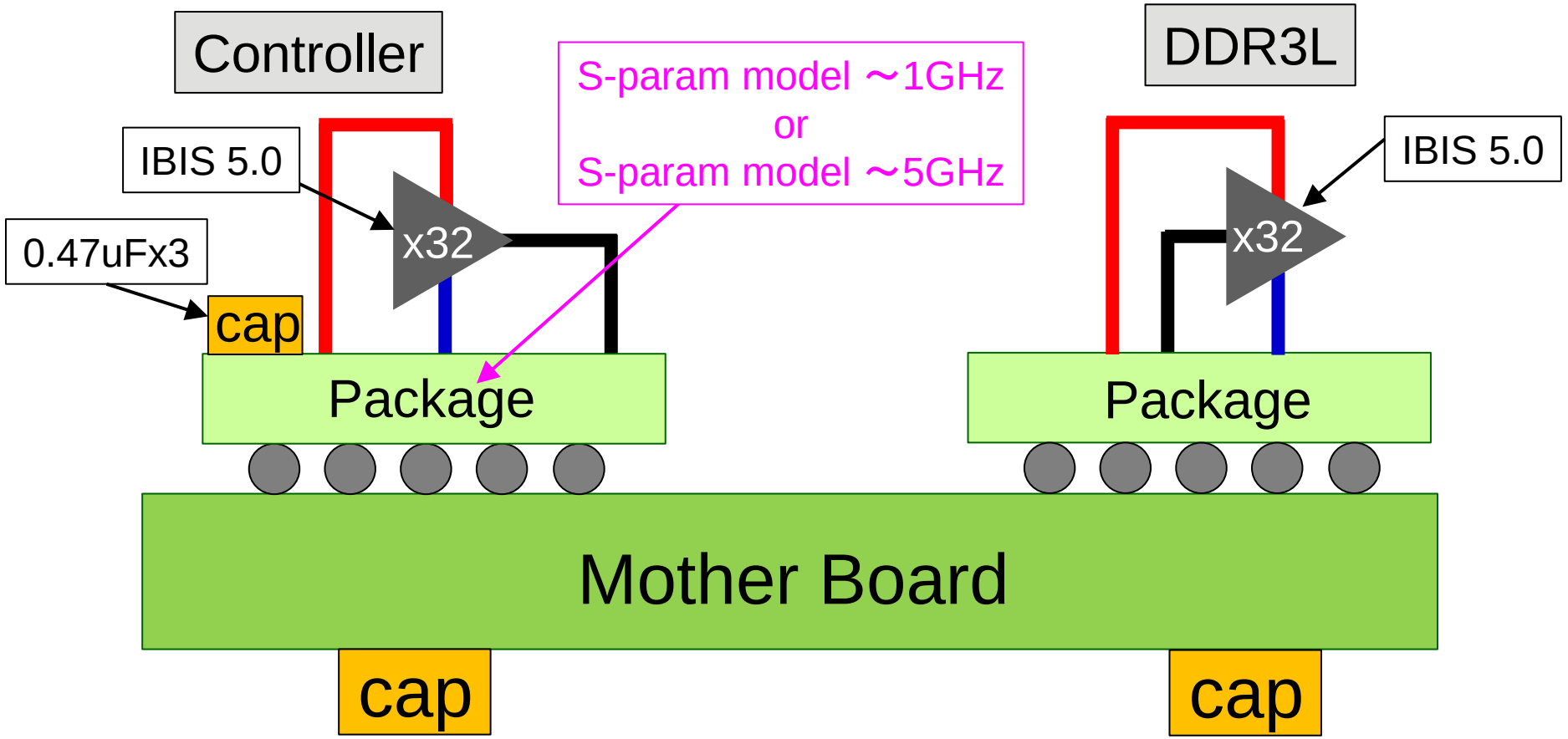
0.47uFx3 No capacitor





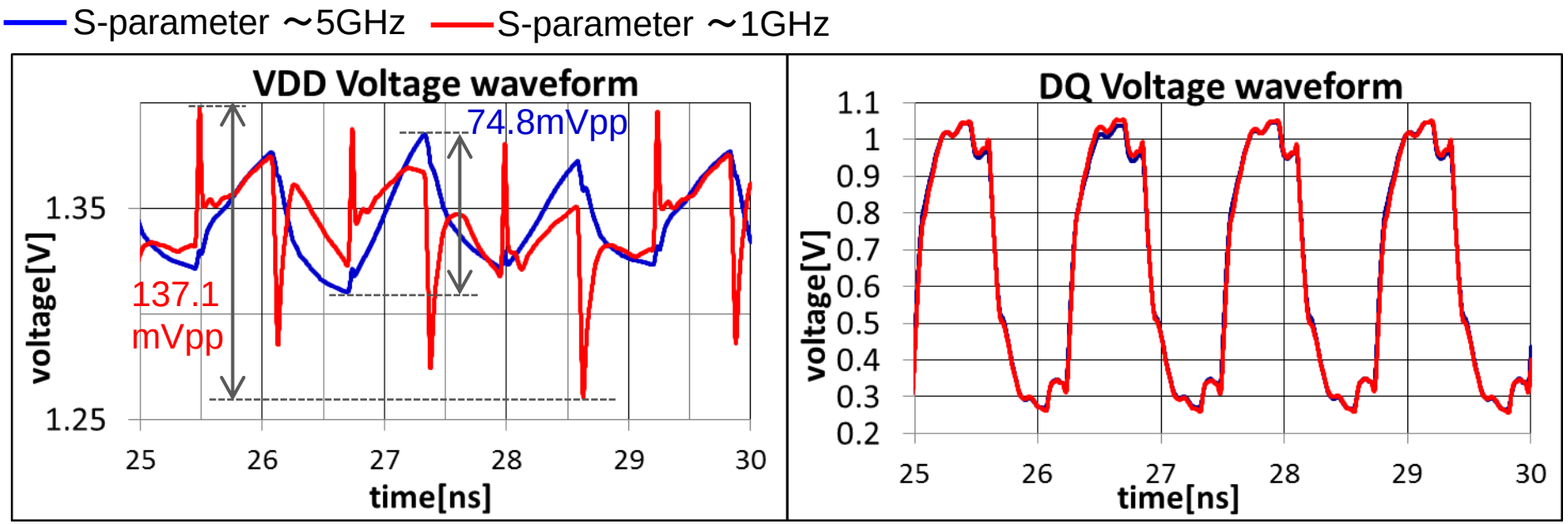
- Impedance less than 1GHz is improved by the package decoupling capacitor.
- But the Power noise increase by the package decoupling capacitor.
  (Because the anti-resonance has moved)
- S-param model that we can put capacitors on is necessary to check this result.
- From these simulation results, it is difficult to judge the improvement of the power noise only by impedance.
- It is necessary to check the power noise.

Power Noise difference by the Package S-param model frequency range



Power Noise difference by the Package S-param model frequency range

A frequency range of S-param model influences the accuracy of the power noise analysis.



Verification with Power Aware IBIS MODEL

Summary

Verification with Power Aware IBIS MODEL Summary

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- In IBIS 5.0, the IO Power current including PDN of the Die is modeled.
- Therefore the accuracy of Power noise simulation is improved.
- Absolute verification of IO power PDN is enabled

- Difference of PKG PDN model format influences VDD Voltage waveform and DQ Voltage waveform.
- S-param model is higher accuracy than LCR model.

- It is necessary for the package mounted with capacitor to model it in S-param.

- The frequency range of the S-param model influences the accuracy of the power noise analysis.

- Expect the spread of IBIS 5.0 and high accuracy PKG PDN model.

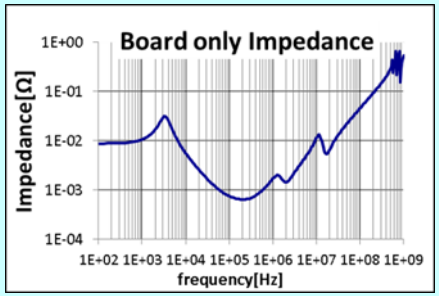
For the Core power PDN verification

For the Core power PDN verification

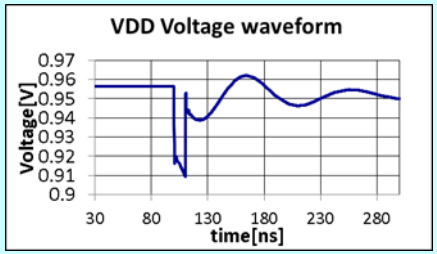
-The currents of the Core power increase lately.
Therefore the design verification of Core power PDN of board also is necessary.

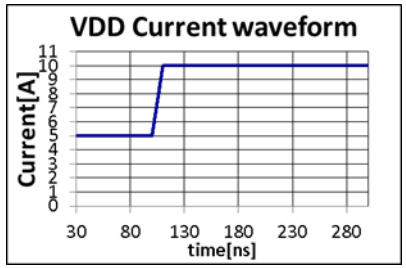
Mother Board only

VDD Impedance



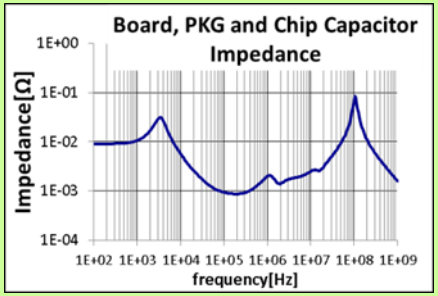
POWER Noise



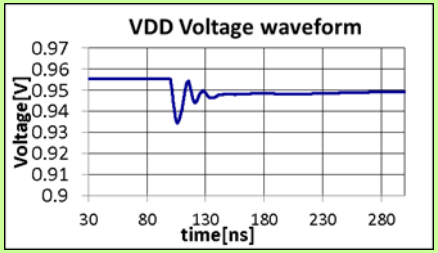


-Mother Board
-Package
-Die Capacitance

VDD Impedance



POWER Noise

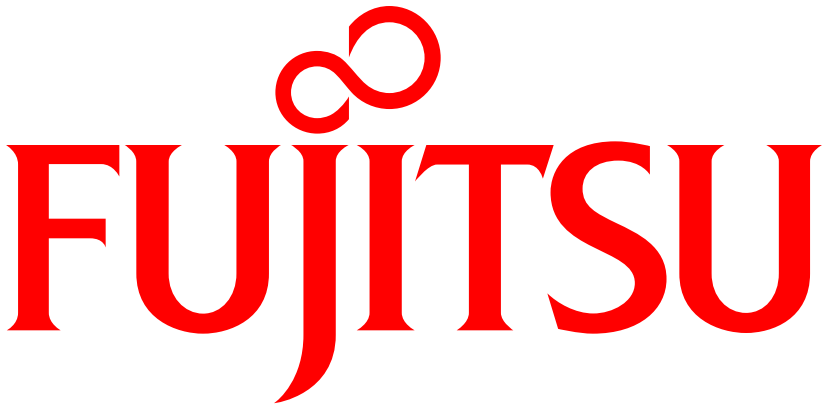


Package, Die capacitance, Current waveforms are necessary for the high accuracy verification.
Also, standardization is expected.

References

- “IBIS (I/O Buffer Information Specification) Version 6.1”,
  IBIS Open Forum 2015
  http://www.ibis.org/ver6.1/ for ibis 6.1

- “IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0”,
  IBIS Open Forum 2011
  http://www.ibis.org/ibis-iss_ver1.0/ for ibis-iss



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