

Differential Modeling Flow with Series Model in Verilog-A

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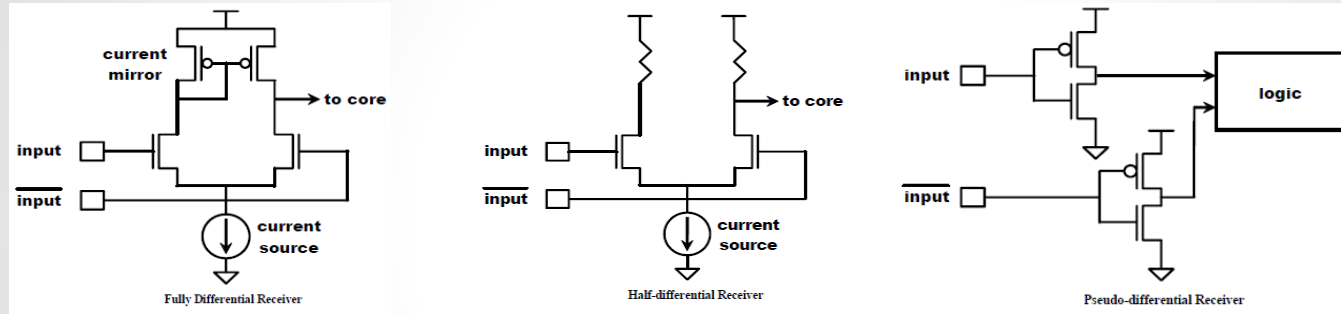


Agenda:

- Background & Motivation
- Verilog-A based modeling
 - Differential current
 - External model
- Flow & Validation
- Summary
- Q & A

Background: (1, IBIS CookBook V4)

- Differential buffer: True/Half/Pseudo differential.

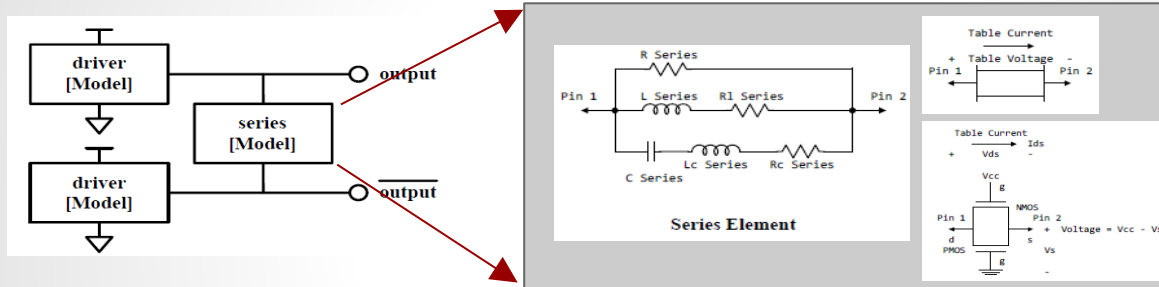


- [Diff Pin]: describe differential behavior between two pins.

| [Diff Pin] | inv_pin | vdiff | tdelay_typ | tdelay_min | tdelay_max |
|------------|---------|-------|------------|------------|------------|
| 1 | | | | | |
| 2 | 3 | NA | NA | 0ns | 5ns |
| 6 | 5 | NA | NA | 0ns | 5ns |

Method 1 for Half/True differential:

- [Series pin mapping]/Series Model:(2)(3)



```
[Diff_Pin]  inv_pin  vdiff  tdelay_typ  tdelay_min  tdelay_max
1           2       0.25    0           NA           NA
3           4       0       0           NA           NA

*****
[Series Pin Mapping]  pin_2  model_name  function_table_group
1           2       R_SERIES_100
3           4       R_SERIES_100

*****
Model R_SERIES_100
*****

[Model]      R_SERIES_100
Model_type   Series
```

Method 2 for Half/True differential:

- [External Model]: Spice/VHDL-AMS/Verilog-AMS/IBIS-ISS(4)

```
[Model]          VHDLAMS-DRV
Model_type       Output
Polarity         Non-Inverting
C_comp          4.60pF          3.50pF          6.00pF
Vmeas = 1.15V
Cref  = 1pF
Rref  = 50ohms
Vref  = 0V
|
[External Model]
Language VHDL-AMS
|
| Corner corner_name file_name      circuit_name entity(architecture)
Corner   Typ          ideal_driver.vhd driver_ideal(linear)
Corner   Min          ideal_driver.vhd driver_ideal(linear)
Corner   Max          ideal_driver.vhd driver_ideal(linear)
|
| Ports List of port names (in same order as in VHDL-AMS)
Ports D_drive A_puref A_pdref A_signal
|
[End External Model]
```

| | |
|--------------|---|
| Input_diff | These model types specify that the model defines a true differential model available directly through the [External Model] keyword documented in Section 6.3. |
| Output_diff | |
| I/O_diff | |
| 3-state_diff | |

Method 1 & 2 can be used together!

Background:

- Data extraction:

- Common-mode current
- Differential current
- C_{comp} & C_{diff}

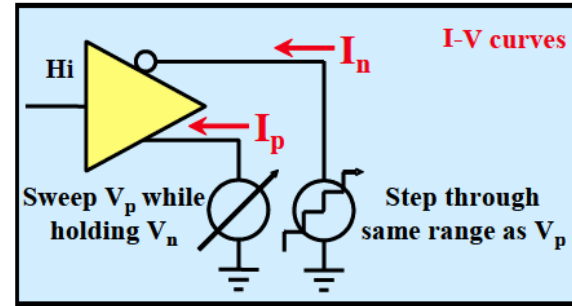
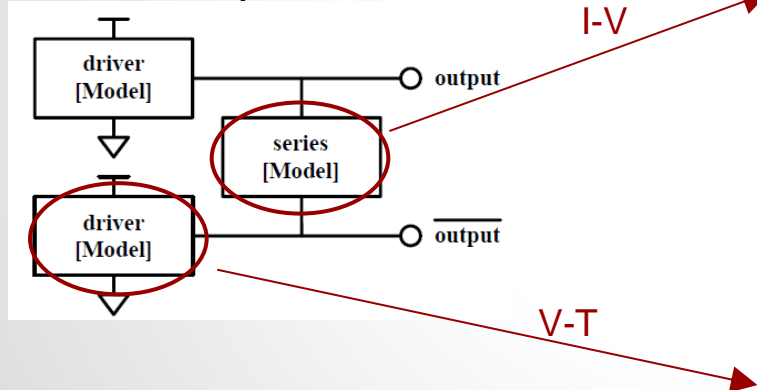


Figure 4.13 – I-V Table Extraction Fixture for a Differential Buffer

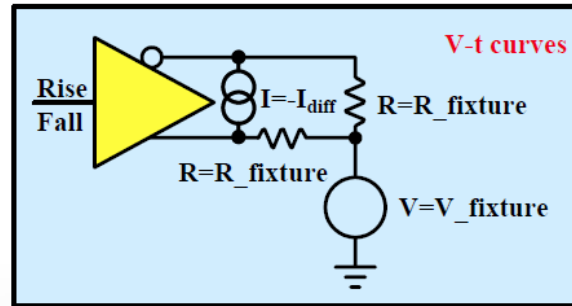
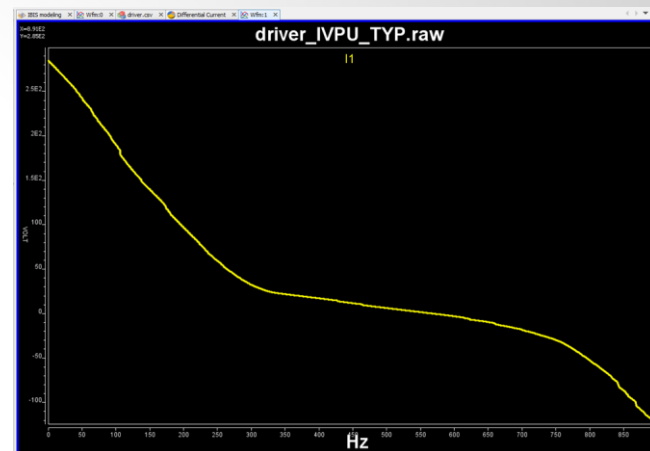
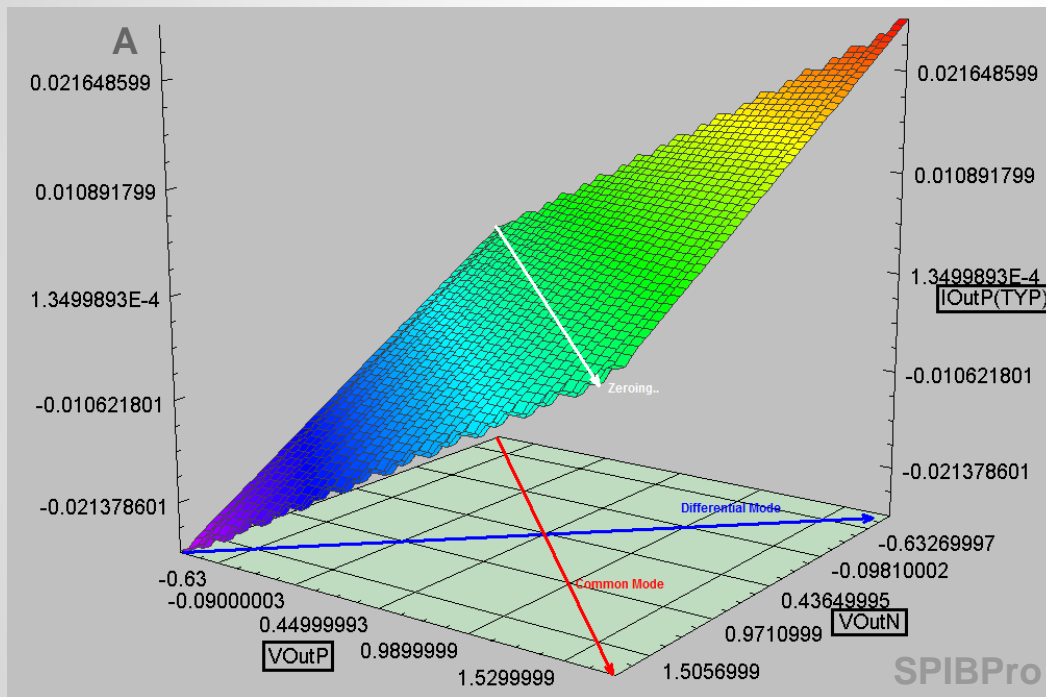
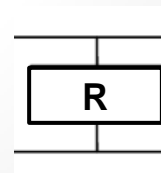


Figure 4.18 – V-T Table Extraction Fixture for a Differential Buffer

Design 1:



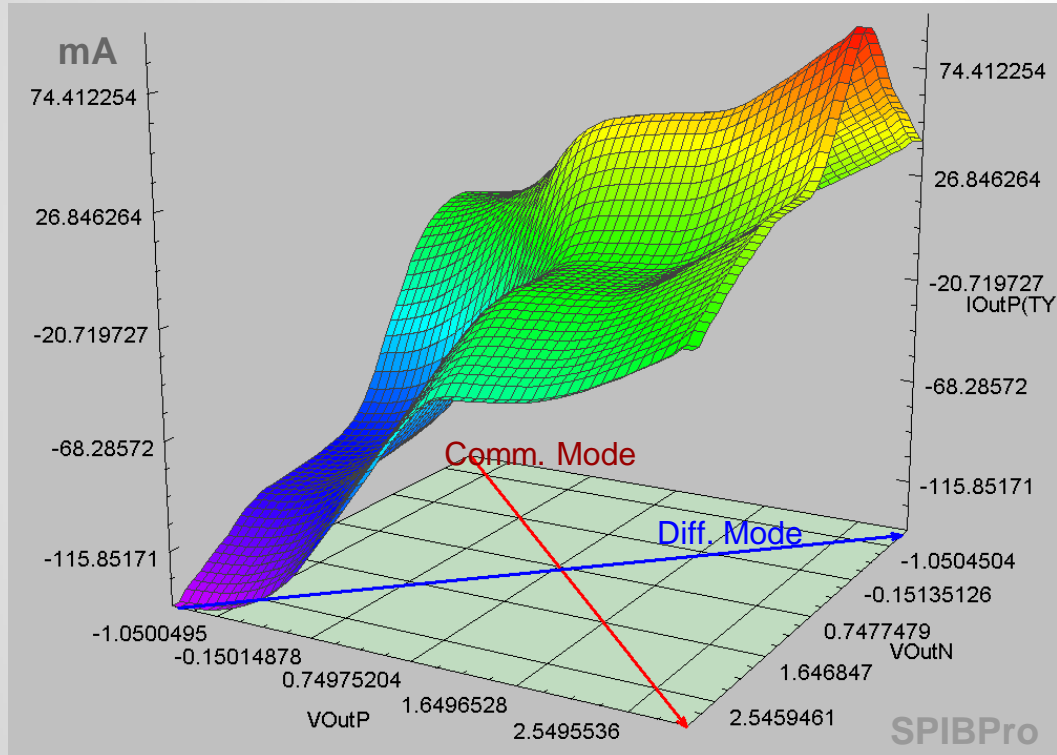
I Comm. Mode as PU/PD, PC/GC



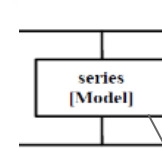
A simple "Series R" can describe this particular design

Shifted surface as differential series elem.

Design 2:



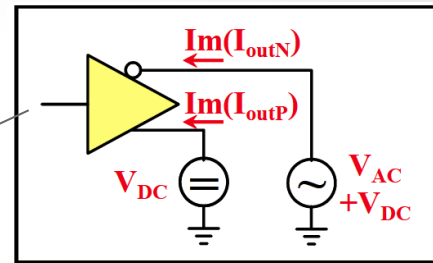
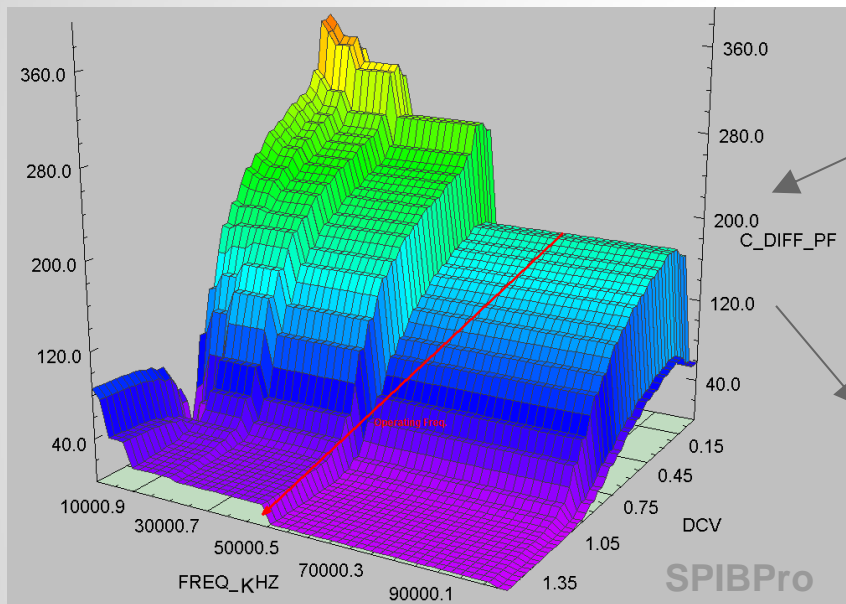
Need to describe this surface data in design 2 for V-T extraction
Affect DC steady states (e.g. mismatch)



Options:

- Surface fit in MSE sense:
 - Need to check residue
 - Translate to EFGH elements
- Series MOSFET
 - Or Series current
- **Behavioral model?**

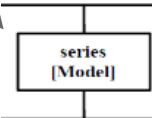
Design 2 C_diff:



Fixture for Extraction of Differential Buffer C_{comp}

Need to describe this surface data for V-T extraction as well

Affects final transient accuracy

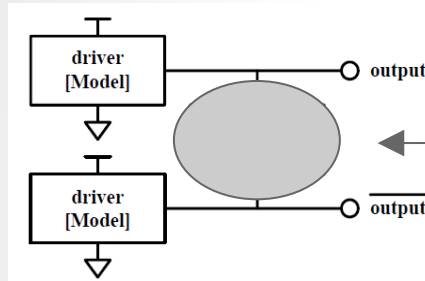


Options:

- Summarize and add single Series C
- **Behavioral model?**

Motivations:

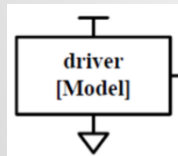
- Limitation of “Generic” series model:



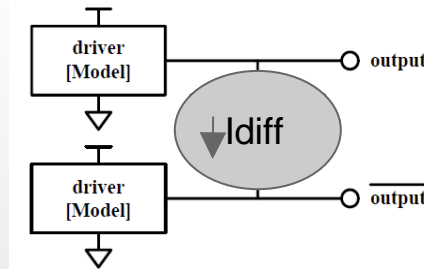
Series Elements:

1. Rigid syntax
2. Condition is fixed (e.g. no polarity)
3. Modeling flow interruption
 - a. Surface fit ?
 - b. Generate tentative series-elem?

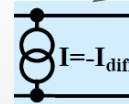
- Accuracy of transient data for V-T extraction:



=



+



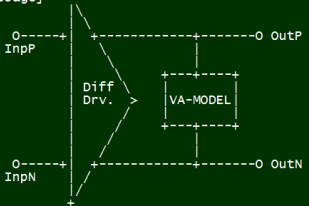
?

Inaccurate TR data will pollute waveform...

Verilog-A based Diff. current model:

Disclaimer:
This Verilog-A model is to subtract differential current for true/half differential IBIS modeling.

[Usage]



1. Please refer to IBIS cook book. Differential model's VT extraction
2. Connect this VA model like the schematic above
3. Prepare corner specific differential_current table using IV data
4. Differential current will be subtracted during VT simulation
5. Resulting transient waveform can be used for VT data table

HSpace Verilog-A Syntax:
.HDL "SPIBPro_DiffI.va"
XDiffI NODEN NODEP SPIDiffI

```

===== TYP =====
module SPIDiffI_TYP(nodeP, nodeN);
  electrical nodeP, nodeN;
  inout nodeP, nodeN;
  parameter real cDiff = 1.000E-11;

  real cDiff; // differential current due to c_diff
  real rDiff; // differential current due to resistance
  real voltP; // P node voltage and slew rate
  real voltN; // N node voltage and slew rate

analog begin
  voltP = V(nodeP);
  voltN = V(nodeN);

  // differential current due to DC steady state
  rDiff = $table_model(voltN, voltP, "driver_TYP.csv", "1L,1L");

  // differential current due to c_diff
  cDiff = ddt(voltP - voltN) * cDiff;

  // current flow between P and N
  I(nodeP, nodeN) <= -(rDiff + cDiff);
end
endmodule

```

A Verilog-A device can be used in differential V-T extraction.

- Behavioral device is very versatile
- Support operator like ddt, if .. else
- Supports 1/2D look-up table **(5), (6)**

```

#Differential current in mA
#VoutN VoutP IDiff_Typ
-1.50E+00 -1.50E+00 0.00E+00
-1.50E+00 -1.46E+00 -7.83E+00
-1.50E+00 -1.41E+00 -1.59E+01
-1.50E+00 -1.37E+00 -2.41E+01
-1.50E+00 -1.32E+00 -3.25E+01
-1.50E+00 -1.28E+00 -4.13E+01
-1.50E+00 -1.23E+00 -5.03E+01
-1.50E+00 -1.19E+00 -5.95E+01
-1.50E+00 -1.14E+00 -6.91E+01
-1.50E+00 -1.10E+00 -7.89E+01
-1.50E+00 -1.05E+00 -8.90E+01
-1.50E+00 -1.01E+00 -9.94E+01
-1.50E+00 -9.60E+01 -1.10E+02

```

Verilog-A for V-T extraction:

```
//===== TYP =====
module SPIDiffI_TYP(nodeP, nodeN);
  electrical nodeP, nodeN;
  inout      nodeP, nodeN;

  parameter real freq = 1.0E9;

  real  cDiffI; // differential current due to c_diff
  real  rDiffI; // differential current due to resistance
  real  voltP;  // P node voltage and slew rate
  real  voltN;  // N node voltage and slew rate
  real  cDiff;  // differential capacitance

analog begin
  voltP = V(nodeP);
  voltN = V(nodeN);

  // differential current due to DC steady state
  rDiffI = $table_model(voltN, voltP, "driver_TYP.csv", "1L,1L");

  // differential current due to c_diff
  cDiff = $table_model(voltN, freq, "driver_CDIF.csv", "1L,1L");
  cDiffI = ddt(voltP - voltN) * cDiff;

  // current flow between P and N
  I(nodeP, nodeN) <+ -(rDiffI + cDiffI);
end
endmodule
```

Voltage & freq. Dependent C_Diff
(or use cross() to find freq. dynamically)

Simulator only supports 1D table?
2D bi-linear look-up can still be done

```
//===== TYP =====
module SPIDiffI_TYP(nodeP, nodeN);
  electrical nodeP, nodeN;
  inout      nodeP, nodeN;

  parameter real freq = 1.0E9; // current working frequency
  parameter real freq1 = 5.0E8; // cdiff at frequency 1
  parameter real freq2 = 2.0E9; // cdiff at frequency 2

  real  cDiffI; // differential current due to c_diff
  real  rDiffI; // differential current due to resistance
  real  voltP;  // P node voltage and slew rate
  real  voltN;  // N node voltage and slew rate
  real  cDiff1, cDiff2, cDiff; // differential capacitance

analog begin
  voltP = V(nodeP);
  voltN = V(nodeN);

  // differential current due to DC steady state
  rDiffI = $table_model(voltN - voltP, "driver_TYP.csv", "1L,1L");

  // differential current due to c_diff
  cDiff1 = $table_model(voltN, "driver_CDIF1.csv", "1L,1L"); // at freq1 = 500M
  cDiff2 = $table_model(voltN, "driver_CDIF2.csv", "1L,1L"); // at freq2 = 2G
  cDiff = (cDiff2 - cDiff1) / (freq2 - freq1) * (freq - freq1) + cDiff1;
  cDiffI = ddt(voltP - voltN) * cDiff;
end
```

Completed Series model:

```
[Pin] signal_name model_name R_pin L_pin C_pin
1 out_p driver 65.00m 4.50nH 0.85pF
2 out_n driver 65.00m 4.50nH 0.85pF

[Series Pin Mapping] pin_2 model_name function_table_group
1 2 seriesmdl
```

- Verilog-A as external model for model type "Series"

```
[Model] seriesmdl
Model_type Series
C_comp 4.60pF typ 3.50pF min 6.00pF max
          typ min max
[External Model]
Language Verilog-AMS
Corner corner_name file_name circuit_name entity(architecture)
Corner Typ series_typ.va series_va
Corner Min series_min.va series_va
Corner Max series_max.va series_va

Ports List of port names
Ports A_pos A_neg

[End External Model]

[Temperature Range] 27.00 70.00 0.000
[Voltage Range] 3.30V 3.13V 3.46V
```

```
[Model] seriesmdl
Model_type Series
C_comp 4.60pF typ 3.50pF min 6.00pF max
          typ min max
[External Model]
Language Verilog-AMS
Corner corner_name file_name circuit_name entity(architecture)
Corner Typ series_typ.va series_va
Corner Min series_min.va series_va
Corner Max series_max.va series_va

Ports List of port names
Ports A_pos A_neg

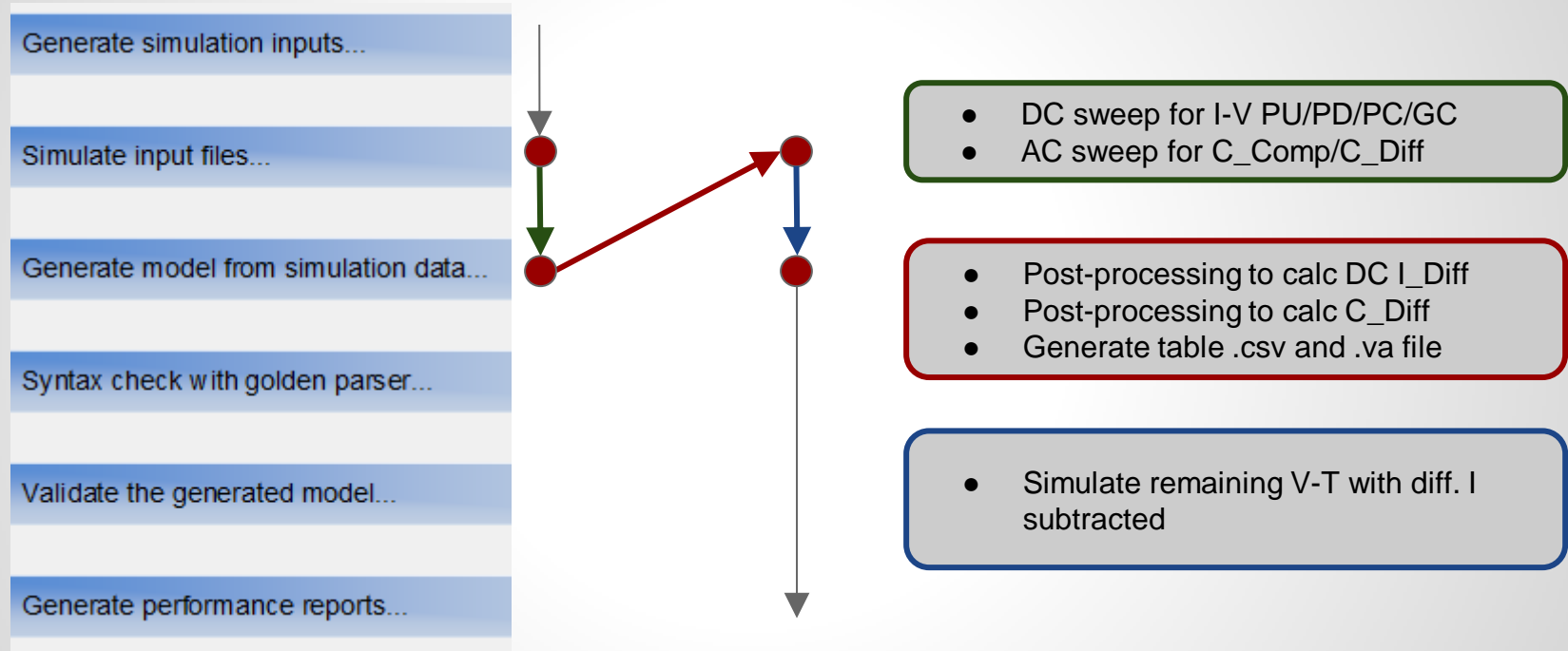
[End External Model]

[Temperature Range] 27.00 70.00 0.000
[Voltage Range] 3.30V 3.13V 3.46V

*****
[R Series] 100ohm 90ohm 110ohm
[C Series] 5pF 4pF 6pF
```

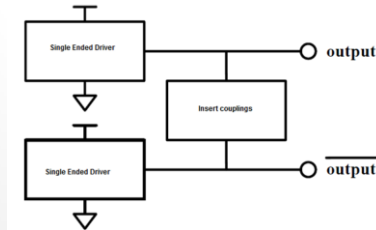
- Verilog-A can work with existing (generic) series model to provide extra accuracy if needed.

Differential modeling flow:



Modeling flow validation:

- Use an existing single-ended driver for P and N
- Insert approximate non-linear behavioral R/L/C elements between P and N outputs
- Flow should recreate same PU/PD/PC/GC as driver
- I-V surface plot should reveal inserted resistance
- C_Diff/C_Comp surface should reveal inserted cap
- Correlations of V-T table depends on I_Diff accuracies.



Summary:

- Verilog-A for differential V-T extraction
 - Versatile, supports many operators
 - E.g. `ddt(Vx)`, `$table_model` for 1D/2D lookup
 - Streamlines modeling flow
 - Extract transient differential current
 - Improve V-T extraction accuracies
 - Use Verilog-A to remove rigid series syntax
- External model for “Series”:
 - [External model] supports “Series” type model
 - Can work with generic series model



References:

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<http://accellera.org/images/downloads/standards/v-ams/VAMS-LRM-2-3-1.pdf>
6. HSpice User's Manual

Q & A



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