Quality checks for power aware IBIS models

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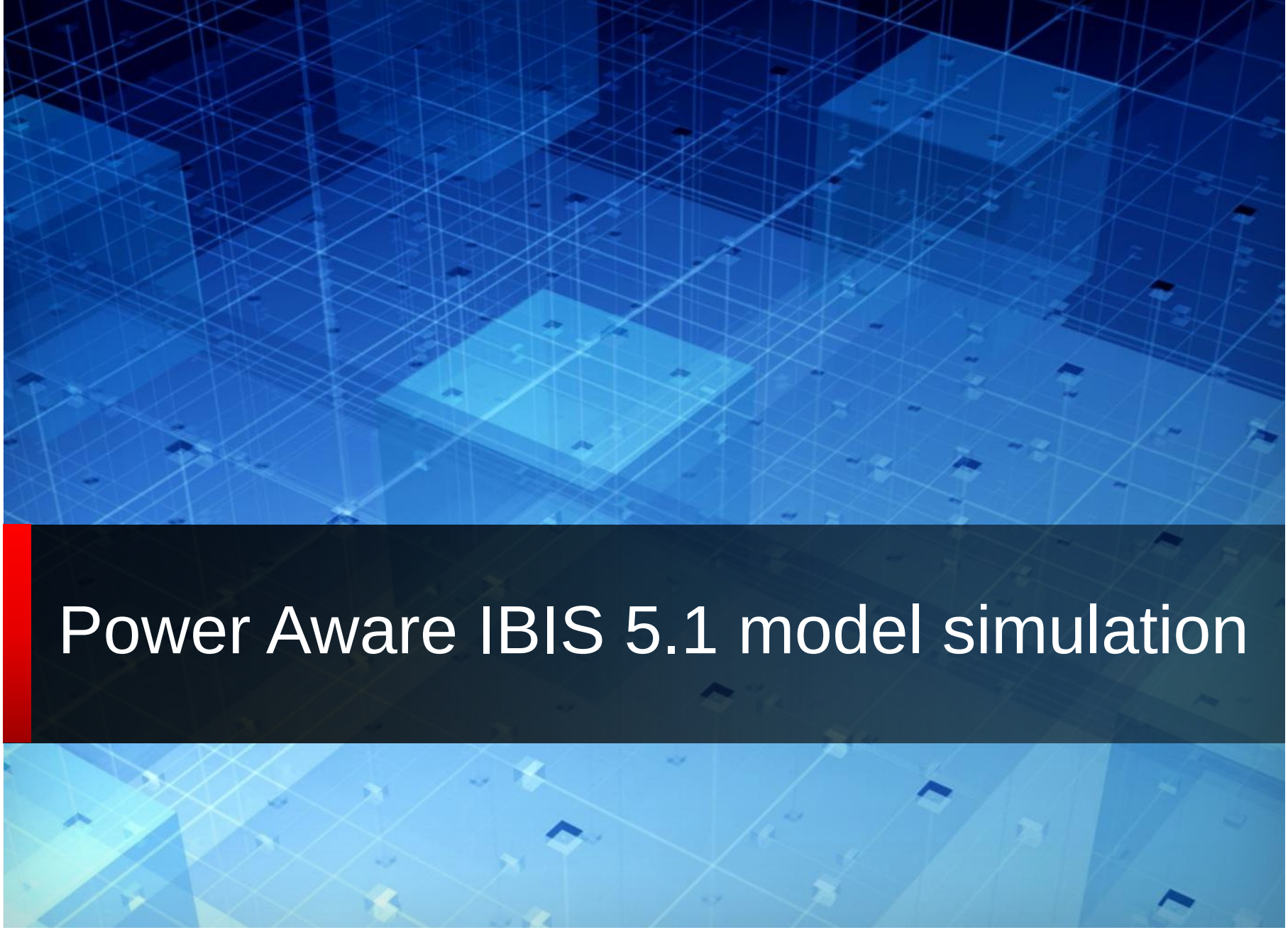
Agenda

- **Introduction**
- **Power aware IBIS 5.1 model simulation**
  1. Simulation with sinusoidal noise injected to power rail
  2. Simulation with parasitic of Power and Ground
- **Limitation with power aware IBIS 5.1 model**
- **Proposed solution**
- **Summary**

Introduction

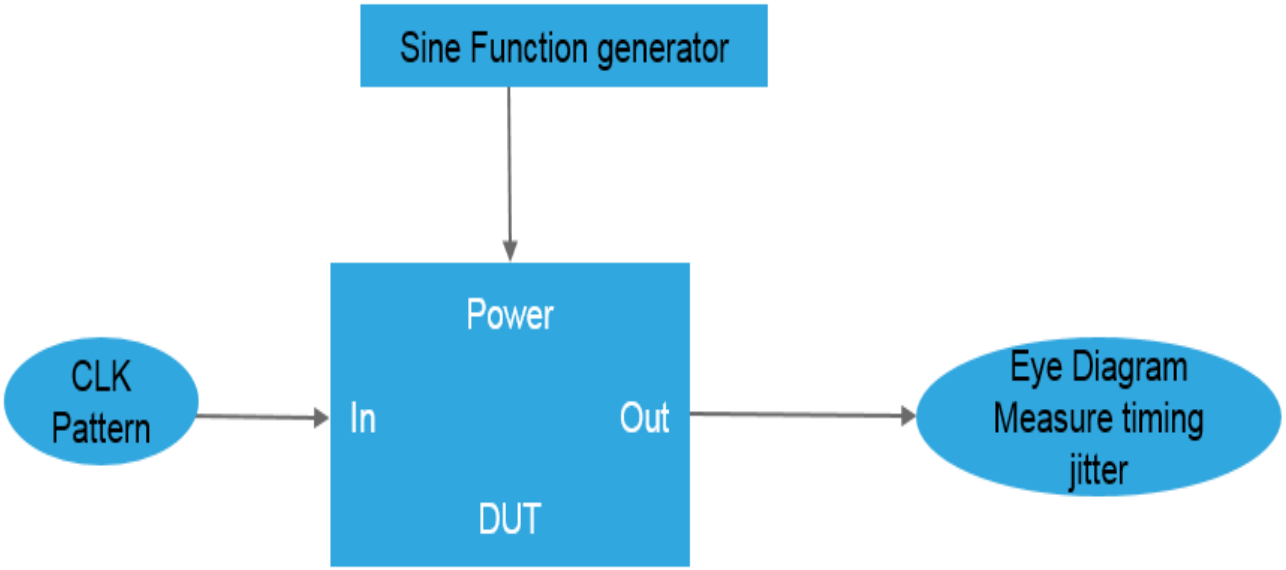
- IBIS 5.1 model is power aware with usage of keywords composite current and ISSO_PU/PD tables
- These keywords take into consideration pre-driver current and gate modulation i.e. driver strength variation due to simultaneously switching noise
- When power aware IBIS model is used in system level simulation power rail is subjected to noise
- IBIS should be sensitive enough to take these variations into account to achieve accurate results
- Quality checks that one should perform and possible solution to correlate with SPICE netlist results are presented
- 28nm-LPDDR4 has been used as a test case



Power Aware IBIS 5.1 model simulation

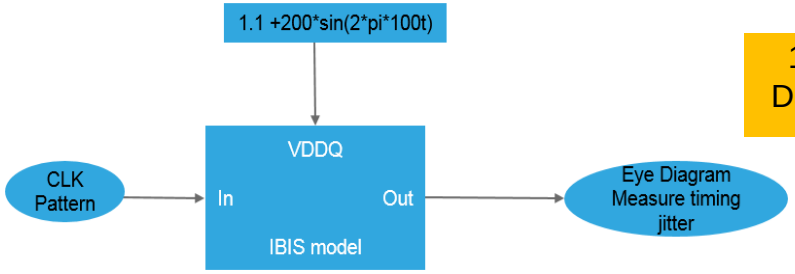
1st Quality Check: Simulation with sinusoidal noise injected to power rail

Setup to measure the jitter sensitivity

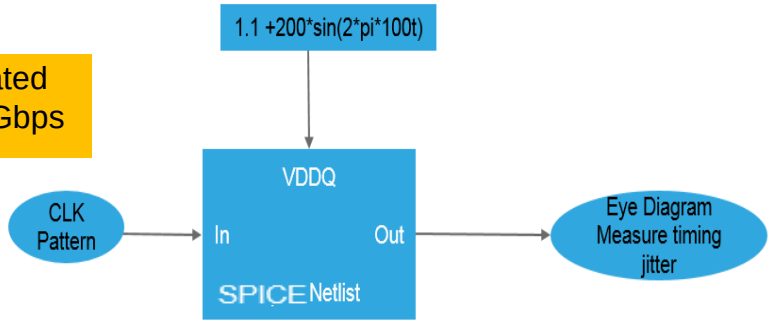


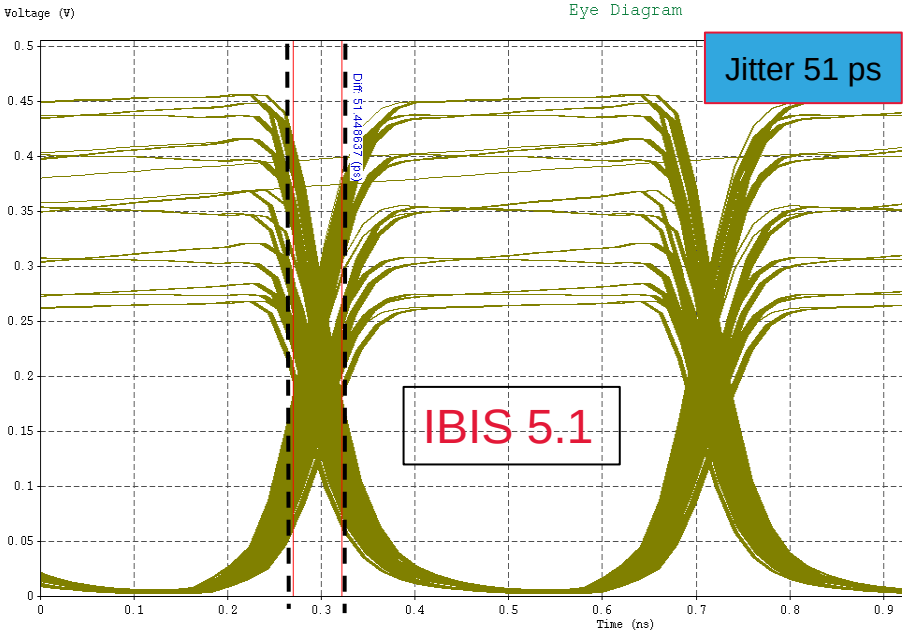
Mismatch in timing jitter

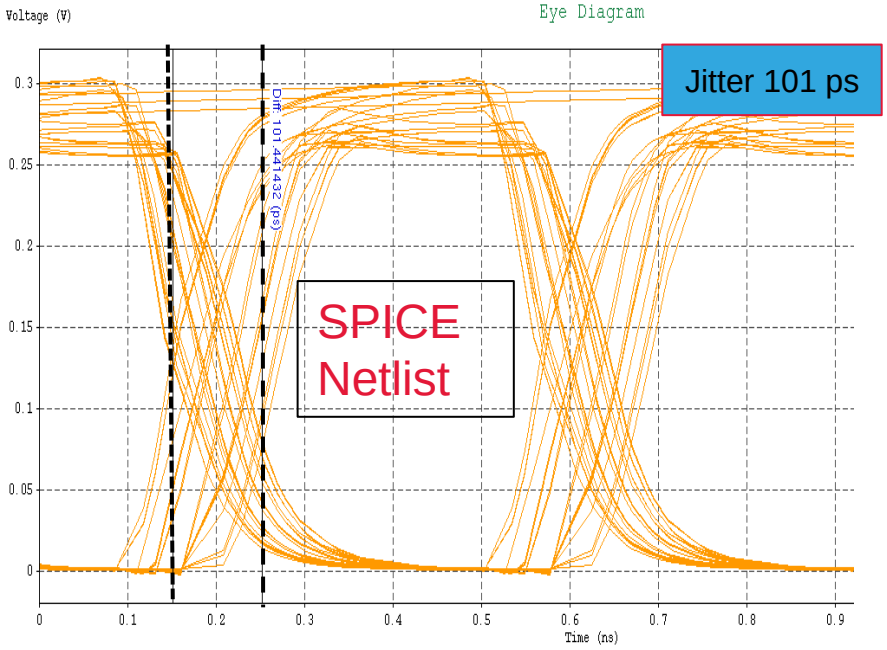
Case1: 100 MHz 200mV p2p sinusoidal noise injected on power rail



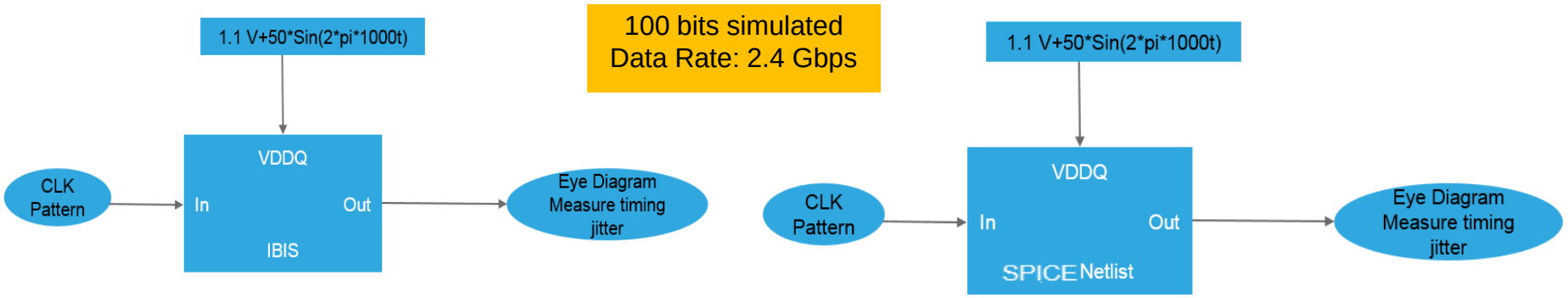
100 bits simulated
Data Rate: 2.4 Gbps

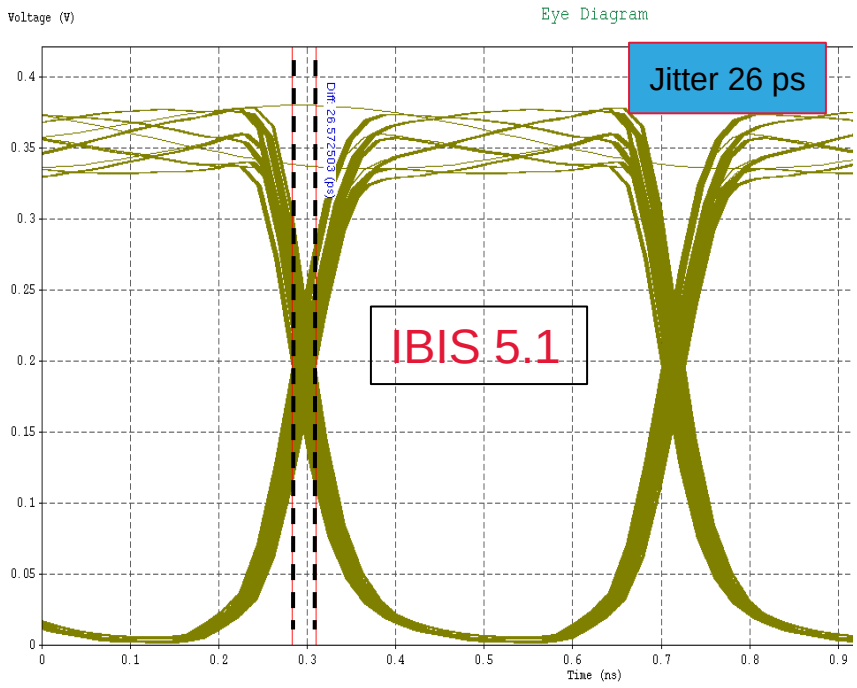


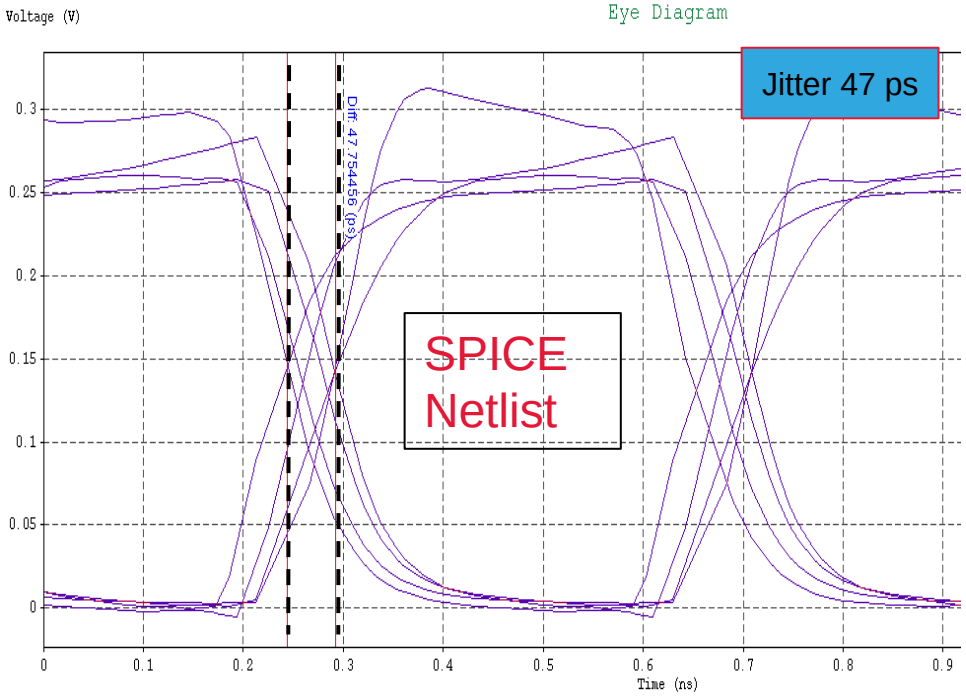




Mismatch in timing jitter
Case2: 1 GHz 50mV p2p sinusoidal noise on power rail

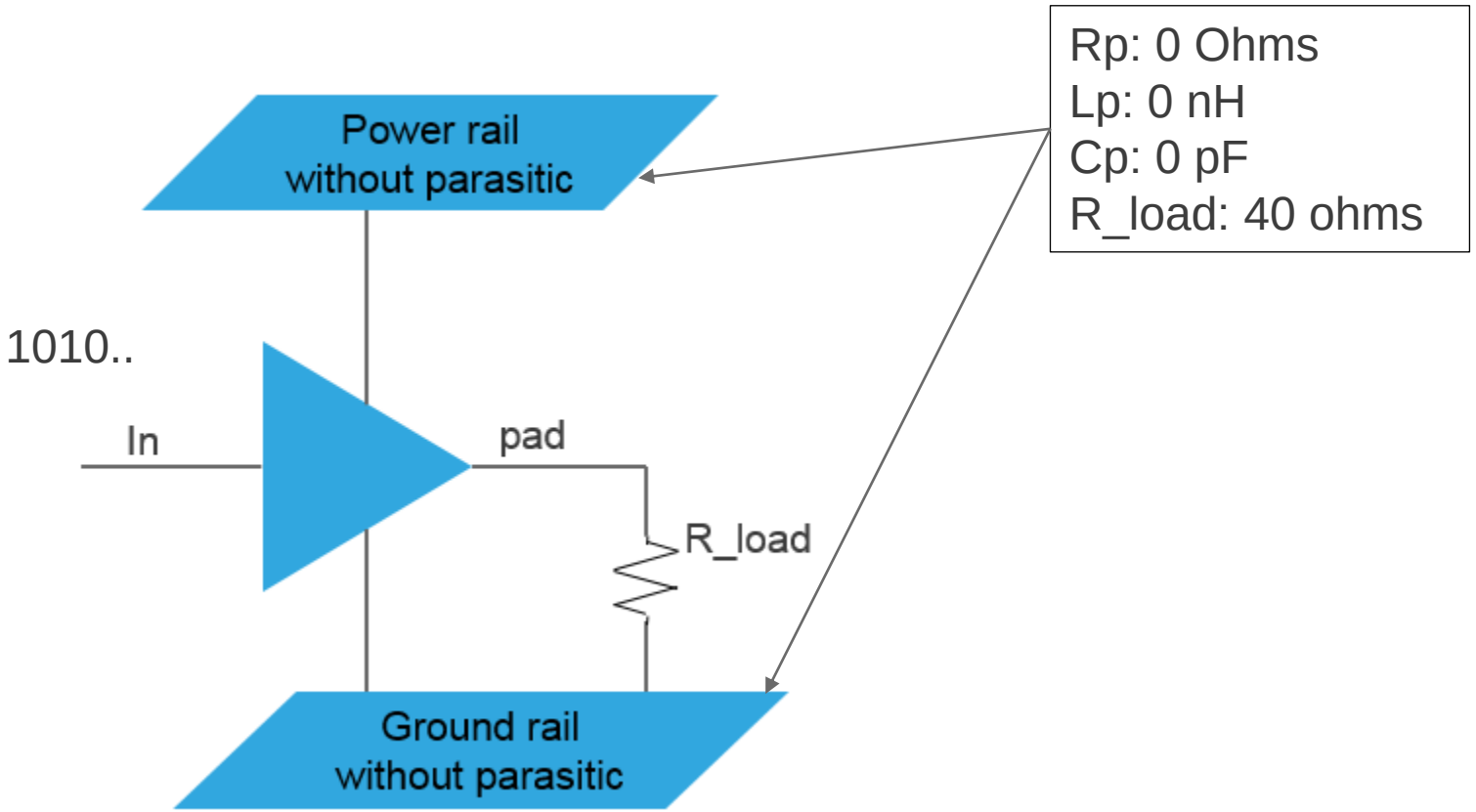






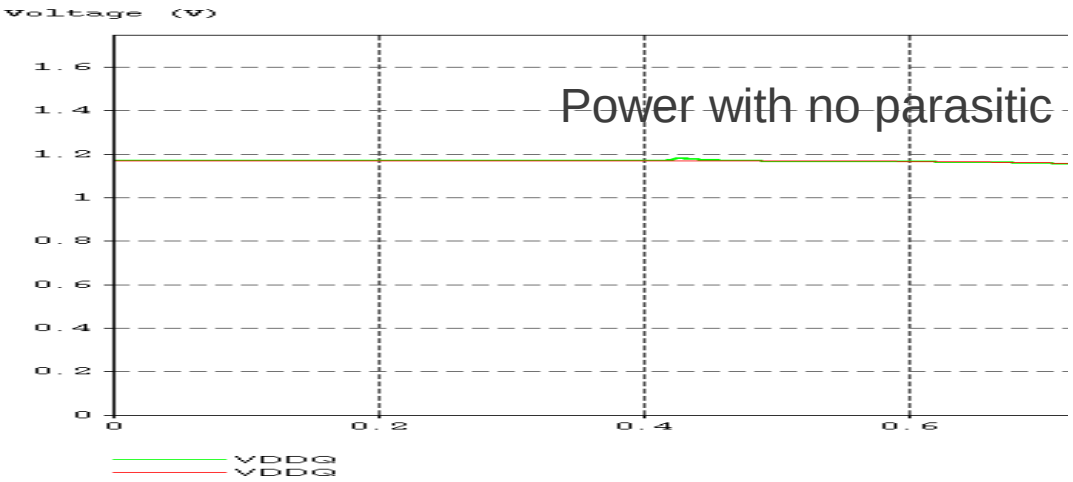
2nd Quality Check: Simulation with/without parasitic of power and ground

Case1: Correlation setup of Power/Ground rail without parasitic



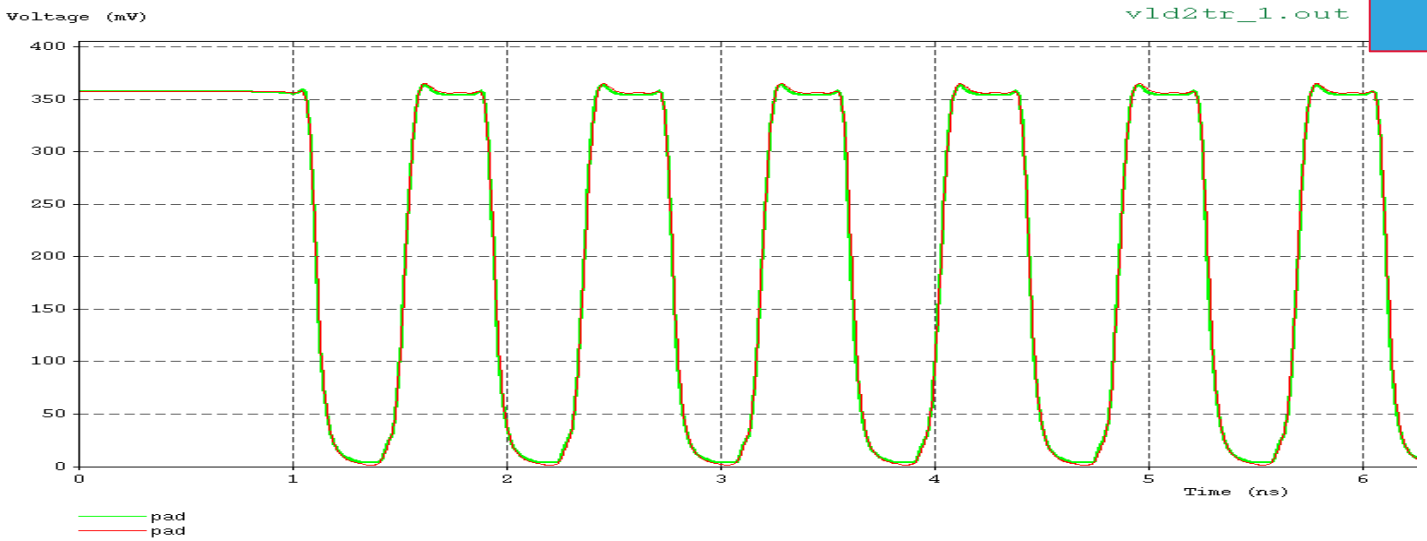
PAD waveform when power without any parasitic is used to do correlation with IBIS 5.1

IBIS
SPICE



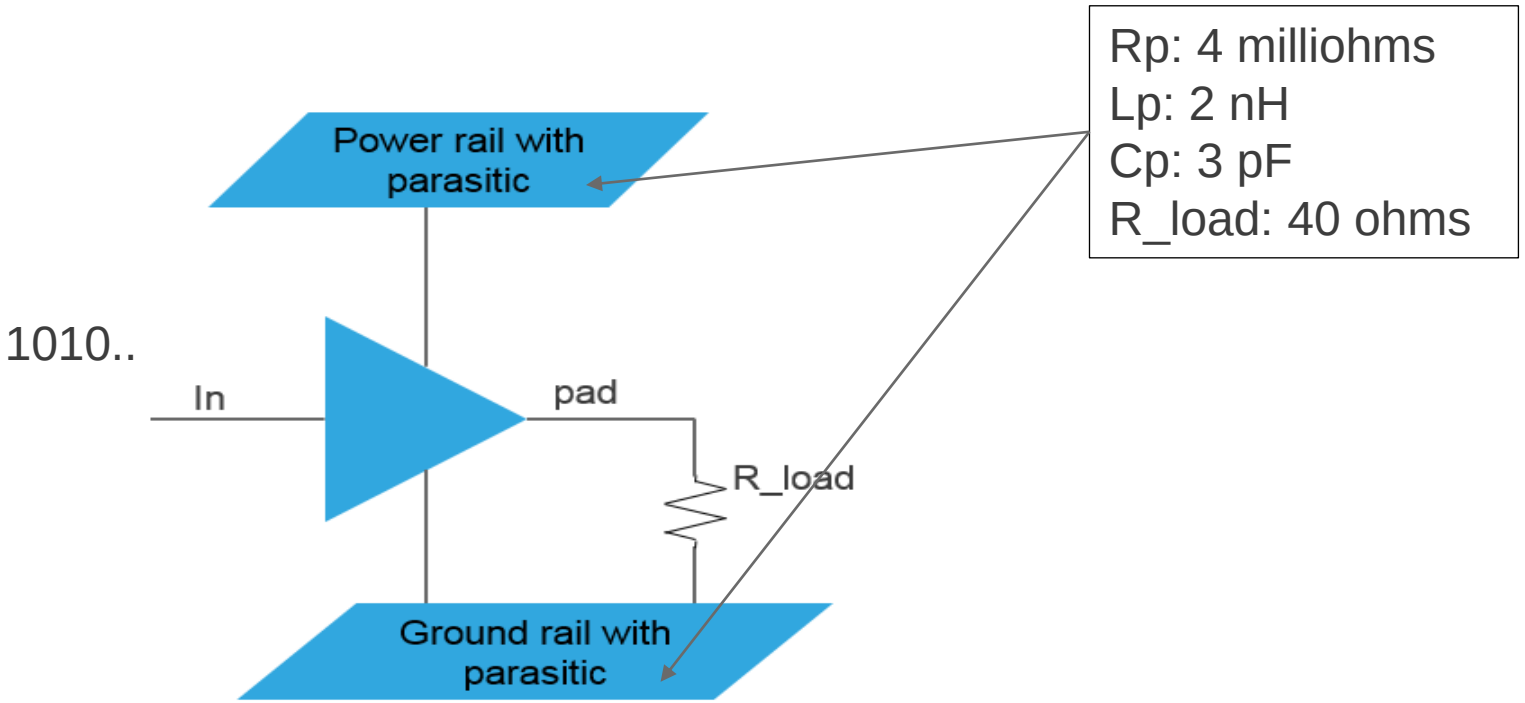
Power of IBIS and SPICE correlate well

FOM is 99.2%



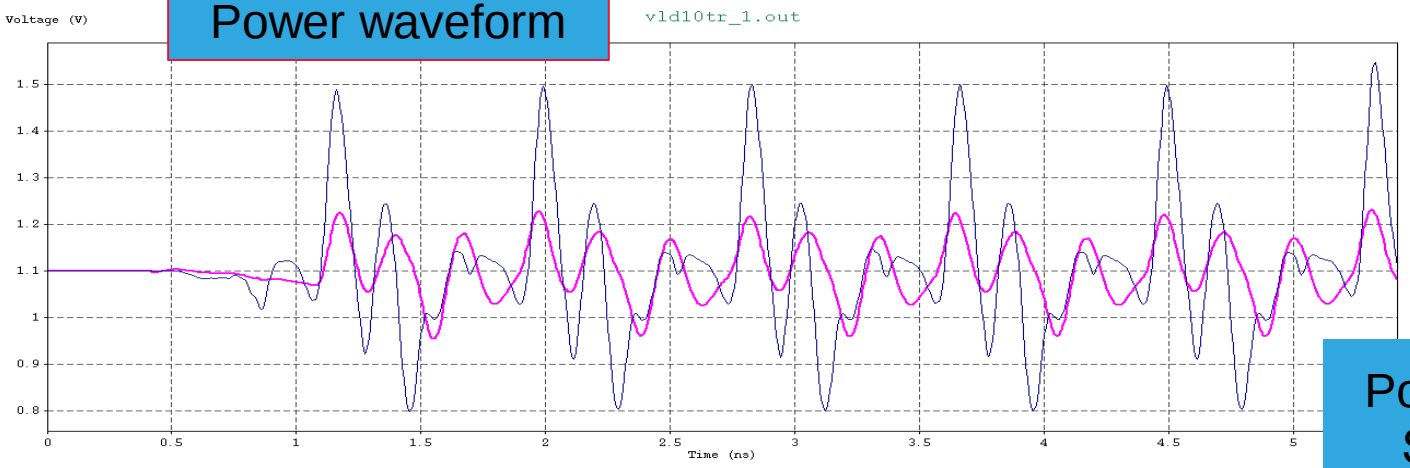
IBIS
SPICE

Case2: Correlation setup of Power/Ground rail with parasitic



With IBIS 5.1 IBIS model

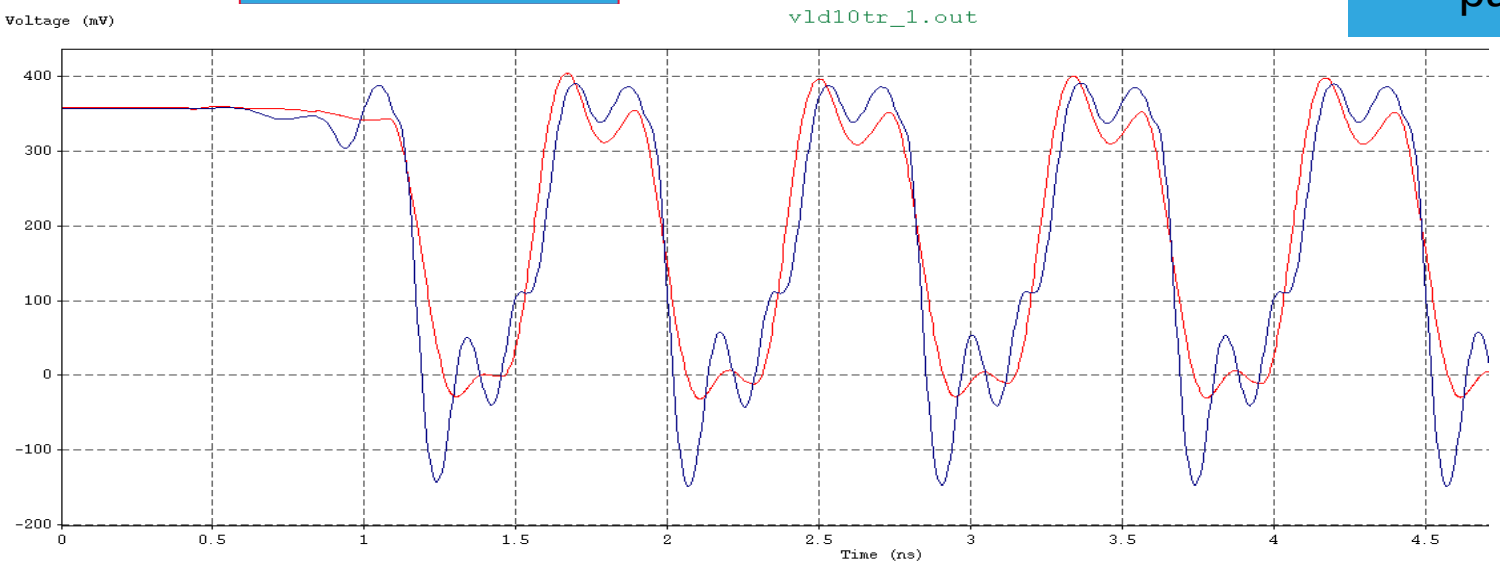
Power waveform



IBIS
SPICE

Power of IBIS and SPICE doesn't correlate so is the pad voltage

PAD waveform



FOM is 93.4%

IBIS
SPICE

Limitation with power aware IBIS 5.1

IBIS 5.1 model limitation

- IBIS 5.1 underestimates power supply variation into signal jitter
- IBIS 5.1 correlation with SPICE netlist fails when power/ground rail is subject to parasitic

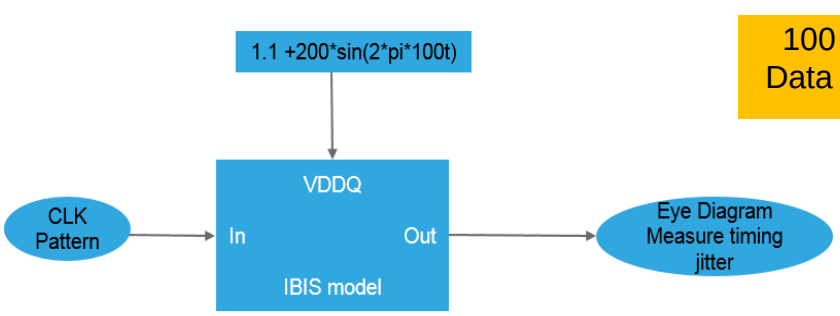
Proposed solution

Proposed solution for Case1
IBIS 5.1 with power variation to account for Power Supply Noise Induced Jitter

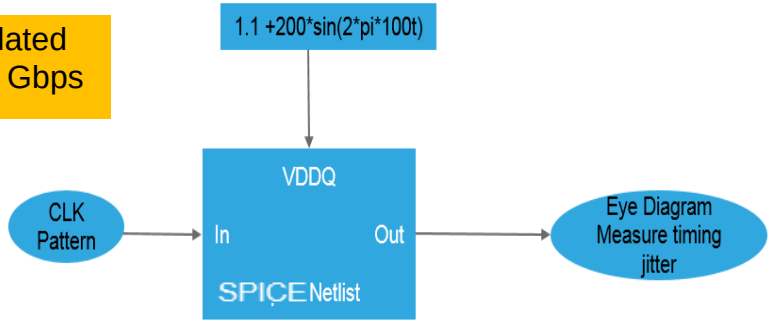
- Jitter occurs due to change in IO buffer delay and buffer delay is a function of the supply voltage
- In order to model jitter due to power supply. We can use typical, min and max waveforms with only variation in terms of voltage whereas process, temperature remains same and overlap these 3 waveforms to account for PSNIJ
- Variation of +/-5% is accounted from typical voltage of 1.1 V (lpddr4 power supply) to fetch three waveforms and all of them over lapped to generate eye diagram

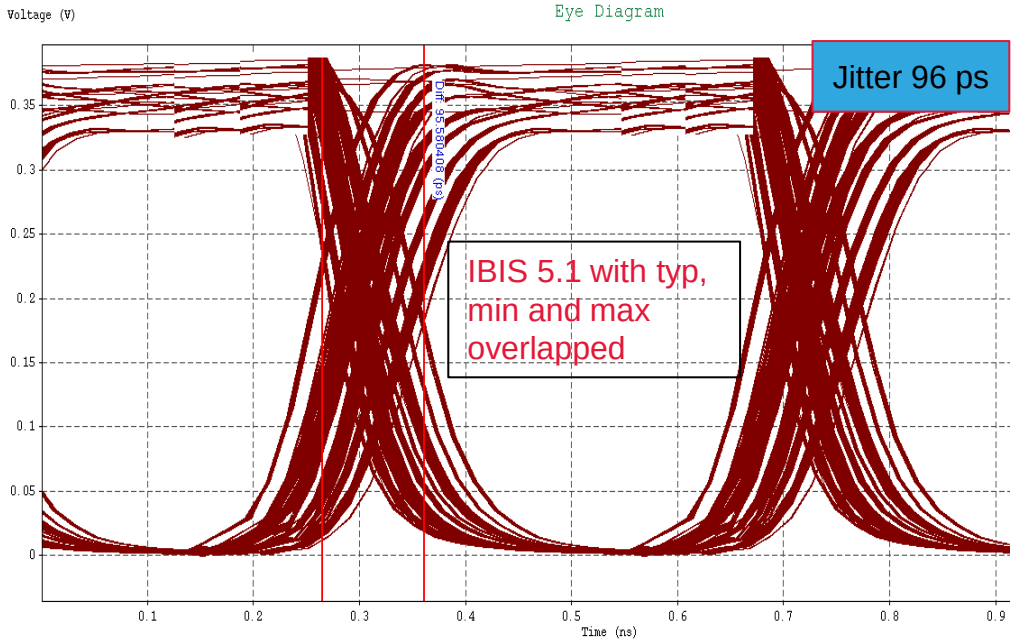
Improved matching in timing jitter

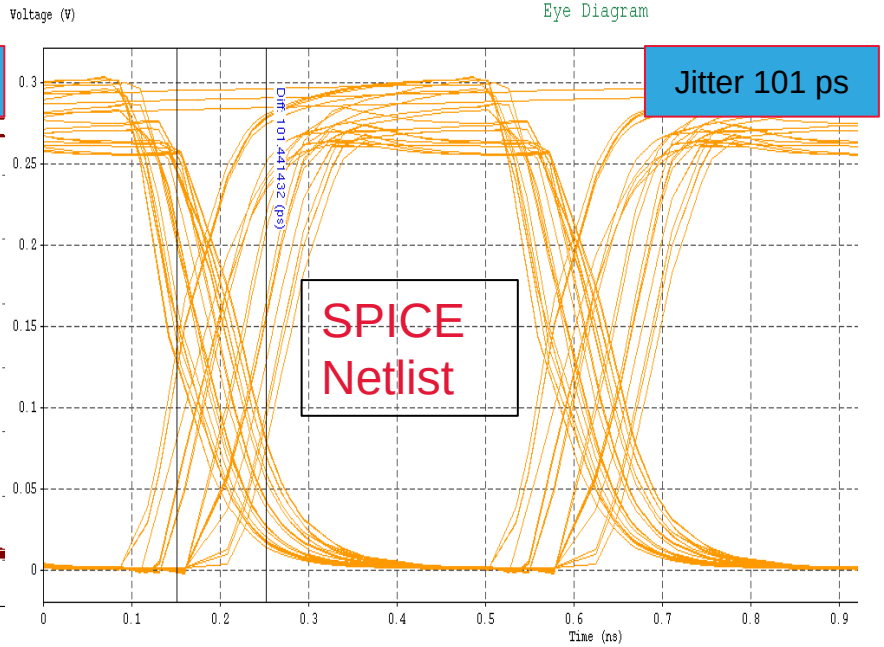
Case1: 100 MHz 200mV p2p sinusoidal noise on power rail



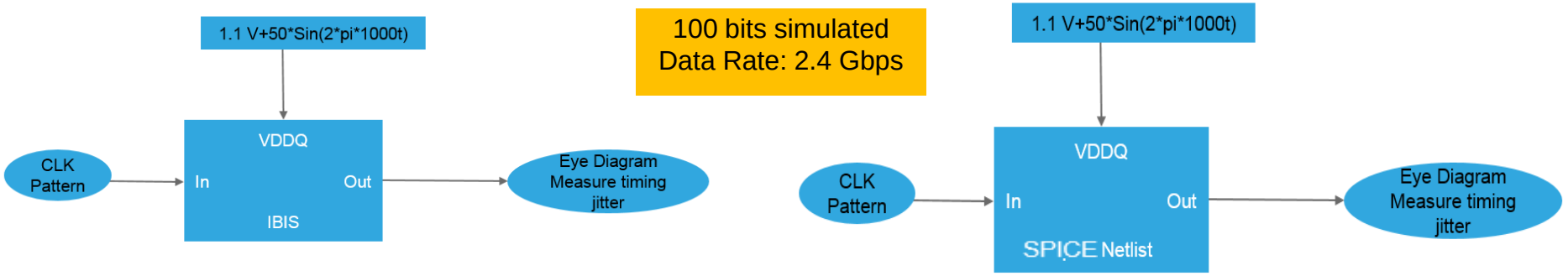
100 bits simulated
Data Rate: 2.4 Gbps

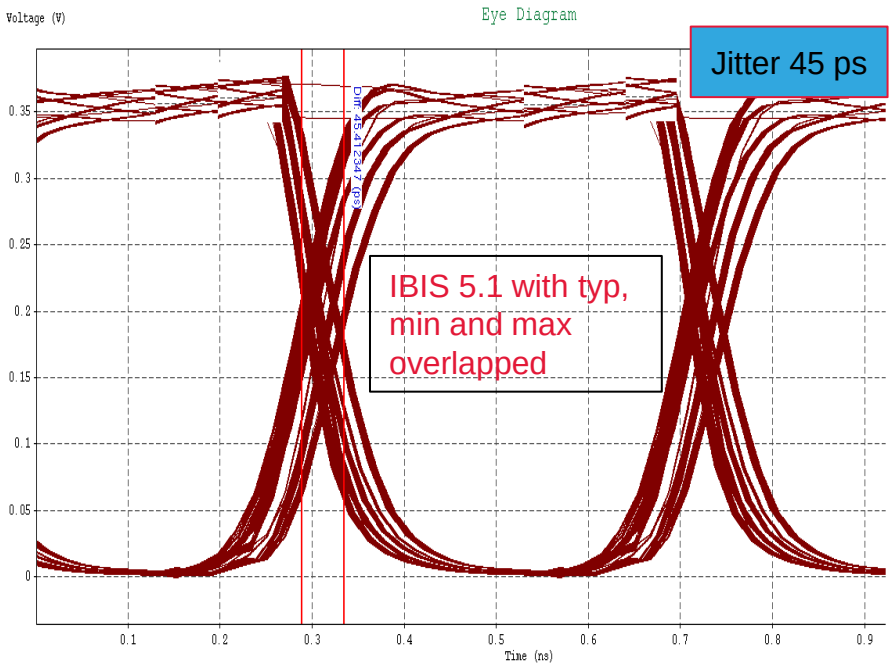


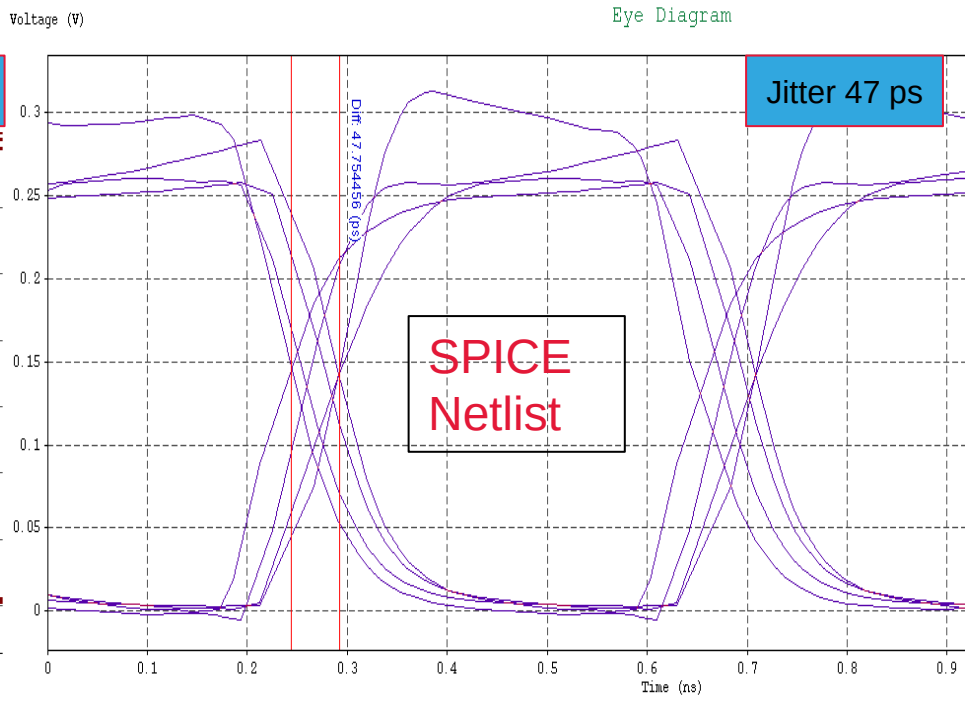




Improved matching in timing jitter
Case2: 1 GHz 50mV p2p sinusoidal noise on power rail







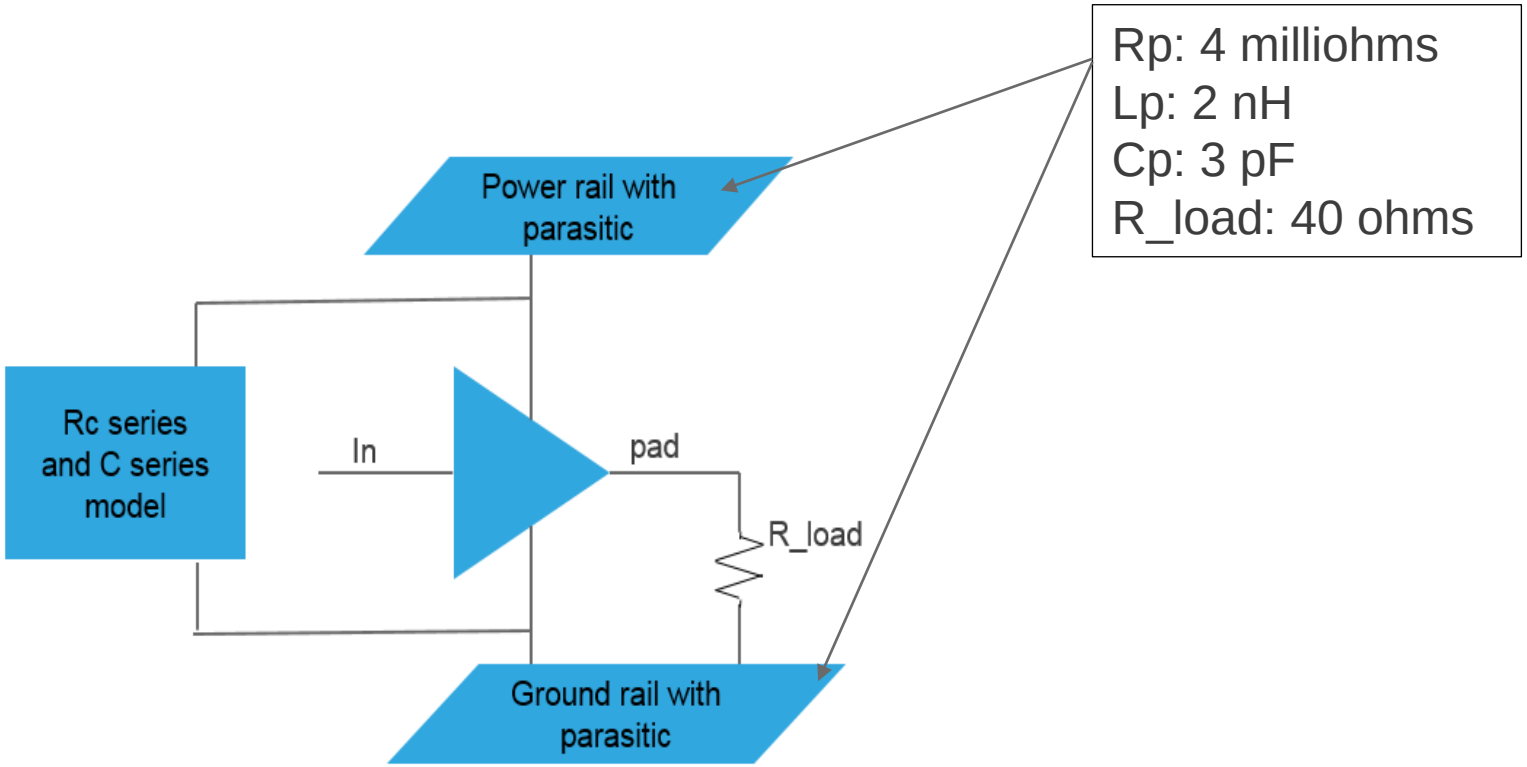
Remarks

- Wherein with new proposed solution one can come close to jitter seen with spice netlist
- To further improve the accuracy more variation in power voltage may be included to account for PSNIJ

Proposed solution for Case2

- R and C between power and ground have to be explored in order to match impedance between power and ground plane

- Setup with Rc series and C series model added to IBIS 5.1 model



IBIS 5.1 + Rc series and C series

```
[Pin]  signal_name          model_name           R_pin     L_pin     C_pin
PAD    PAD                 lpddr4_60_40
|IN    IN                   dummy
|enout enout                dummy
vssq   vssq_die             GND
vccq   vccq_die             POWER
|
[Series Pin Mapping]  pin_2        model_name        function_table_group
vccq   vssq                 vccq_vssq_cap
```

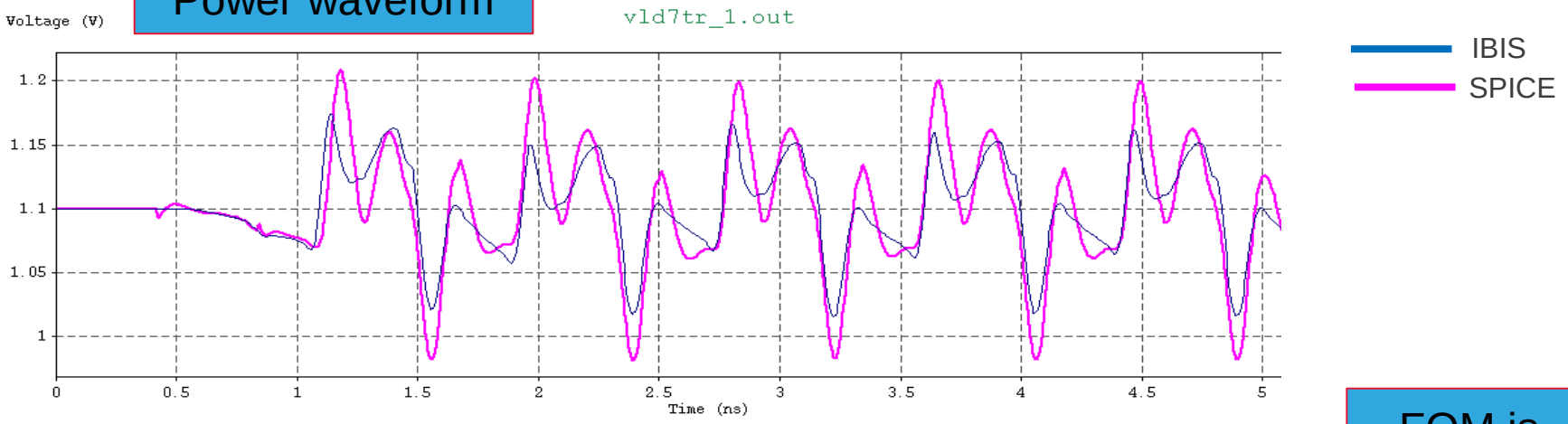
```
|*****************************************************************************
|                        Model vccq_vssq_cap
|*****************************************************************************
|
[Model] vccq_vssq_cap
Model_type Series
C_comp    0.0F              NA                   NA
|
[Temperature Range]    50.000            0.110k              0.0
[Voltage Range]         1.500V            1.425V              1.575V
|  variable          C(typ)           C(min)            C(max)
[C Series]          0.452n           0.452n              0.453n
|  variable          R(typ)           R(min)            R(max)
[Rc Series]         2.186            2.187               2.185

[End]
```

A model to be calculated in order to match impedance between power and ground

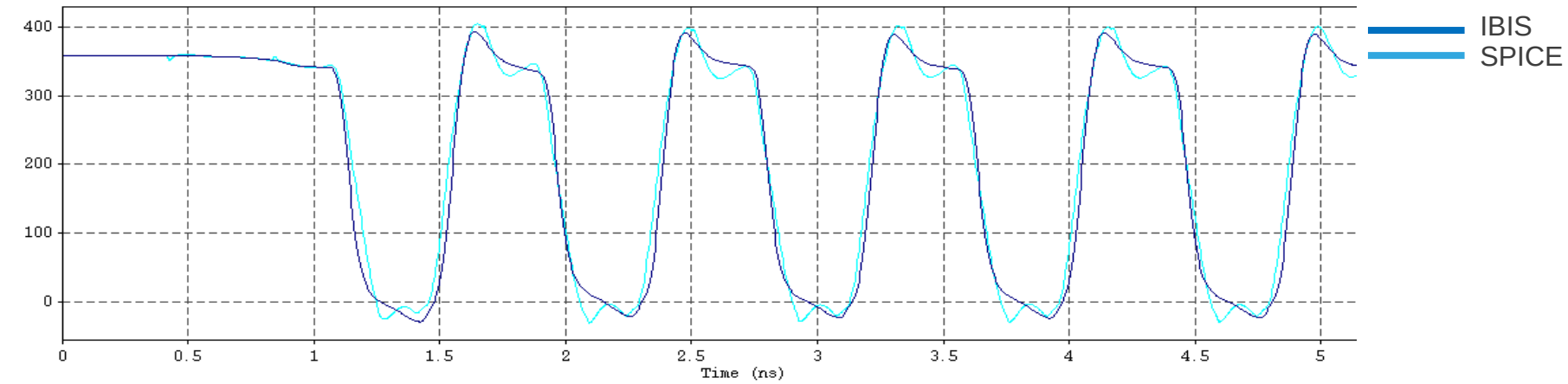
With IBIS 5.1 + [Rc and C series] model

Power waveform



FOM is 97.8%

PAD waveform



Remark:

More accurate RC model can be computed using computational algorithms

Summary

Summary

- Such storage of power voltage variation and storage of delay can be dumped into a file and this file can be used to show the variation of timing jitter by EDA tool
- Series model can be calculated by EDA tool to match the impedance of power and ground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