**ASIAN IBIS SUMMIT (TOKYO) AGENDA**

Time/Date: Friday, November 18, 2016, 12:30 to 17:30

**Organizational Sponsors:**

 **Japan Electronics and Information Technology**

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 **IBIS Open Forum**

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12:30 **SIGN IN**

13:00 **MEETING WELCOME**

 Shogo FUJIMORI (Fujitsu Advanced Technologies,

 Chair JEITA IBIS Promotion WG)

 Mike LaBONTE (Signal Integrity Software (SiSoft),

 Chair IBIS Open Forum)

13:10 **IBIS Chair's Report**

 Mike LaBONTE (Signal Integrity Software (SiSoft)

13:25 **IBIS Promotion Working Group Report**

 Shogo FUJIMORI (Fujitsu Advanced Technologies, Japan)

13:40 **Differential Modeling Flow with Series Model in Verilog-A**

 Wei-hsing HUANG\* and Sanjeev GUPTA\*\*

 (\*SPISim, USA and \*\*Sigintegrity Solutions, India)

 [Presented by Wei-hsing HUANG (SPISim, USA)]

14:10 **Is Typical Analysis Enough? What Is Corner Condition?**

 Shinichi MAEDA (KEI Systems, Japan)

14:35 **Embedded DDR4 Design Simulation**

 Yukio MASUKO\* and Shinichi MAEDA\*\*

 (\*Japan Electronics Packaging and Circuit Association,

 \*\*KEI Systems, Japan)

 [Presented by Yukio MASUKO

 (Japan Electronics Packaging and Circuit Association)]

15:05 **BREAK**

15:25 **Quality Checks for Power Aware IBIS Models**

 Ashish GUPTA, Rameet PAI(Cadence Design Systems, India)

 [Presented by Takuya MORIYA

 (Cadence Design Systems, Japan)]

15:50 **Verification of PDN Design with Power Aware IBIS Model**

 Masaki KIRINAKA, Akiko TSUKADA

 (Fujitsu Interconnect Technologies Limited, Japan)

 [Presented by Akiko TSUKADA

 (Fujitsu Interconnect Technologies Limited, Japan)]

16:25 **IBISCHK6 V6.1.3 and Executable Model File Checking**

 Bob ROSS (Teraspeed Labs, USA)

 [Presented by Mike LaBONTE

 (Signal Integrity Software (SiSoft), USA)]

16:50 **Touchstone Conversion Wrapper**

 Anders EKHOLM (Ericsson, Sweden)

17:05 **IBIS Model - the Thankworthy Technology**

 Kazuhiko KUSUNOKI (WADOW, Japan)

17:20 **CONCLUDING ITEMS**

17:30 **END OF MEETING**

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