On-Die Decoupling Model Improvements for IBIS Power Aware Models

Randy Wolff and Aniello Viscardi

Micron Technology

Asian IBIS Summit

November 14, 2016, Taipei, Taiwan

(Previously given at the European IBIS Summit

May 11, 2016 Turin, Italy)

©2016 Micron Technology, Inc. All rights reserved. Information, products, and/or specifications are subject to change without notice. All information is provided on an "AS IS" basis without warranties of any kind. Statements regarding products, including regarding their features, availability, functionality, or compatibility, are provided for informational purposes only and do not modify the warranty, if any, applicable to any product. Drawings may not be to scale. Micron, the Micron logo, and all other Micron trademarks are the property of Micron Technology, Inc. All other trademarks are the property of their respective owners.

Outline

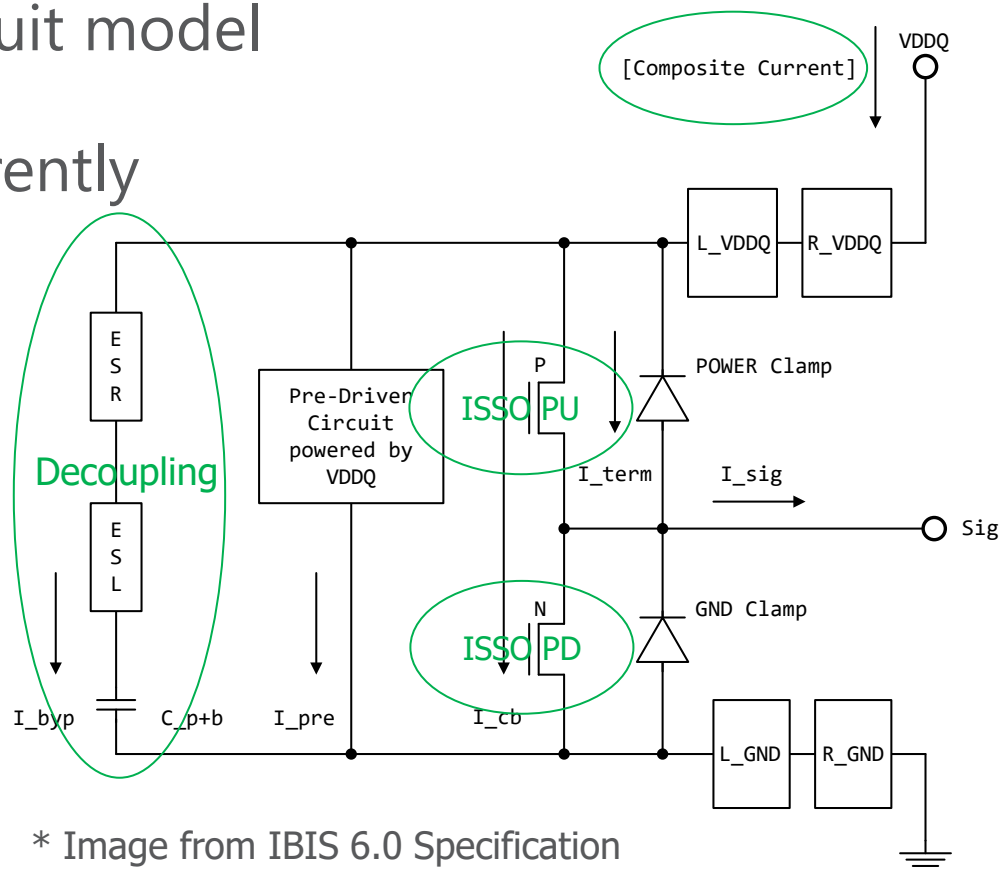
- IBIS Power-aware modeling overview
- On-die Decoupling models
- Multi-port Decoupling models
- Example Simulations
- Conclusions

© 2016 Micron Technology, Inc.

IBIS Power-aware Modeling Overview

- Power Integrity modeling uses [Composite Current], [ISSO PU], [ISSO PD] and an IBIS-ISS on-die decoupling circuit model
- Decoupling model external to IBIS currently

```
I_byp     - Bypass current
I_pre     - Pre-Driver current
I_cb      - Crow-bar current
I_term    - Termination current (optional)
L_VDDQ    - On-die inductance of I/O Power
R_VDDQ    - On-die resistance of I/O Power
L_GND     - On-die inductance of Ground
R_GND     - On-die resistance of Ground
C_p+b     - Bypass + Parasitic Capacitance
ESR       - Equivalent Series Resistance for on-die Decap
ESL       - Equivalent Series Inductance for on-die Decap
```

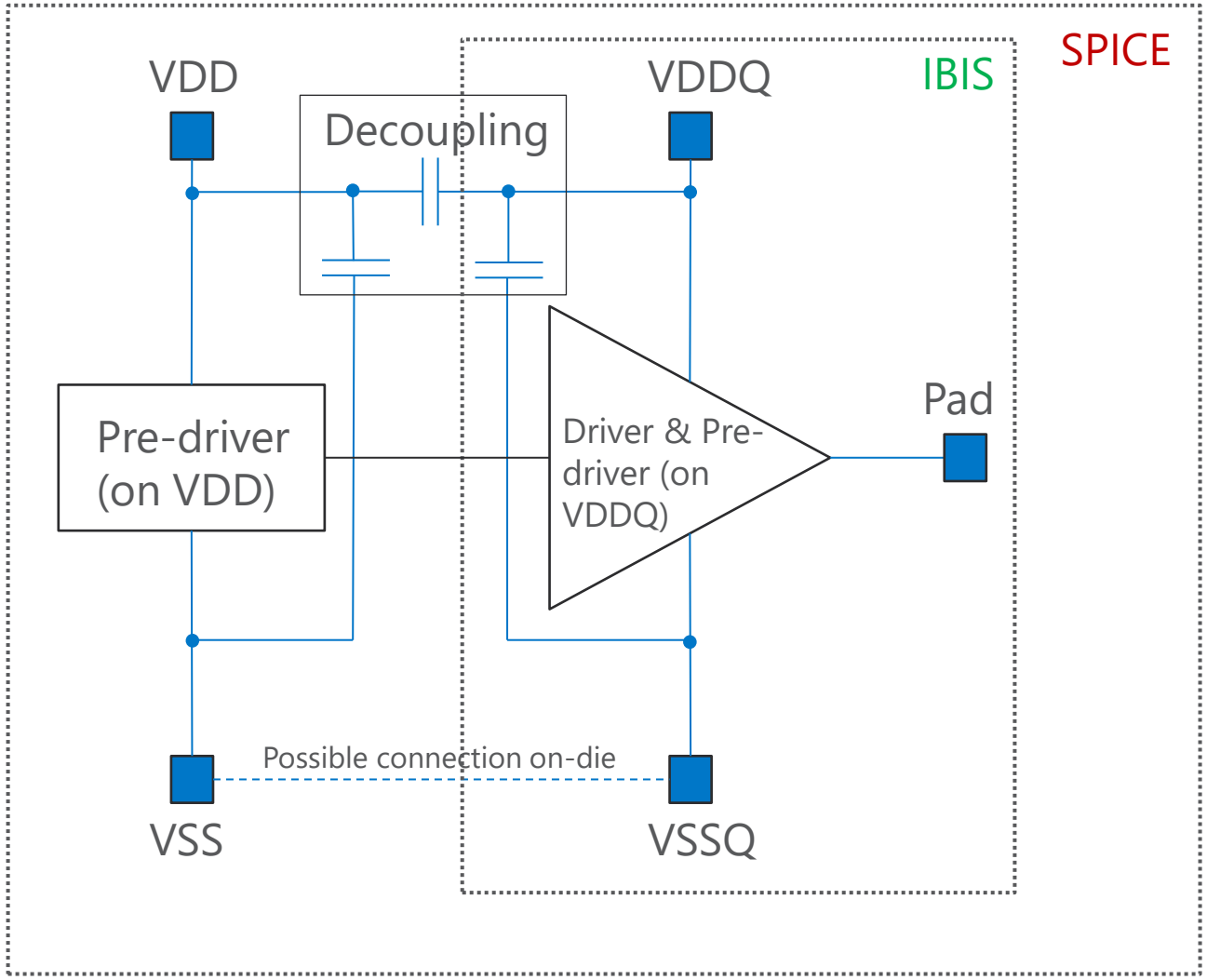


* Image from IBIS 6.0 Specification

© 2016 Micron Technology, Inc.

On-die Decoupling Models

- SPICE model may have pre-driver circuits on separate power supplies
- May be one common ground on-die
- Decoupling model could include VDDQ, VSSQ, VDD, VSS
- What is needed for IBIS to correlate with SPICE?



© 2016 Micron Technology, Inc.

Multi-port Decoupling Models

- Decoupling circuits may contain proprietary modeling equations or process data
- A non-proprietary model can be an S-parameter or a broadband SPICE macromodel (of the S-parameter characterization)
- S-parameter port options
  - 1-port: VDDQ with VSSQ reference
  - 2-port: VDDQ, VSSQ, with 0 reference
  - 3 or [4] port: VDDQ, VSSQ, VDD, [VSS], with 0 reference

© 2016 Micron Technology, Inc.

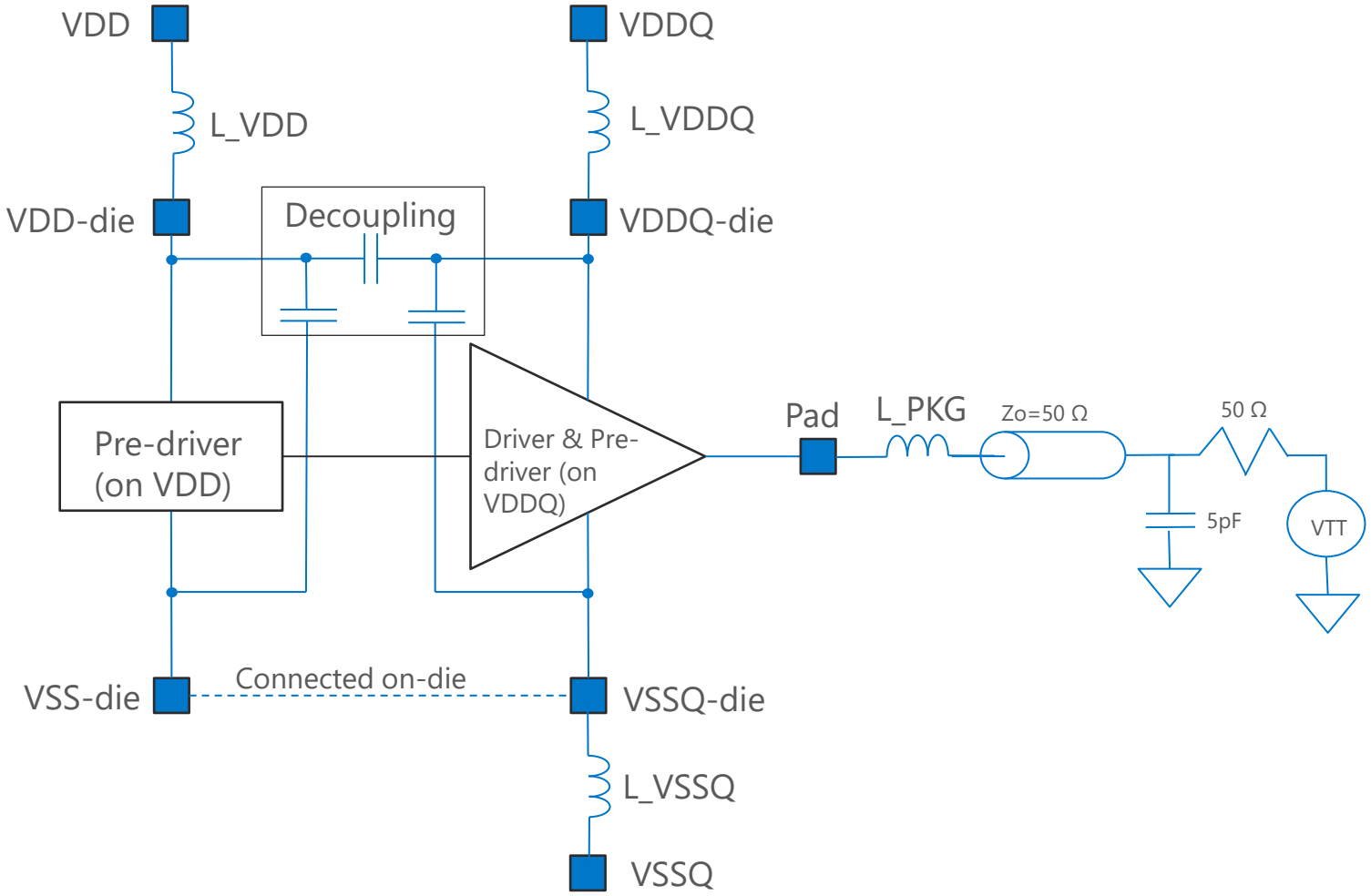
SPICE Setup Examples for Decoupling Model Creation

- Buffer Instance in Hi-Z state:
  - Xbuff … VDDQ_die VSSQ_die … Buffer_name
- Port Definition:
  - Single Port
    - P1 VDDQ_die VSSQ_die port=1 Z0=50 DC VDDQ
  - Multi Port
    - P1 VDDQ_die 0 port=1 Z0=50 DC VDDQ
    - P2 VSSQ_die 0 port=2 Z0=50 DC 0
- AC Analysis
  - .lin sparcalc=1 filename='s_model.sNp' format=touchstone dataformat=ma freqdigit=10 spardigit=10
  - .ac dec 100 1 10e12

© 2016 Micron Technology, Inc.

Example Simulation 1 – Ideal VDD
Comparing Transistor-level and IBIS Model in SPICE

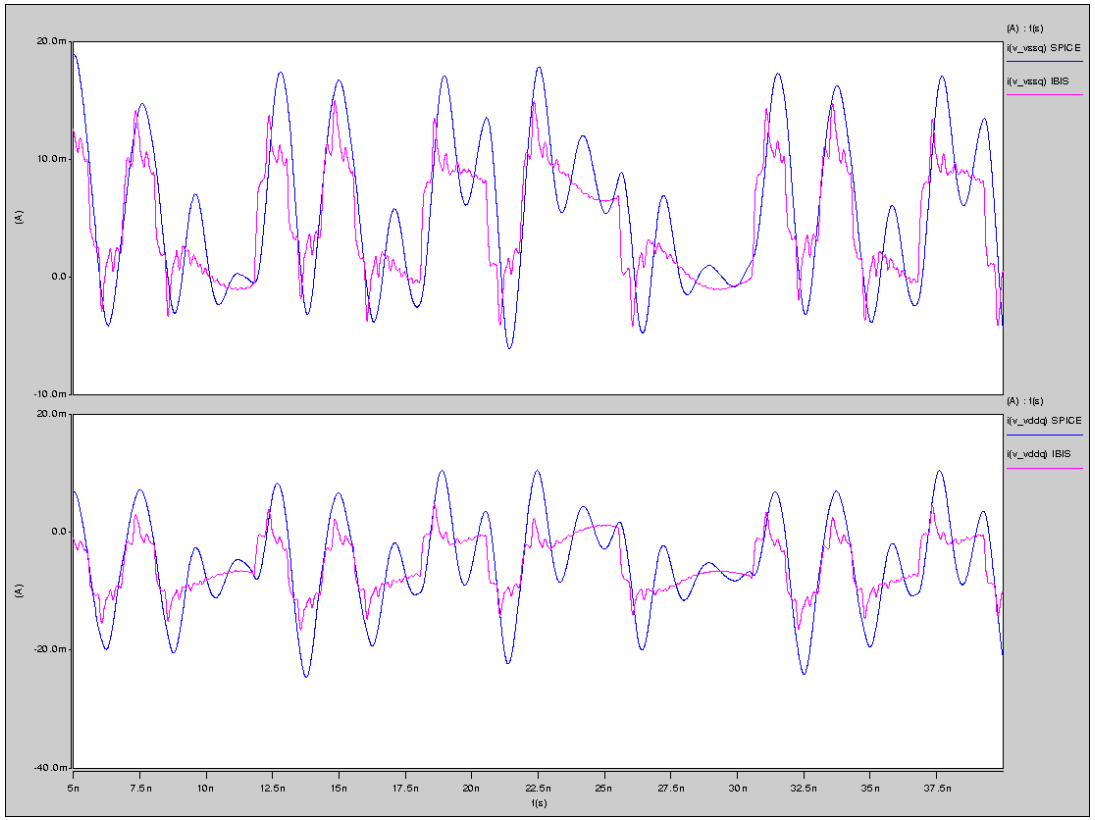
- L_VDD=0 (short)
- L_VDDQ=1.25nH
- L_VSSQ=1.25nH
- L_PKG=1.25nH



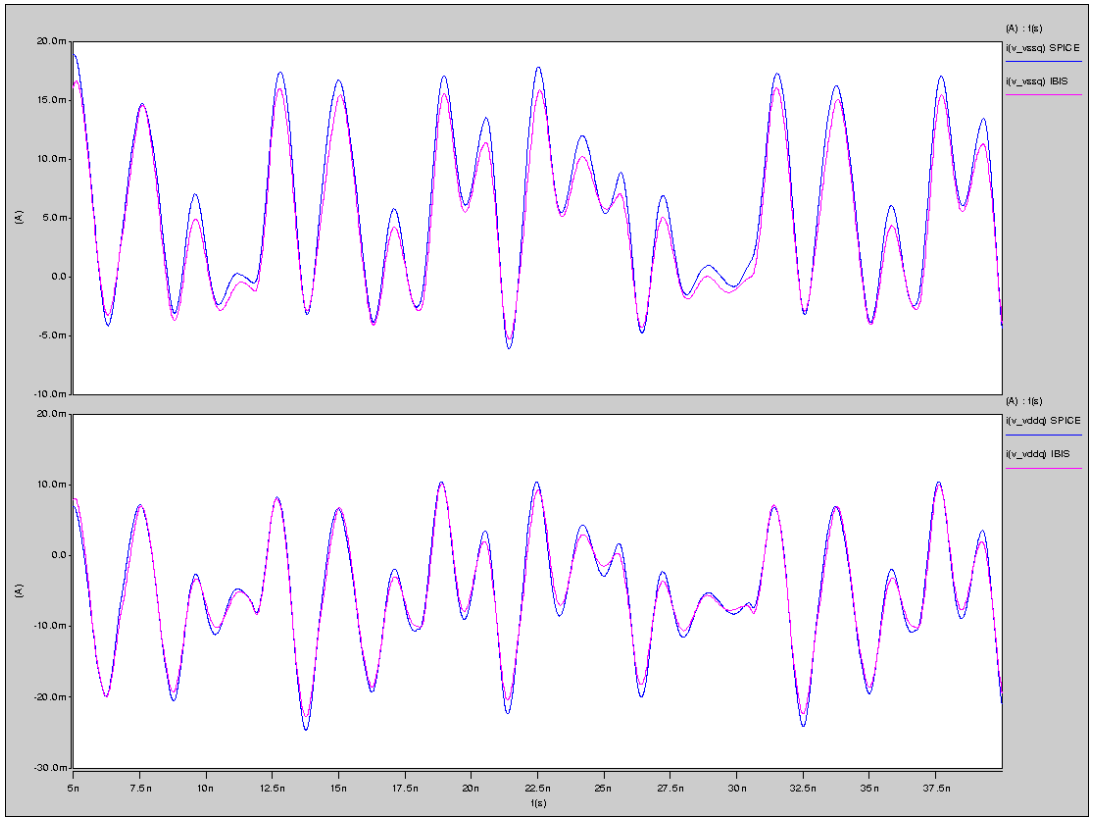
© 2016 Micron Technology, Inc.

1-Port vs. 2-Port Models, I(VSSQ) and I(VDDQ)

1-Port



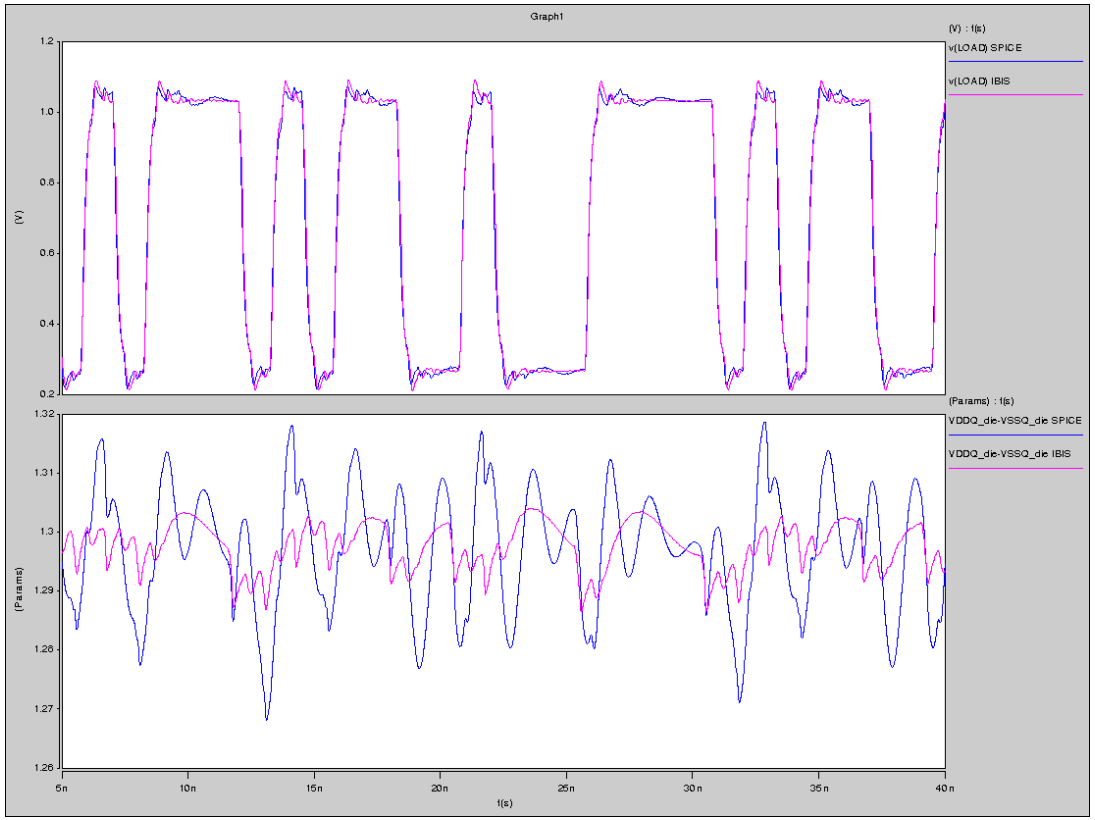
2-Port



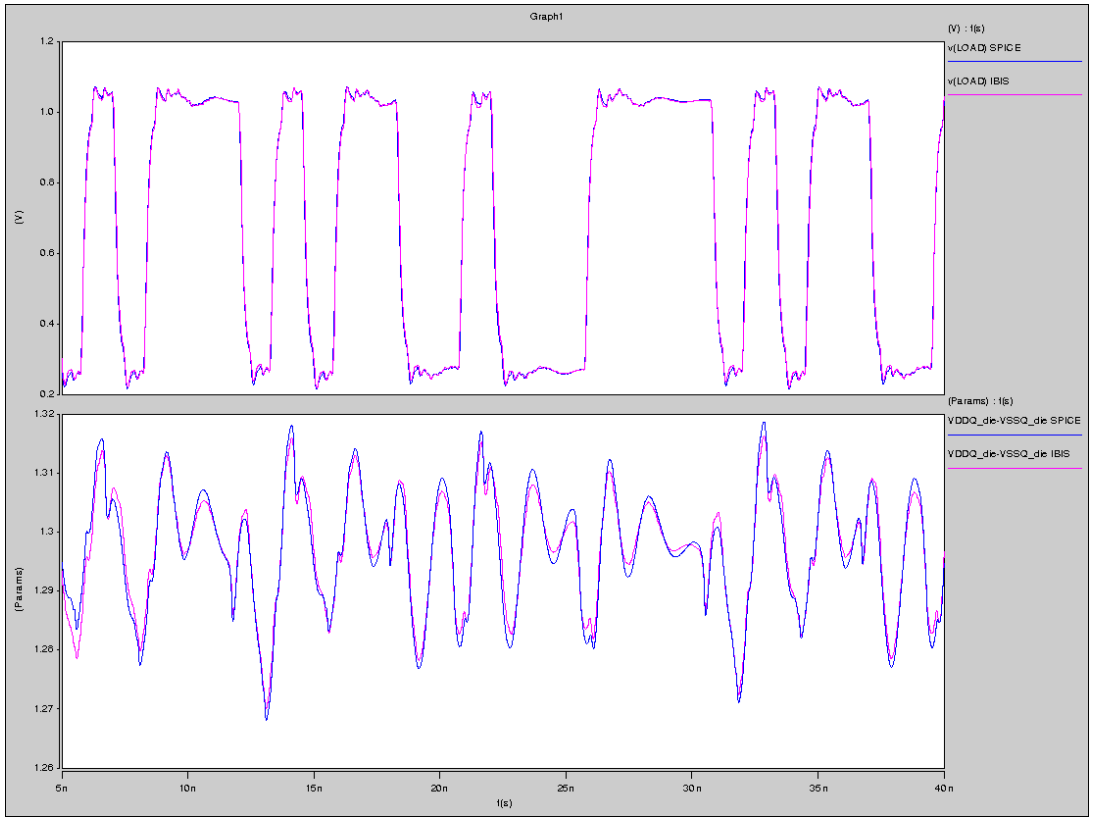
© 2016 Micron Technology, Inc.

V(LOAD) and V(VDDQ_die)-V(VSSQ_die)

1-Port



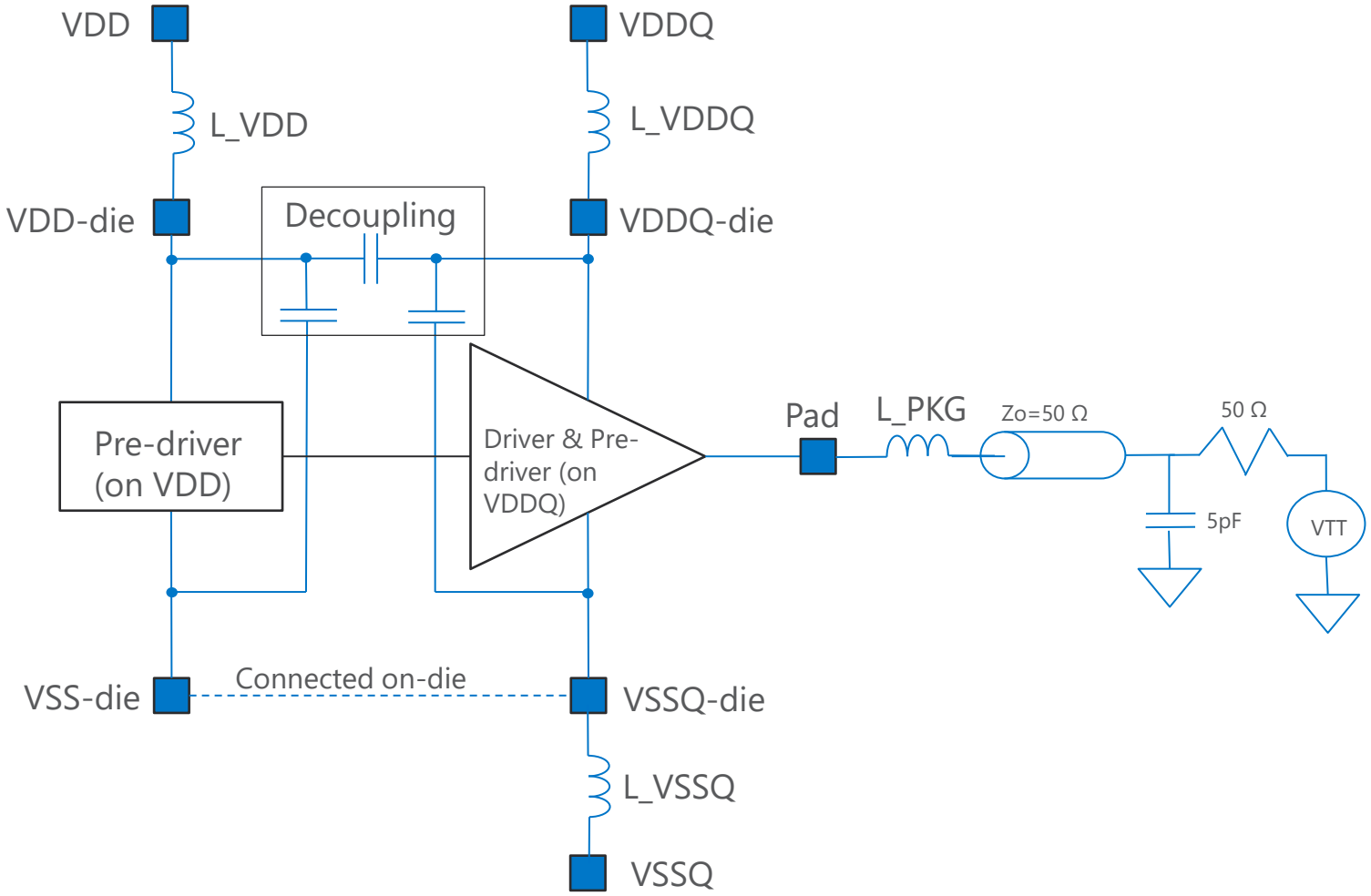
2-Port



© 2016 Micron Technology, Inc.

Example Simulation 2 – Non-ideal VDD
Comparing Transistor-level and IBIS Model in SPICE

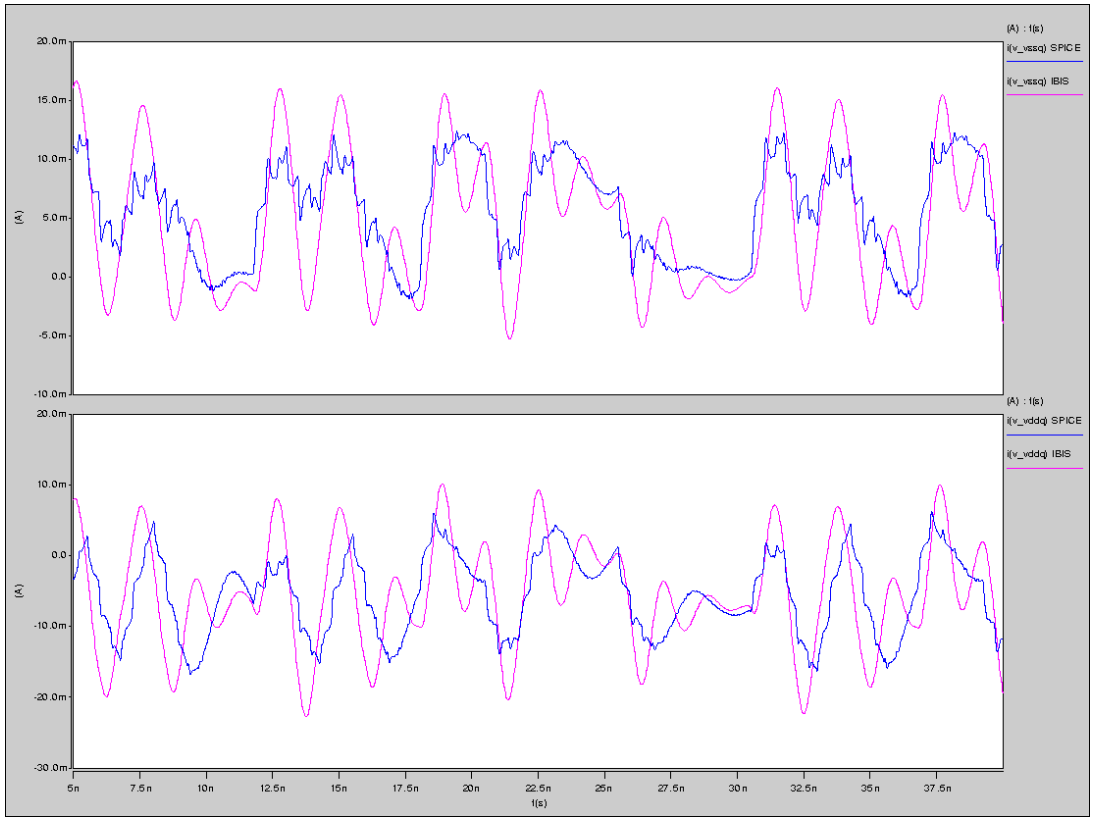
- L_VDD=1.25nH
- L_VDDQ=1.25nH
- L_VSSQ=1.25nH
- L_PKG=1.25nH



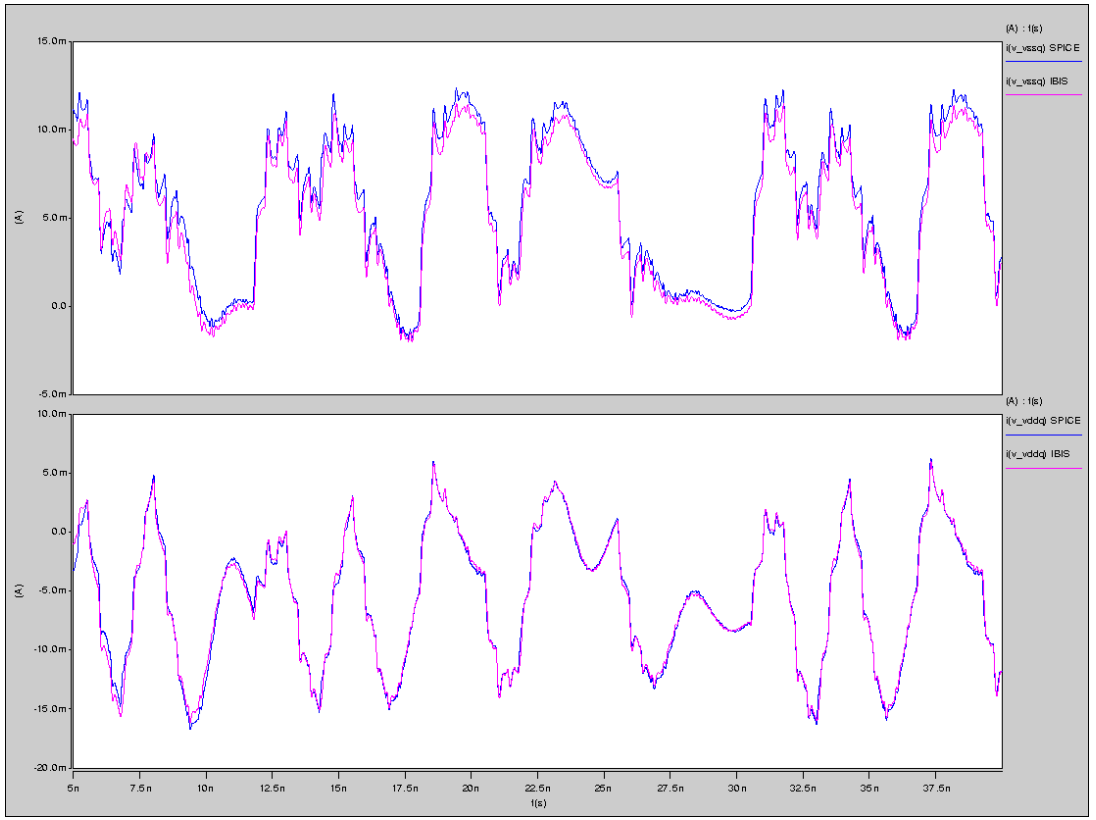
 © 2016 Micron Technology, Inc.

2-Port vs. 3-Port Models, I(VSSQ) and I(VDDQ)

2-Port



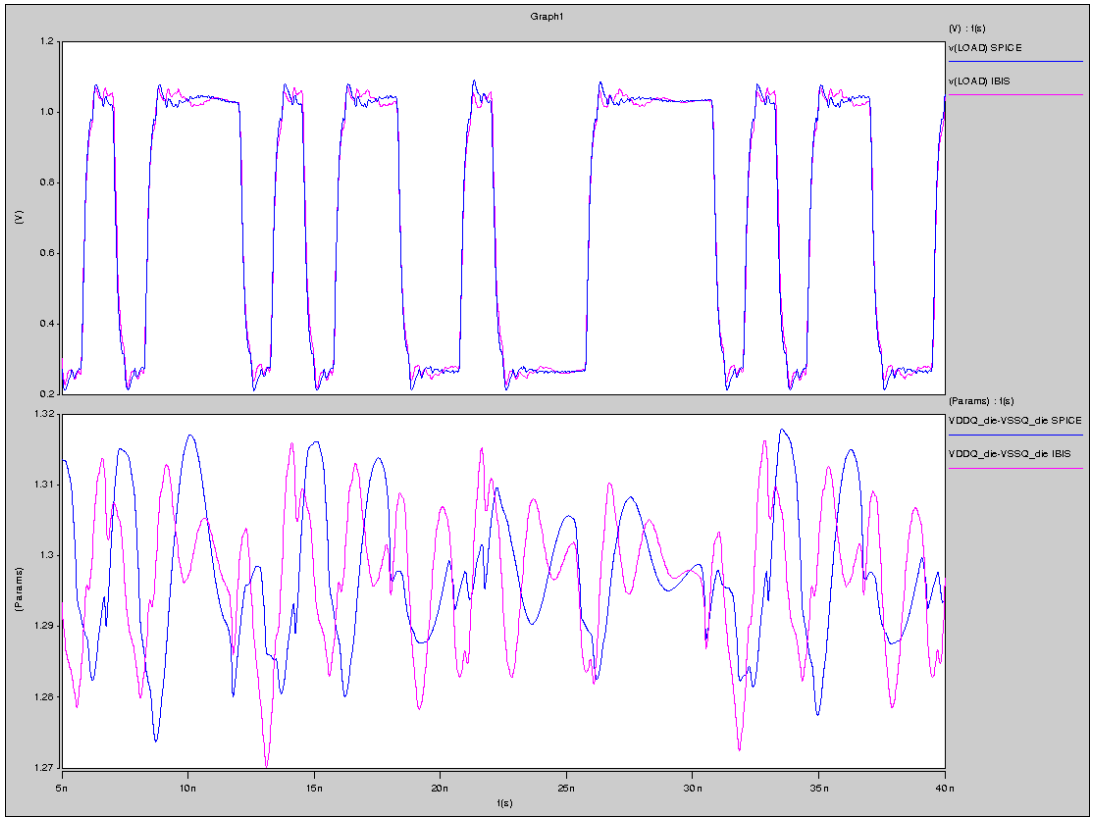
3-Port



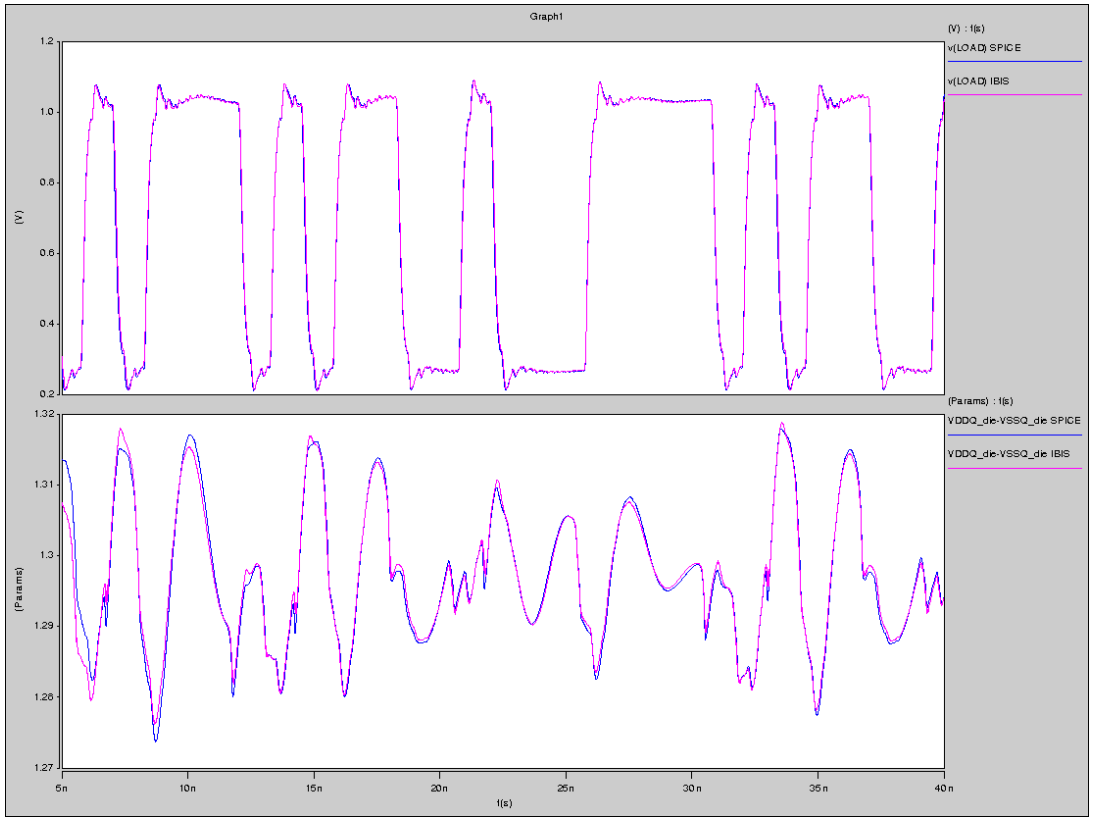
 © 2016 Micron Technology, Inc.

V(LOAD) and V(VDDQ_die)-V(VSSQ_die)

2-Port



3-Port



 © 2016 Micron Technology, Inc.

Conclusions

- A 2-port S-parameter (3-terminal macro-model) for on-die decoupling is a better model than a 1-port model for power-aware simulations.
  - This solution requires use of node 0 in the decoupling model.
- Correlating to a SPICE simulation that includes non-ideal supply connections to pre-driver circuits requires extra ports for non-ideal supplies in the decoupling model.
- A multi-port decoupling model is most versatile. Unused ports not connected to a package model should be connected to 0.
- The new IBIS Interconnect BIRD will allow the IBIS-ISS decoupling model to be connected properly to the package model.

 © 2016 Micron Technology, Inc.


Micron®