IBIS Chair's Report

http://www.ibis.org/

Mike LaBonte
Signal Integrity Software
Chair, IBIS Open Forum

Asian IBIS Summit
Taipei, Taiwan
November 14, 2016

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models

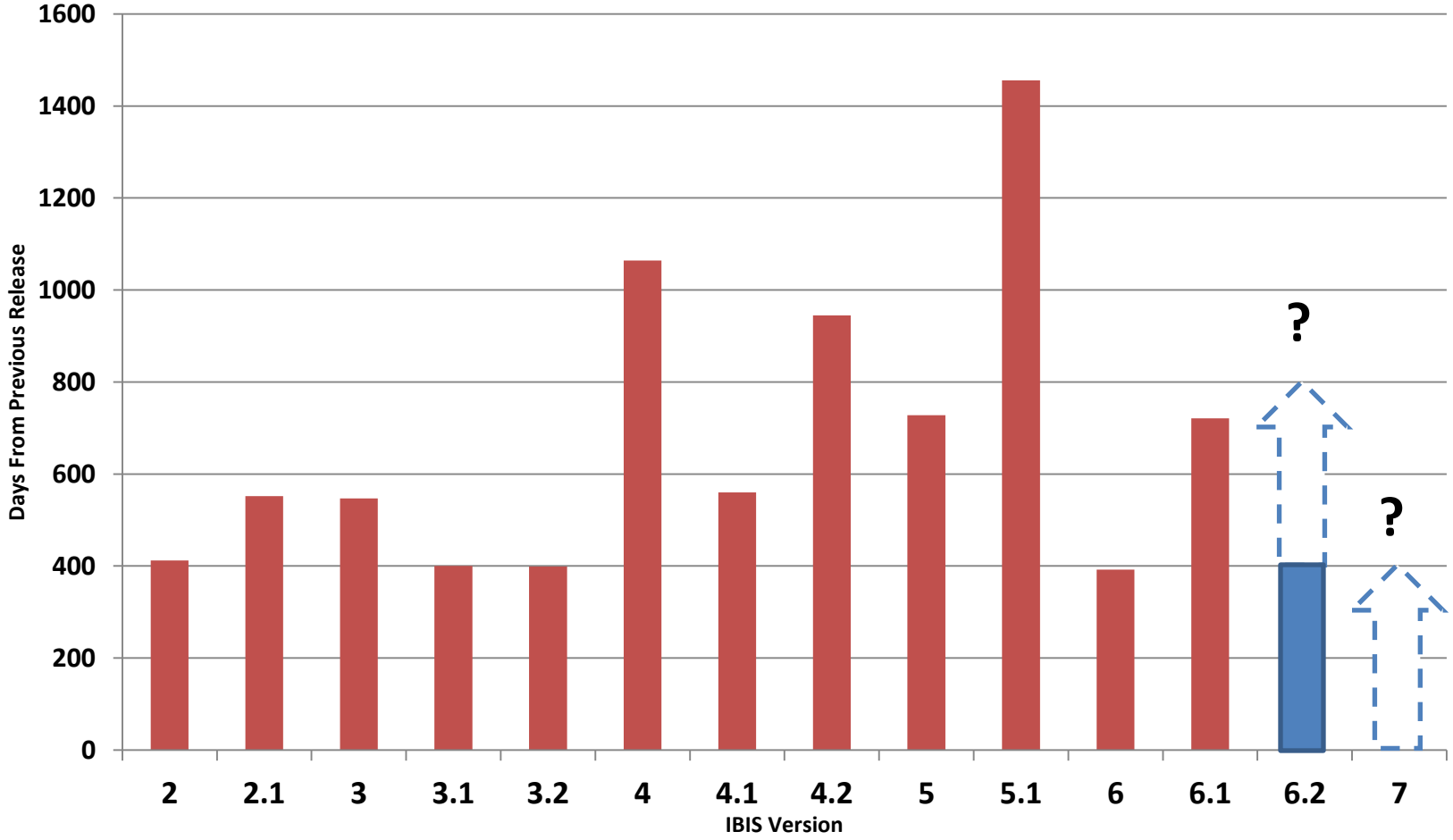
Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone® 2.0***
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

**Touchstone® is a registered trademark of Agilent Technologies, Inc.*

IBIS Version Development

As of 23-Oct-2016



Work In Progress

- Advanced Technology Modeling Task Group
  - IBIS 6.2 dedicated to reference node clarifications
  - Back-channel support (BIRD147.3)
  - C_comp model enhancements
  - Redriver flow enhancements
- Interconnect Task Group
  - External Package/on-die models using IBIS-ISS and Touchstone®
- IBIS Quality Task Group
  - IBISCHK enhancements and documentation

In Progress: IBIS 6.2

- Purpose: Clarify reference terminal conventions in IBIS
- BIRDs submitted, discussed in ATM Task Group
- Editorial Task Group will resume after BIRDs passed

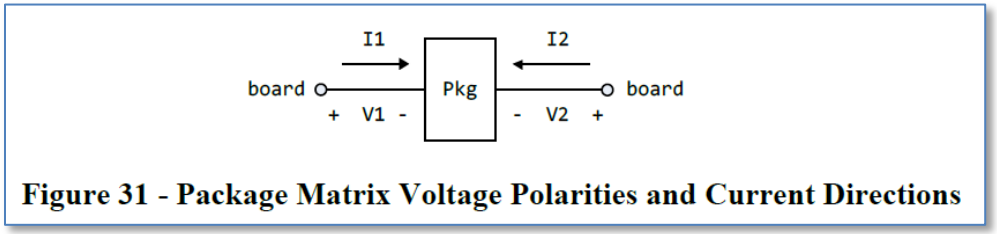


Figure 31 - Package Matrix Voltage Polarities and Current Directions

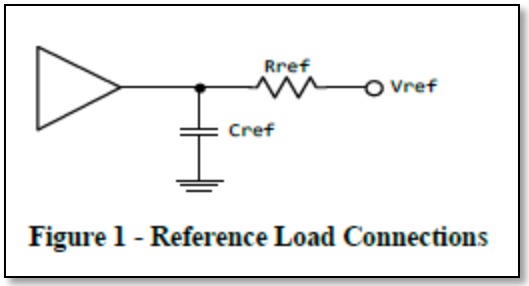


Figure 1 - Reference Load Connections

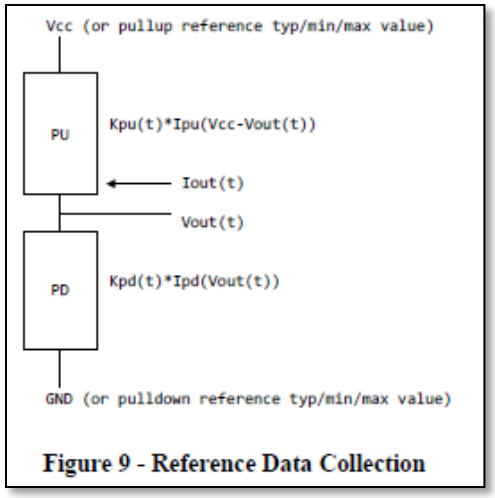
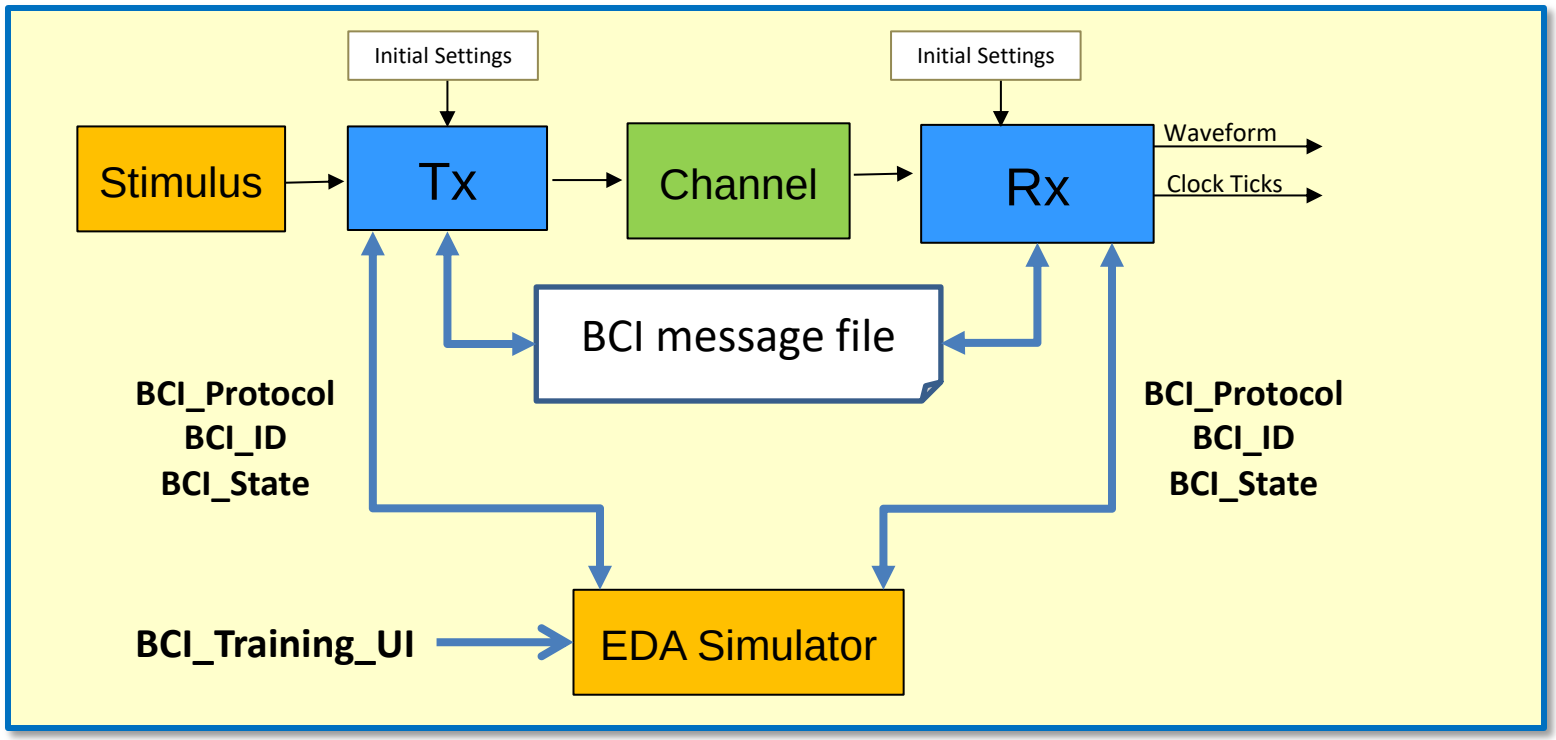


Figure 9 - Reference Data Collection

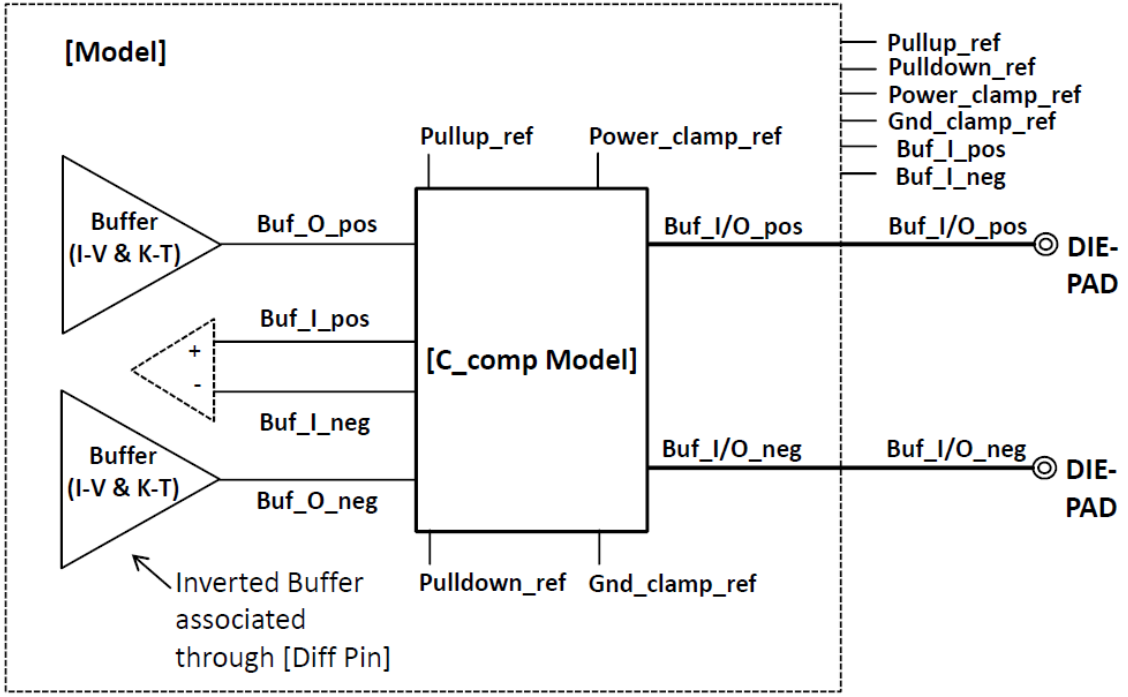
In Progress: Backchannel support

- Purpose: Backchannel to model time domain link training
- BIRD 147.3 recommended by ATM Task Group for acceptance



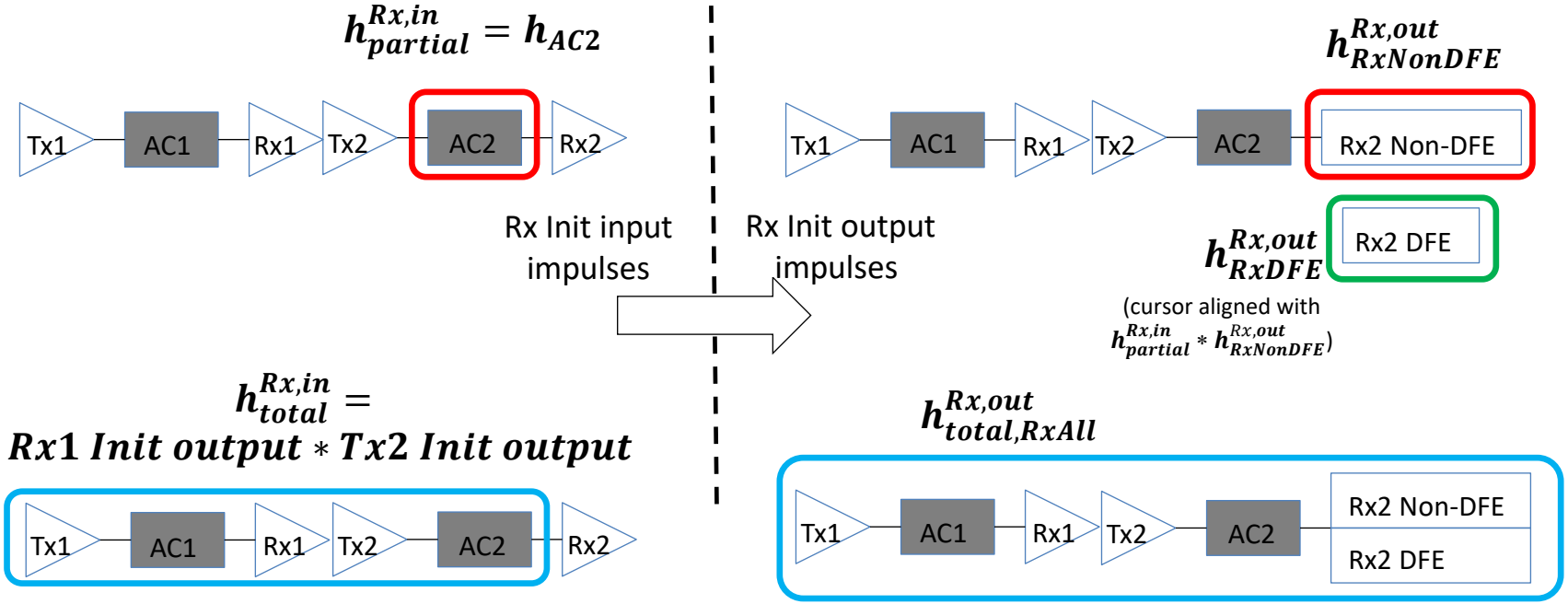
In Progress: C_comp Model Enhancements

- Purpose: Accurate C_comp model supporting frequency and voltage dependence, using IBIS-ISS and Touchstone®
- In ATM Task group, BIRD not yet submitted



In Progress: Redriver Flow Enhancements

- Purpose: Provide full redriver channel impulse to Rx Init for optimization, eliminate the need for deconvolution
- In ATM Task group, BIRD not yet submitted



In Progress: Interconnect BIRD

- Purpose: External Package/on-die models using IBIS-ISS
- In Interconnect Task Group, BIRD (draft 42) not yet submitted

```
[Interconnect Model Set]       Full_ISS_PDN_sn_2
[Interconnect Model]           Full_ISS_buf_pin_2
File_IBIS-ISS   full_buf_pin.iss                full_buf_pin_2_typ
Number_of_terminals = 14
1  Pin_I/O      pin_name      A1    |  DQ1          DQ
2  Pin_I/O      pin_name      A2    |  DQ2          DQ
3  Pin_I/O      pin_name      A3    |  DQ3          DQ
4  Pin_I/O      pin_name      D1    |  DQS+         DQS
5  Pin_I/O      pin_name      D2    |  DQS-         DQS
6  Pin_Rail     signal_name   VDD   |  VDD          POWER
7  Pin_Rail     signal_name   VSS   |  VSS          GND
8  Buf_I/O      pin_name      A1    |  DQ1          DQ
9  Buf_I/O      pin_name      A2    |  DQ2          DQ
10 Buf_I/O      pin_name      A3    |  DQ3          DQ
11 Buf_I/O      pin_name      D1    |  DQS+         DQS
12 Buf_I/O      pin_name      D2    |  DQS-         DQS
13 Buf_Rail     signal_name   VDD   |  VDD          POWER
14 Buf_Rail     signal_name   VSS   |  VSS          GND
|
[End Interconnect Model]
[End Interconnect Model Set]
```

In Progress: Approved BIRDs

- All are targeted for IBIS 6.2

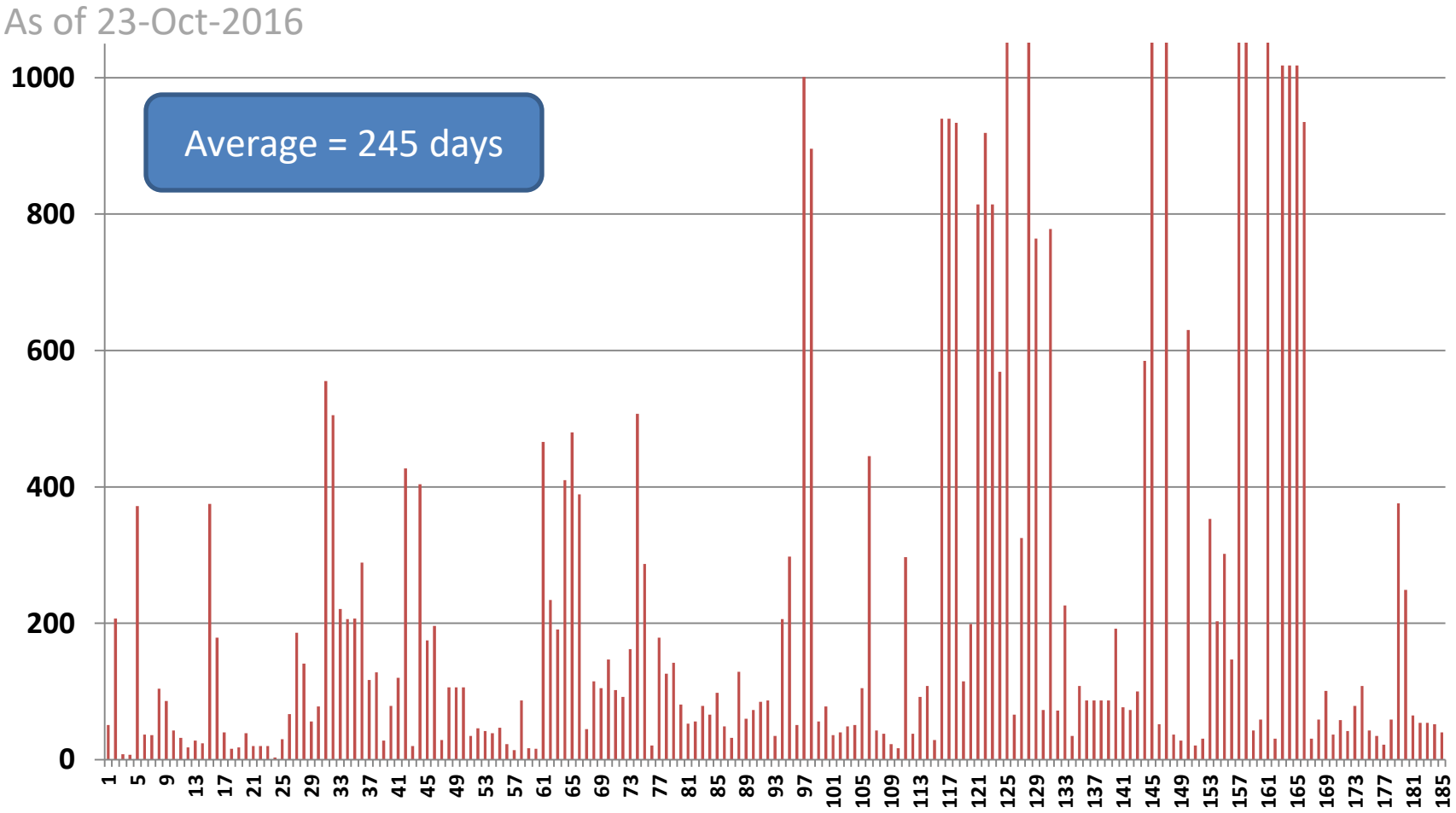
BIRD	Title
179	New IBIS-AMI Reserved Parameter Special_Param_Names
180	Require Unique Pin Names in [Pin]
182	POWER and GND [Pin] signal_name as [Pin Mapping] bus_label
183	[Model Data] Matrix Subparameter Terminology Correction

In Progress: Open BIRDs

- Some are targeted for IBIS 6.2
- Some are superseded by new BIRDs and will be rejected

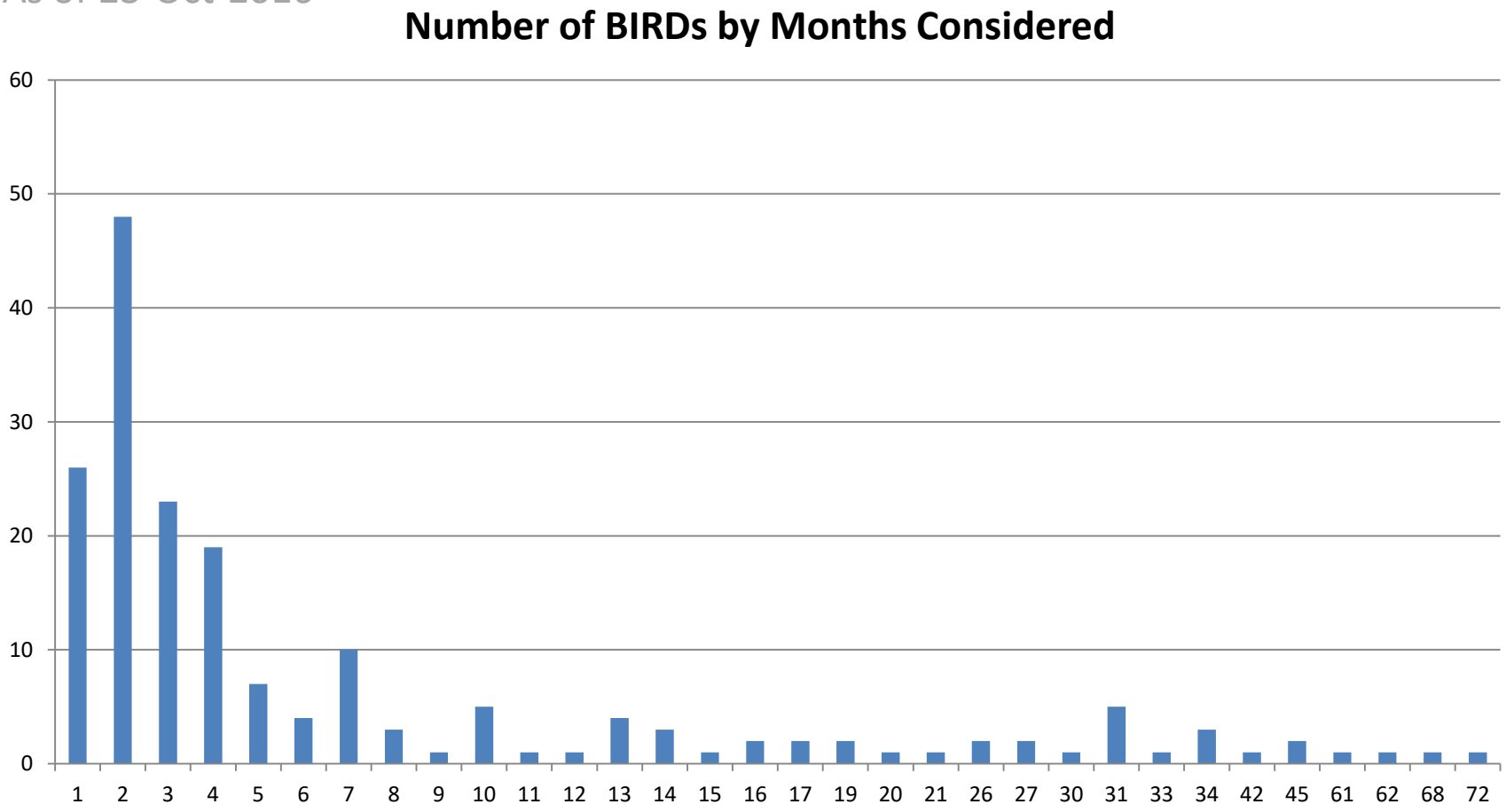
125.1	Make IBIS-ISS Available for IBIS Package Modeling
145.3	Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword
157	Parameterize [Driver Schedule]
158.3	AMI Touchstonefile (R) Analog Buffer Models
161.1	Supporting Incomplete and Buffer-only [Component] Descriptions
163	Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]
164	Allowing Package Models to be defined in [External Circuit]
165	Parameter Passing Improvements for [External Circuit]s
166	Resolving problems with Redriver Init Flow
181	I-V Table Clarifications
184.1	Model_name and Signal_name Restriction for POWER and GND Pins
185.1	Section 3 Reserved Word Guideline Update

Days To Resolve BIRDs

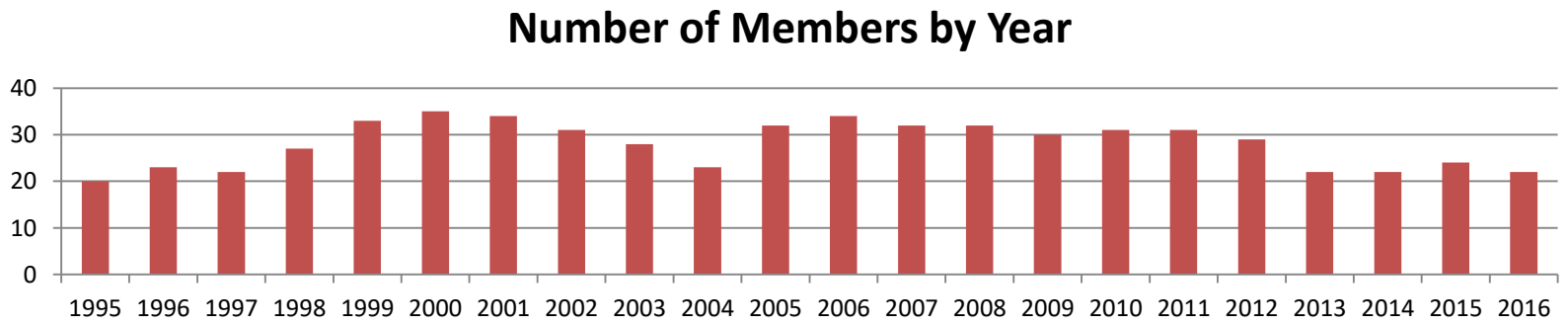


Most BIRDs Resolved < 9 Months

As of 23-Oct-2016



22 IBIS Members



IBIS Officers 2016-2017

Chair:	*Mike LaBonte, Signal Integrity Software*
Vice-Chair:	*Lance Wang, IO Methodology Inc.*
Secretary:	*Randy Wolff, Micron Technology*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Webmaster:	*Mike LaBonte, Signal Integrity Software*
Postmaster:	*Curtis Clark, ANSYS*

IBIS Meetings

- Teleconferences every week
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays, now suspended)
- IBIS Open Forum teleconference every 3 weeks
- IBIS Summit meetings: DesignCon, SPI, Shanghai, Taipei, Tokyo, EPEPS (2015)

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.