
ASIAN IBIS SUMMIT (TAIPEI) AGENDA

Time/Date: 8:15 - 16:30, Monday, November 14, 2016

Sponsors: **Cadence Design Systems**
IO Methodology
Peace Giant Corporation
Synopsys
Xpeedic Technology

8:15 **SIGN IN**
- Vendor Tables Open at 8:30

9:00 **WELCOME**
- Mike LaBonte (Chair, IBIS Open Forum)
(Signal Integrity Software (SiSoft), USA)

9:10 **IBIS Chair's Report**
Mike LaBonte (Signal Integrity Software (SiSoft), USA)

9:40 **Case Study: Modeling IBIS for Open_drain True Differential Pair Buffer**
Lance Wang* and Liang Yan**
(*IO Methodology* and **Maxim Integrated, USA)
[Presented by Lance Wang (IO Methodology, USA)]

10:10 **Differential Modeling Flow with Series Model in Verilog-A**
Wei-hsing Huang* and Sanjeev Gupta**
(*SPISim, USA and **Sigintegrity Solutions, India)
[Presented by Wei-hsing Huang (SPISim, USA)]

10:40 **BREAK** (Refreshments and Vendor Tables)

11:00 **IBIS-AMI Model Generation with Quality**
Skipper Liang (Cadence Design Systems, ROC)

12:00 **FREE BUFFET LUNCH** (Hosted by Sponsors)
- Vendor Tables

13:30 **Achieving Full System Signal Integrity for High Speed Backplane System**
Wenliang Dai (Xpeedic Technology, PRC)
[Presented by Zachary Su, (Xpeedic Technology, ROC)]

14:00 **On-Die Decoupling Model Improvements for IBIS Power Aware Models**
Randy Wolff#, Aniello Viscardi##
(Micron Technology; #USA, ##Italy)
[Presented by Lance Wang (IO Methodology, USA)]

14:30 **BREAK** (Refreshments and Vendor Tables)

14:50 **IBISCHK6 V6.1.3 and Executable Model File Checking**
Bob Ross (Teraspeed Labs, USA)
[Presented by Mike LaBonte
(Signal Integrity Software (SiSoft), USA)]

15:20 **Touchstone Conversion Wrapper**
Anders Ekholm (Ericsson, Sweden)

15:45 **DISCUSSION**

16:20 **CONCLUDING ITEMS**

16:30 **END OF IBIS SUMMIT MEETING**
