# Suggestion on Issuing VSR/CAUI-4 Based IBIS-AMI Model

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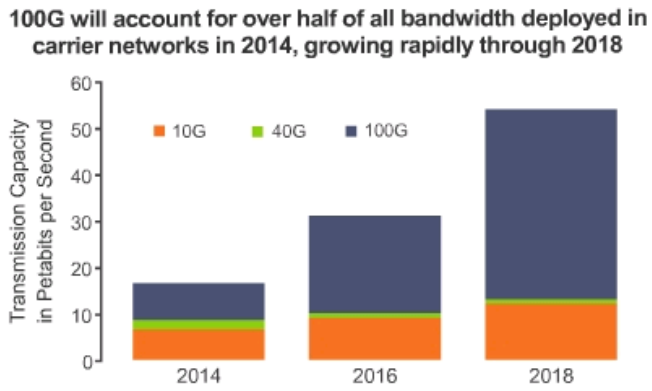
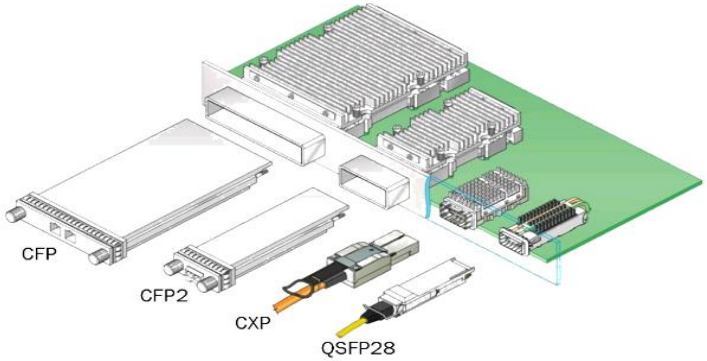
# Industry Trend: Optical Module with CDR Inside Becomes a Standard Beyond 25Gbps/lane




© Infonetics Research, *10G/40G/100G Optical Transceivers: Biannual Market Size, and Forecasts:* November 2014




| MODULE | CXP | QSFP28 | CFP | CFP2 | CFP4 | CPAK |
|---|---|---|---|---|---|---|
| Line Rates | 12x12G or 10x12G | 4x 25-28G | 40/100G (4*25G) | 40/100G (4*25G) | 40/100G (4*25G) | 40/100G (4*25G) |

FIBRE CHANNEL

Physical Interface-6

REV 3.10

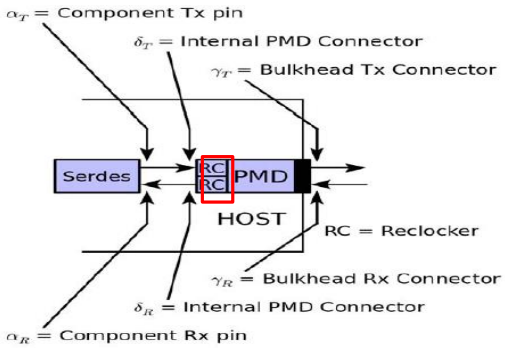



**Figure 1 – Reclocker location for all 32GFC PMDs**

OIF OPTICAL INTERNETWORKING FORUM

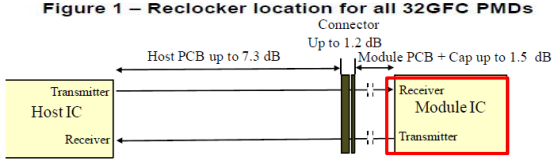
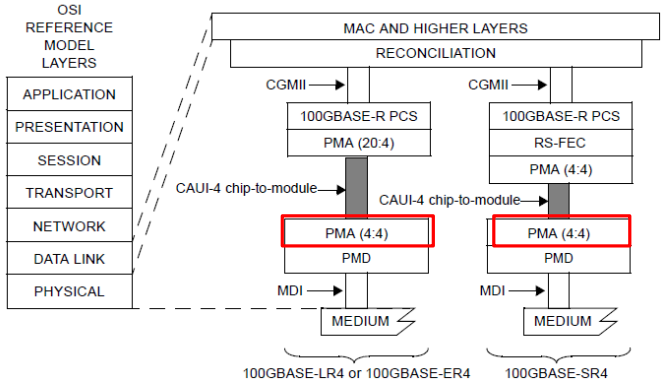



**Figure 13-21. CEI-28G-VSR full Channel Reference Model**

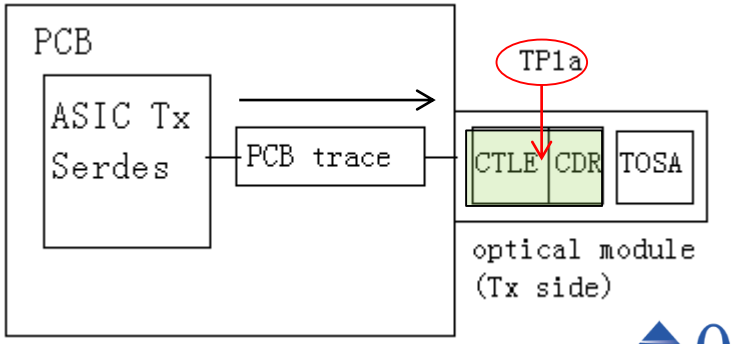
IEEE




Electrical interface between chip and module becomes a SerDes to SerDes connection.

# Electrical Interface Compliance Test Defined in OIF CEI-28G-VSR / IEEE 802.3bm CAUI-4

- TP1a is the test point after CTLE inside CDR device. The real eye diagram at TP1a can't be measured
- A standard "Reference CTLE" and "Golden PLL" model is defined for compliance test instead



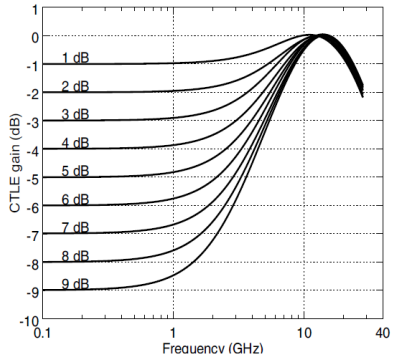




Figure 13-14. Host output Reference receiver equalizer (CTLE) transfer function for gains of 1 dB to 9 dB

Table 13-8. Reference equalizer coefficients for rate of 28 GBd.

| Peaking (dB) | G | P1/2π (GHz) | P2/2π (GHz) | Z1/2π (GHz) |
|---|---|---|---|---|
| 1 | 0.891 | 18.6 | 14.1 | 8.31 |
| 2 | 0.794 | 18.6 | 14.1 | 7.10 |
| 3 | 0.708 | 15.6 | 14.1 | 5.68 |
| 4 | 0.631 | 15.6 | 14.1 | 4.98 |
| 5 | 0.562 | 15.6 | 14.1 | 4.35 |
| 6 | 0.501 | 15.6 | 14.1 | 3.82 |
| 7 | 0.447 | 15.6 | 14.1 | 3.43 |
| 8 | 0.398 | 15.6 | 14.1 | 3.00 |
| 9 | 0.355 | 15.6 | 14.1 | 2.67 |

$$H(s) = \frac{(G)(P1)(P2)}{Z1}\frac{(S+Z1)}{(S+P1)(S+P2)}$$

Table 13-1. Host-to-Module Electrical Specifications at TP1a (host output)

| Parameter | Min. | Max. | Units | Conditions |
|---|---|---|---|---|
| Differential Voltage pk-pk | - | 900 | mV | |
| Common Mode Noise RMS | - | 17.5 | mV | See Section 13.3.5 |
| Differential Termination Resistance Mismatch | - | 10 | % | At 1 MHz See Section 13.3.6 |
| Differential Return Loss (SDD22) | - | See Equation 13-19 | dB | |
| Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22) | - | See Equation 13-21 | dB | |
| Common Mode Return Loss (SCC22) | - | -2 | dB | From 250 MHz to 30 GHz |
| Transition Time, 20 to 80% | 10 | - | ps | See Section 13.3.10 |
| Common Mode Voltage | -0.3 | 2.8 | V | Referred to host ground |
| Eye Width at $10^{-15}$ probability (EW15)[1] | 0.46 | - | UI | See Section 13.3.11 |
| Eye Height at $10^{-15}$ probability (EH15)[1] | 95 | - | mV | See Section 13.3.11 |

1. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE)

Note: a reference clock recovery unit (CRU) with a first order transfer function with a 3 dB tracking bandwidth of fb/2578.

# Oscilloscope Measurement Solution for TP1a

- Post-process the measurement waveform with software reference CTLE and golden PLL based on formula
- Use the noise and jitter extrapolation to get the EH / EW @ BER=1e-15

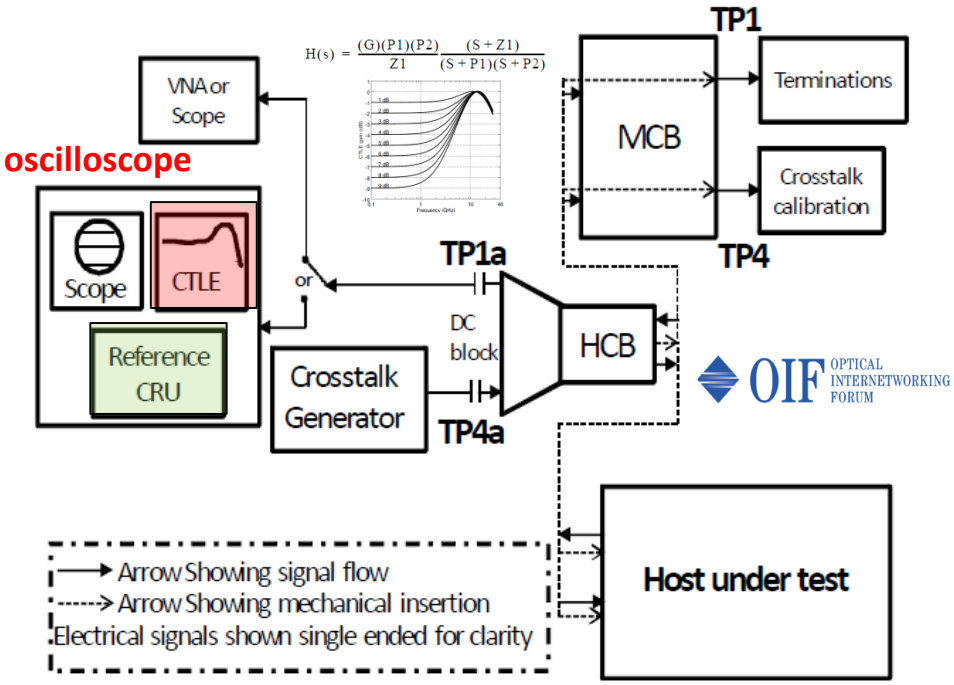
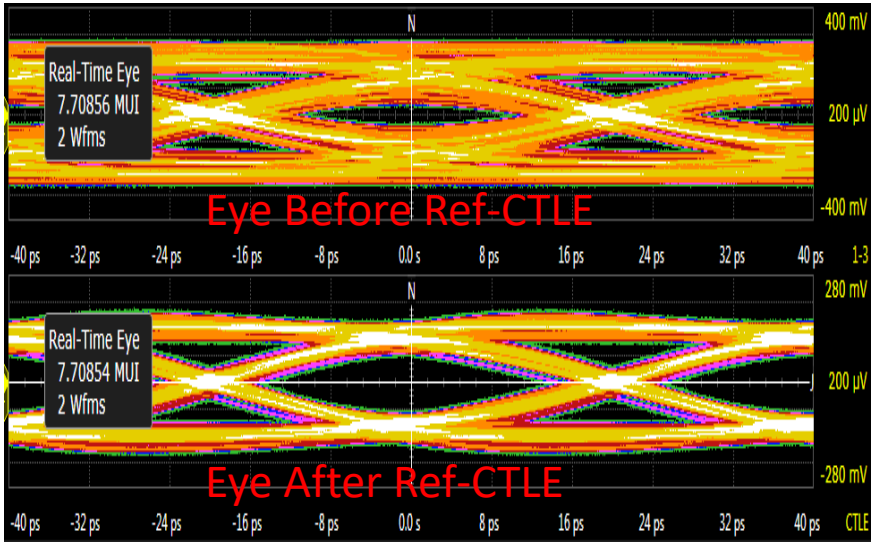
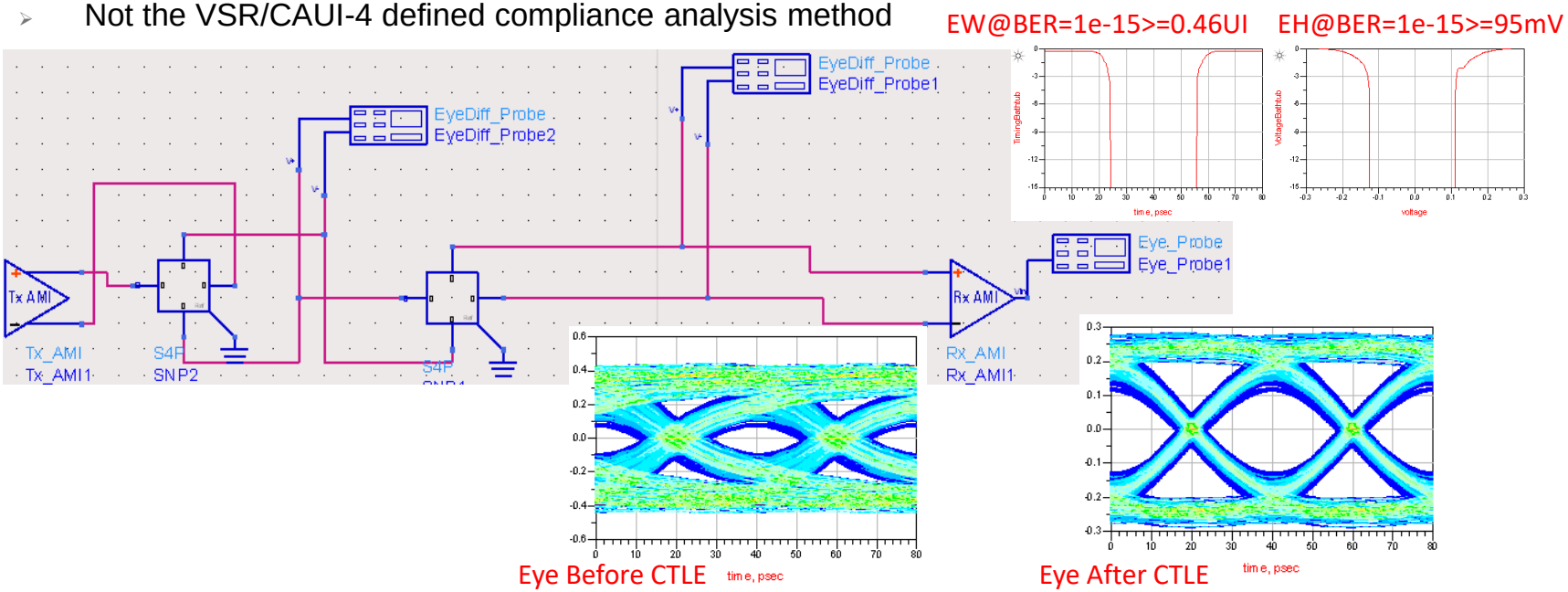



Figure 13-8. Host output test setup



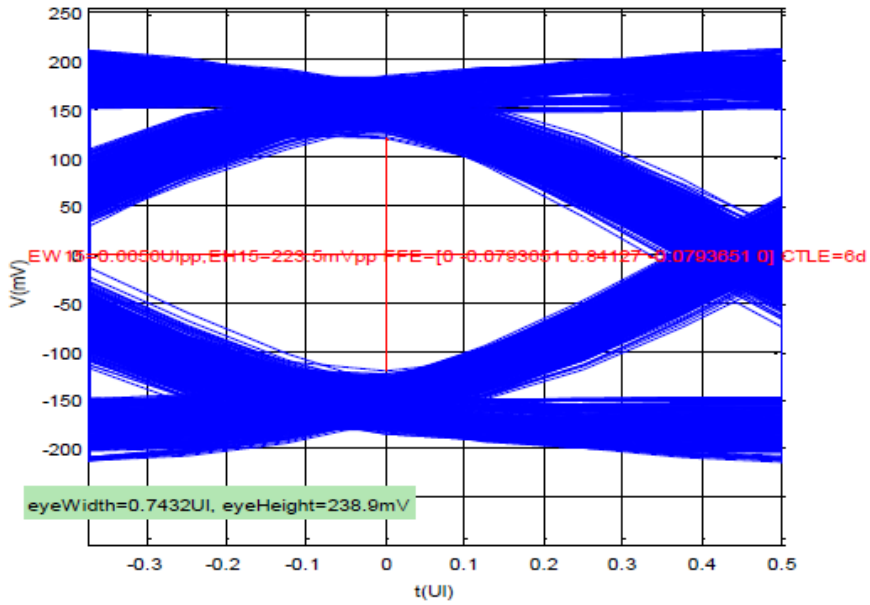
# Simulation Solution for TP1a (1): Acquire Certain Module's CDR IBIS-AMI Model

- Advantage:
  - Display real performance of certain optical module's CDR
  - Supported by commercial EDA tools
- Disadvantage:
  - Not all vendors can provide their CDR's IBIS-AMI model
  - Not the VSR/CAUI-4 defined compliance analysis method



# Simulation Solution for TP1a (2): Waveform Post-processing Based on VSR/CAUI-4 Spec

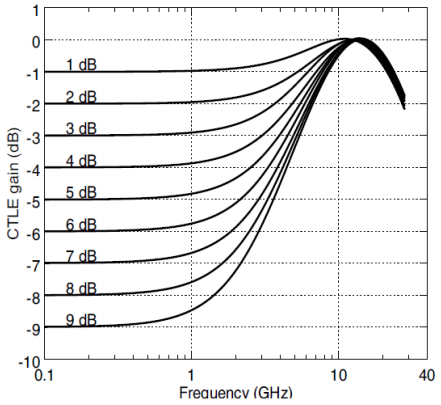
- Similar to measurement, current simulation has to be done with self-programmed data post-processing script
- Without reference CTLE IBIS-AMI model, VSR/CAUI-4 electrical interface simulation can’t be achieved in EDA tools



# Suggest IBIS Organization Issue the IBIS-AMI Model of Standard Reference CTLE for Customers

- Suggest IBIS Organization issue the standard VSR/CAUI-4 compliant IBIS-AMI model including reference CTLE and golden PLL
  - As reference CTLE is a definite formula and fully meets LTI system, it's not difficult to generate such a standard model

OIF OPTICAL INTERNETWORKING FORUM

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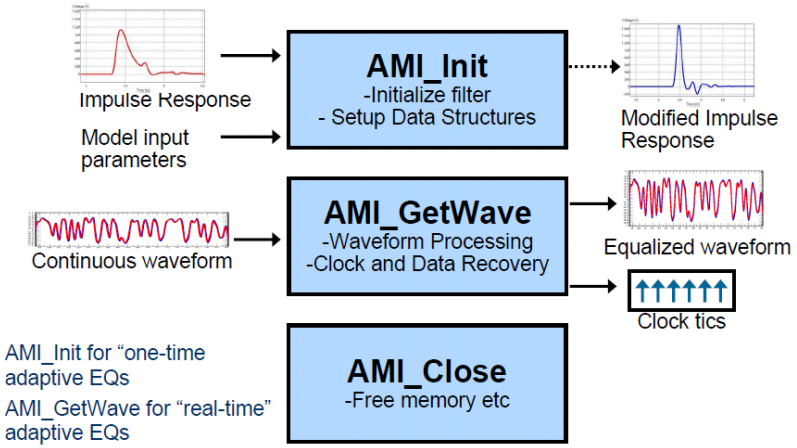

# Further Discussion

- The issue of the VSR/CAUI-4 based IBIS-AMI model may provide a way for optical CDR vendor to do the correlation between their setting and MSA EQ setting
  - Although MSA defined the unified I2C EQ setting, different optical module vendor uses different CDR and different CTLE, which may have different mapping relationship between MSA EQ and CDR's CTLE.
  - Without a unified correlation method, how to keep the reliability that passing the reference CTLE test of TP1a can pass the error test

SFF Committee

**SFF-8636**

Specification for

Management Interface for Cabled Environments

TABLE 6-34 INPUT EQUALIZATION (PAGE 03H BYTES 234-235)

| Value | Transmitter Input Equalization | |
|---|---|---|
| | Nominal | Units |
| 11xxb | Reserved | |
| 1011b | Reserved | |
| 1010b | 10 | dB |
| 1001b | 9 | dB |
| 1000b | 8 | dB |
| 0111b | 7 | dB |
| 0110b | 6 | dB |
| 0101b | 5 | dB |
| 0100b | 4 | dB |
| 0011b | 3 | dB |
| 0010b | 2 | dB |
| 0001b | 1 | dB |
| 0000b | 0 | No EQ |

- CTLE non-linearity feature should be considered in future
  - Currently formula-based model without considering the non-linearity

# Thank you

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