IBIS-AMI Model Generation -With Quality

Skipper Liang

Asian IBIS Summit, Shanghai, China

November 11, 2016

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Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
  3. A System – TX + Channel + RX
- Conclusion

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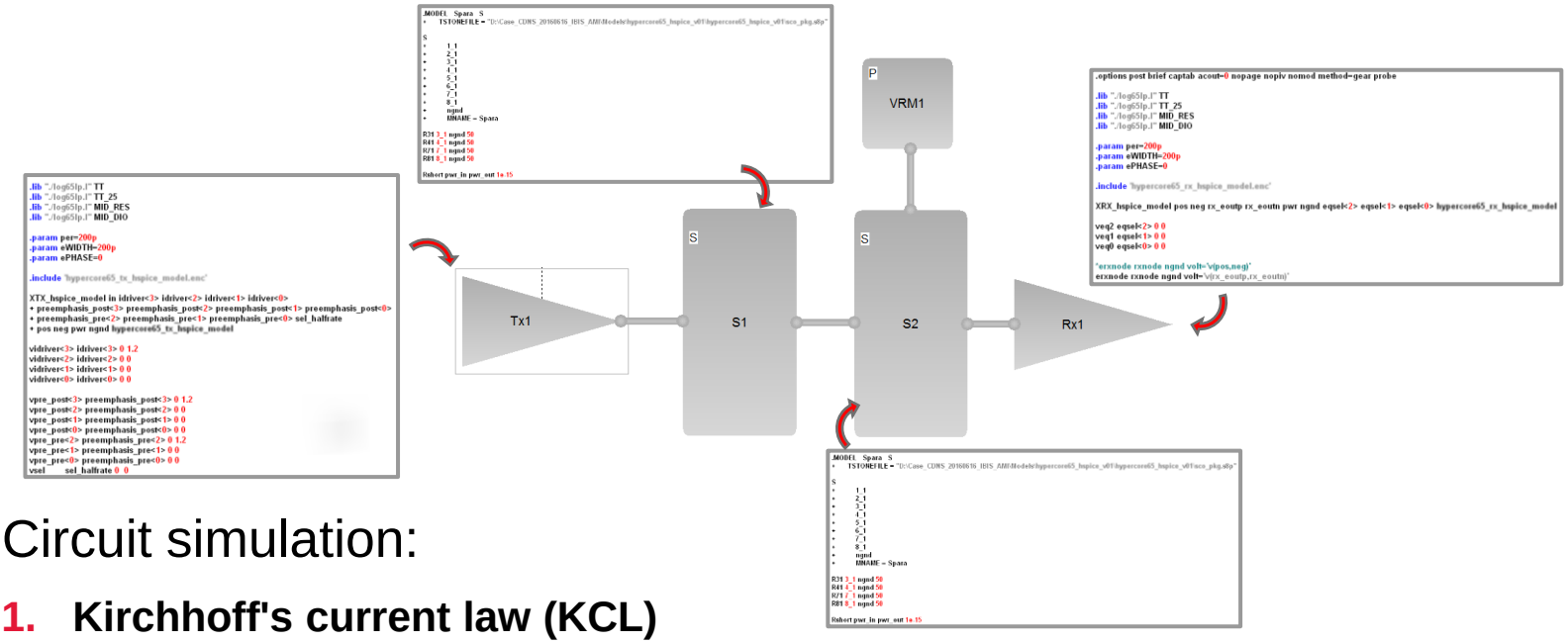
Circuit Simulation–

Using transistor **SPICE netlist** model



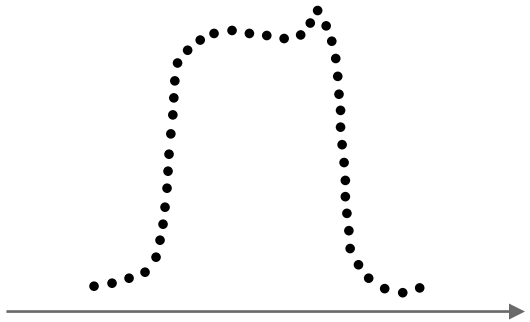
- Circuit simulation:

1. **Kirchhoff's current law (KCL)**

   At any node (junction) in an electrical circuit, the sum of current flowing into that node is equal to the sum of currents flowing out of that node

2. **Kirchhoff's voltage law (KVL)**

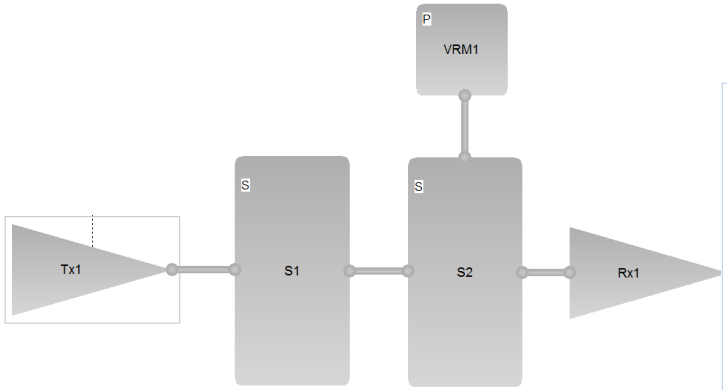
   The directed sum of the electrical potential differences (voltage) around any closed network is zero



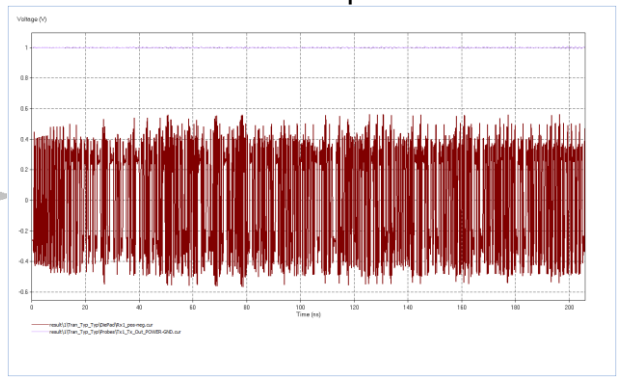
Traditional signoff flow –
Using transistor **SPICE netlist** model (con't)

Advantages:

- Accurate PI prediction under **limited** bits transmission
- Accurate jitter prediction under **limited** bits transmission

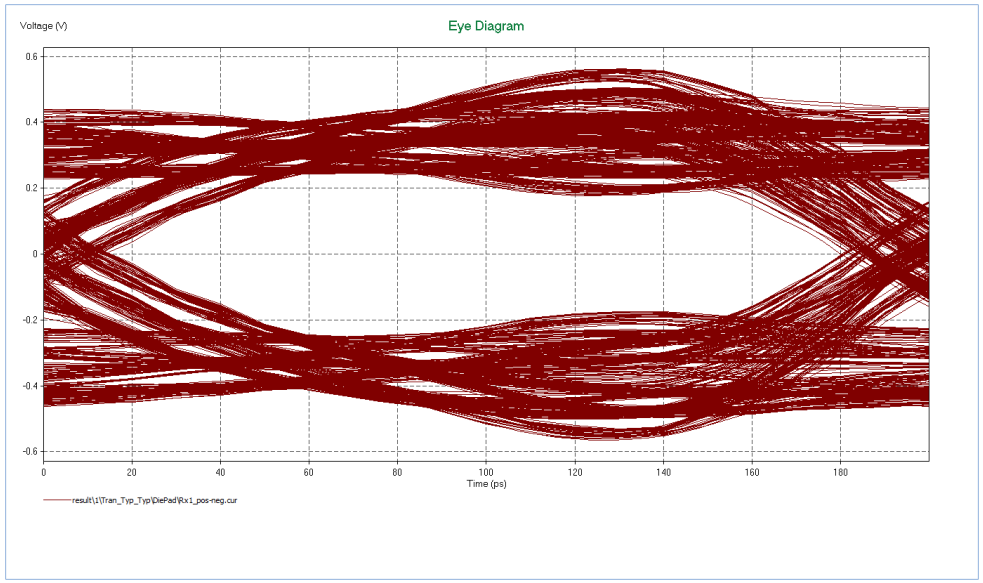


8hr34min for **1024** bit pattern simulation



Disadvantages:

- Very slow for SPICE netlist model - Takes weeks/months to get bit error-rate (BER) prediction
- Can't model the adaptive mechanism in RX



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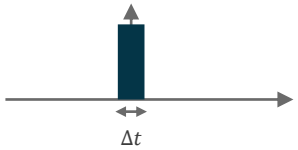
LTI – Linear time invariant (con't.)

- Signal expressed in an impulse-train format:
  - Impulse:

$$\delta(t) = \begin{cases} 0, other\ than\ t = 0 \\ \infty, t = 0 \end{cases}$$

so, $\int_{-\infty}^{\infty} \delta(t)dt = 1$

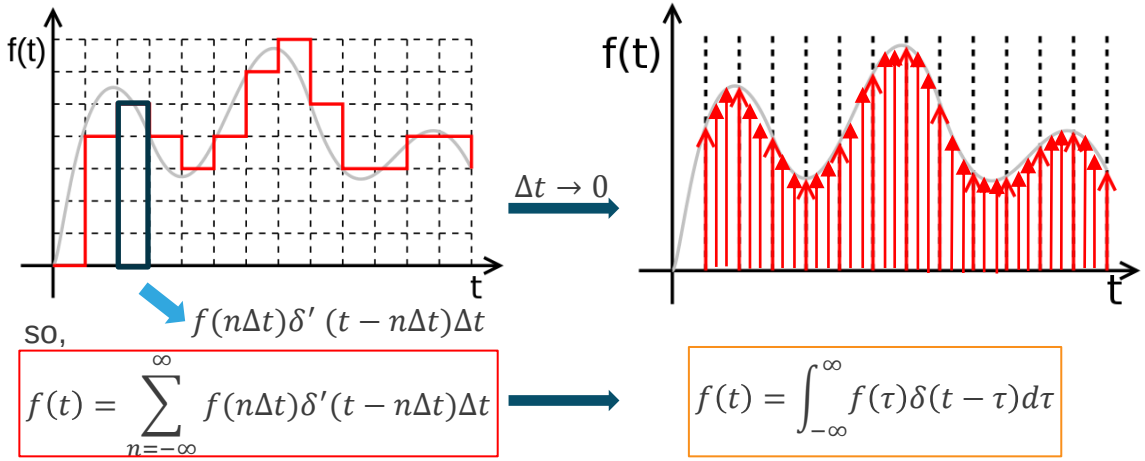
  - Quasi-Impulse:



$$\delta'(t) = \begin{cases} 0, |t| > \frac{\Delta t}{2} \\ \frac{1}{\Delta t}, |t| \le \frac{\Delta t}{2} \end{cases}$$

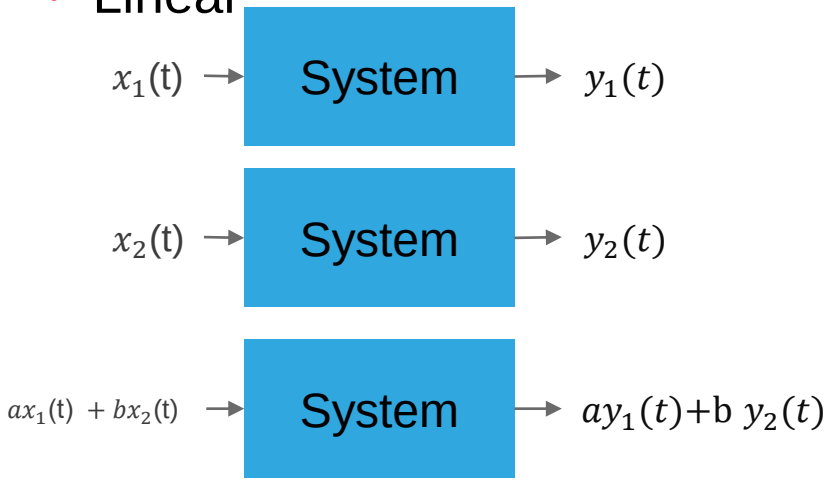
so, $\int_{-\infty}^{\infty} \delta'(t)dt = 1$

  - Any Signal:

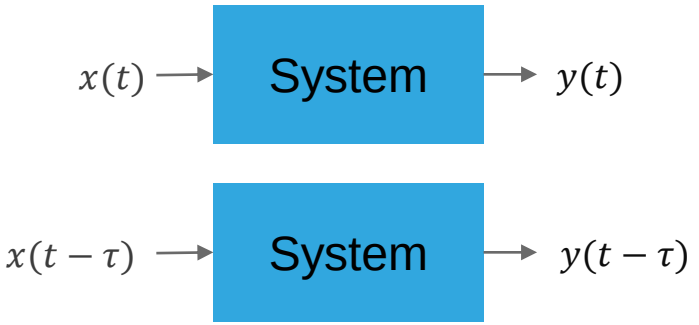


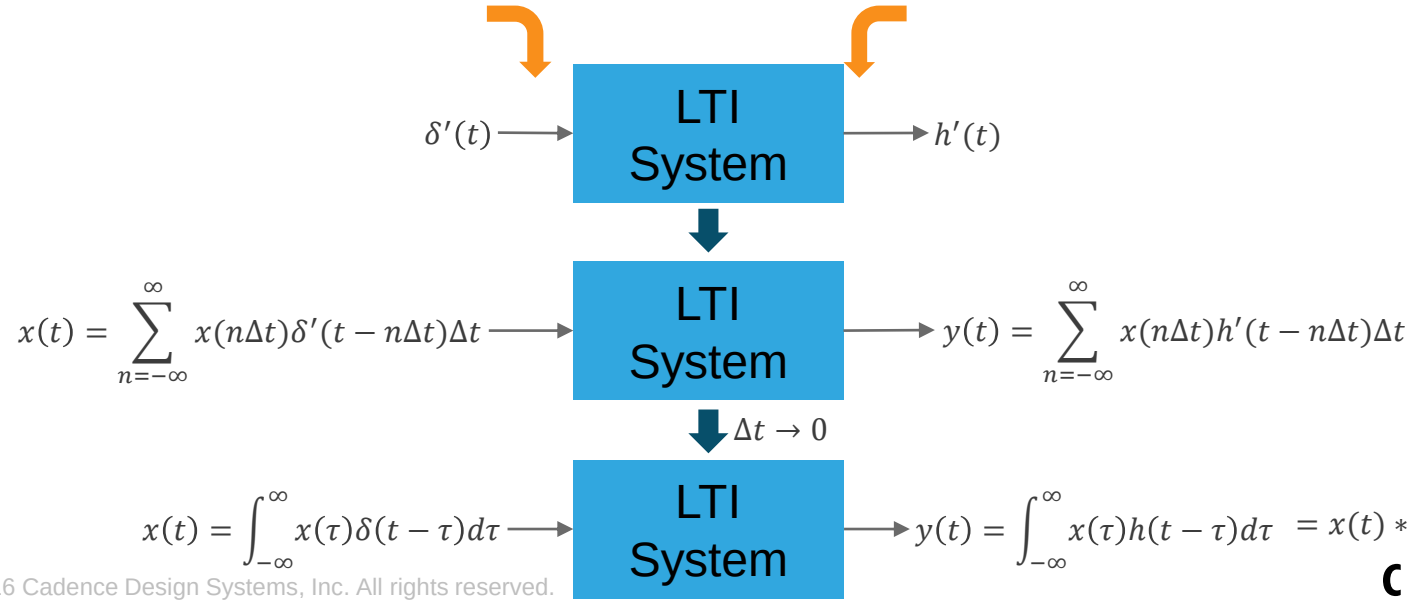
LTI – Linear time invariant (Con't.)

- Linear



- Time Invariant





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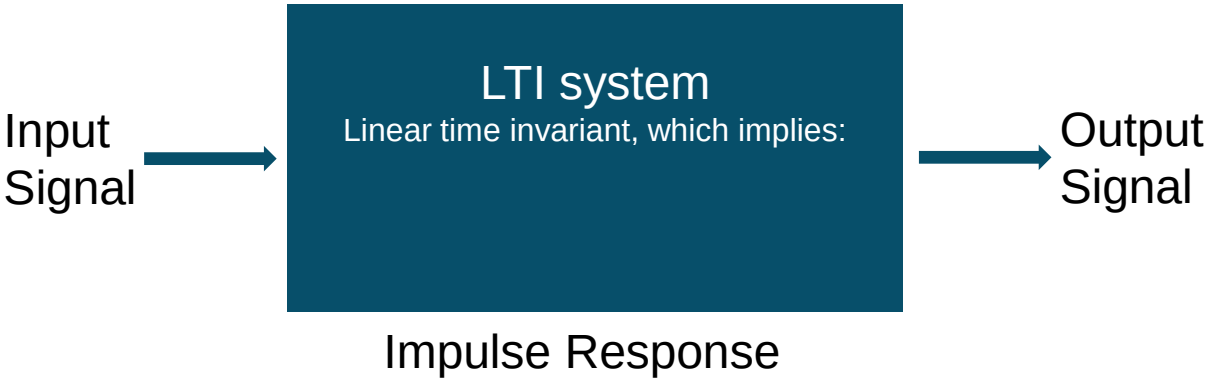
Channel-Simulation

- Channel simulation :



x(t) * h(t) = y(t)

(convolute)

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau$$

X(f) × H(f) = Y(f)

Multi-times faster than circuit simulation!!

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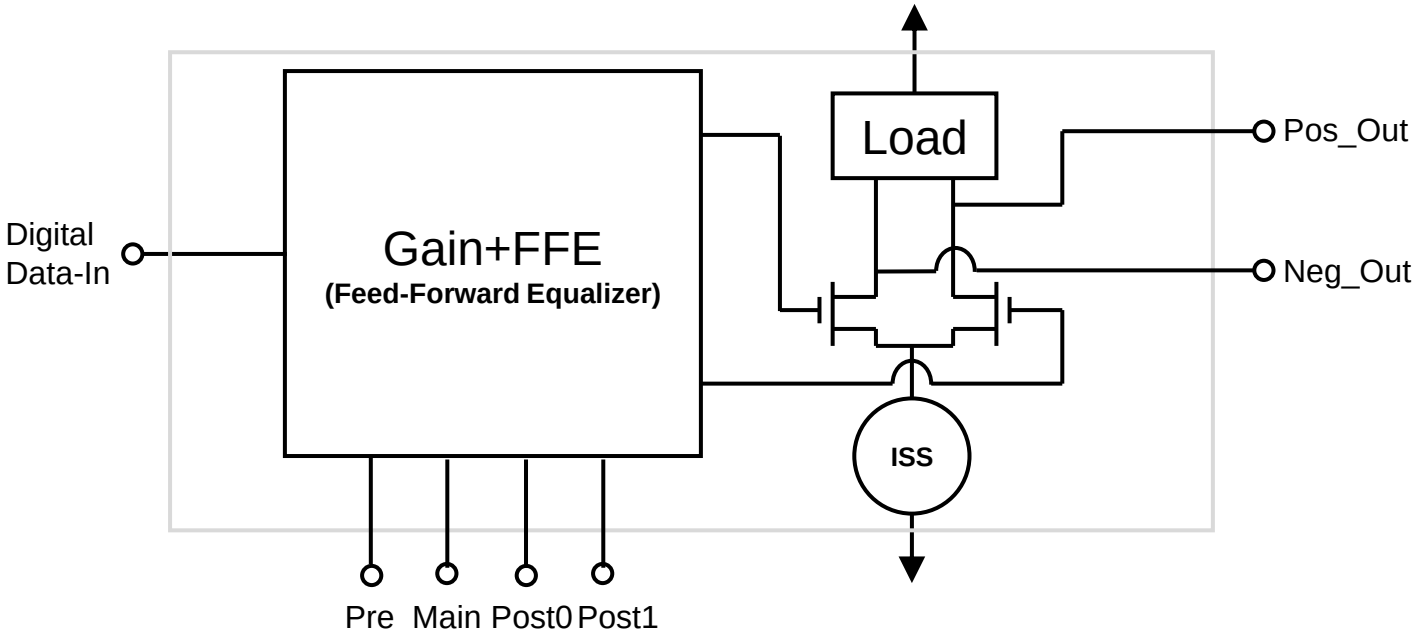
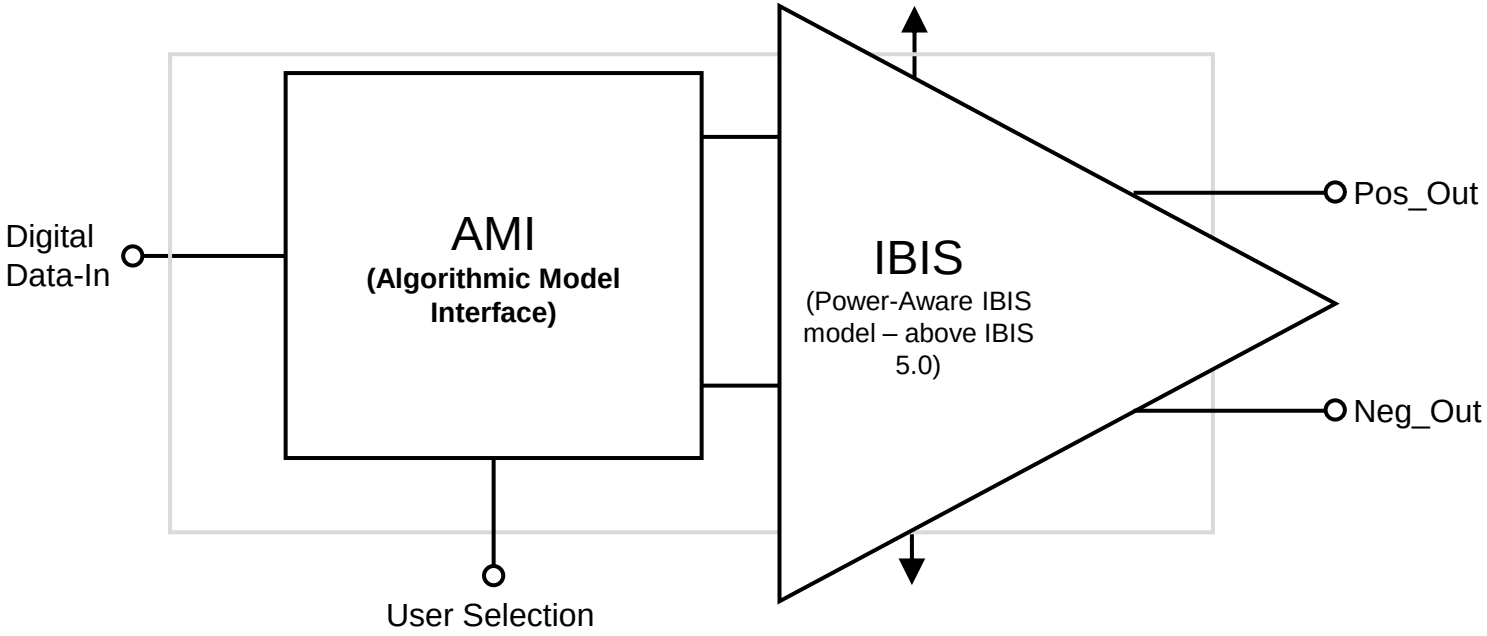
What is IBIS+AMI model (Example: TX)



Accompanied with channel simulator:

- PI prediction with good accuracy without limits on transmission bits
- Jitter prediction with good accuracy without limits on transmission bits
- Very fast for IBIS+AMI netlist model - Takes minutes to get BER prediction
- Can model the adaptive mechanism in RX

What is IBIS+AMI model (Example: TX)



Accompanied with channel simulator:

- PI prediction with good accuracy without limits on transmission bits
- Jitter prediction with good accuracy without limits on transmission bits
- Very fast for IBIS+AMI netlist model - Takes minutes to get BER prediction
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But you might be concerned:

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- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – **Validation** is the **KEY**!!
- Successful Stories:
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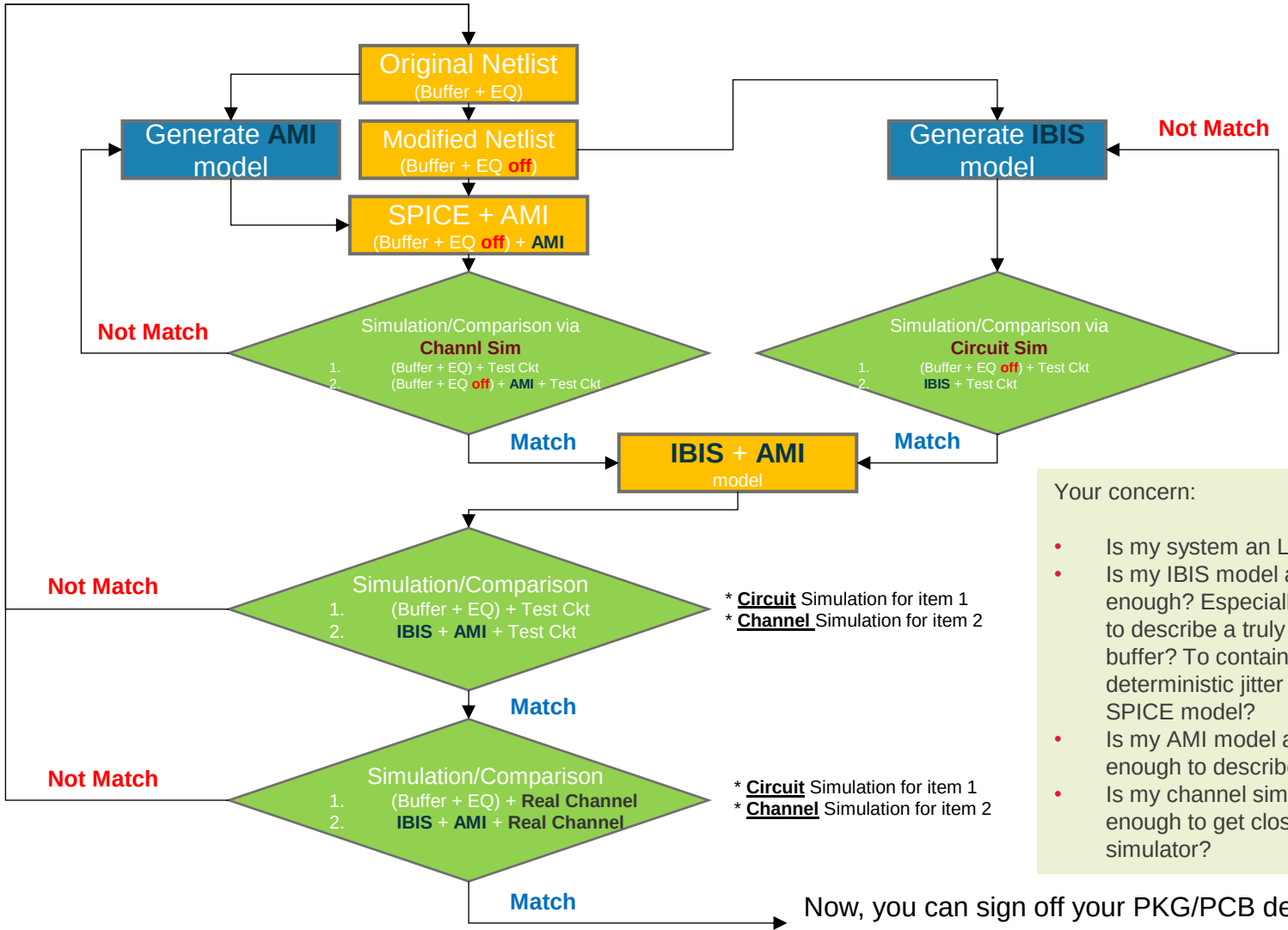
IBIS+AMI model generation flow



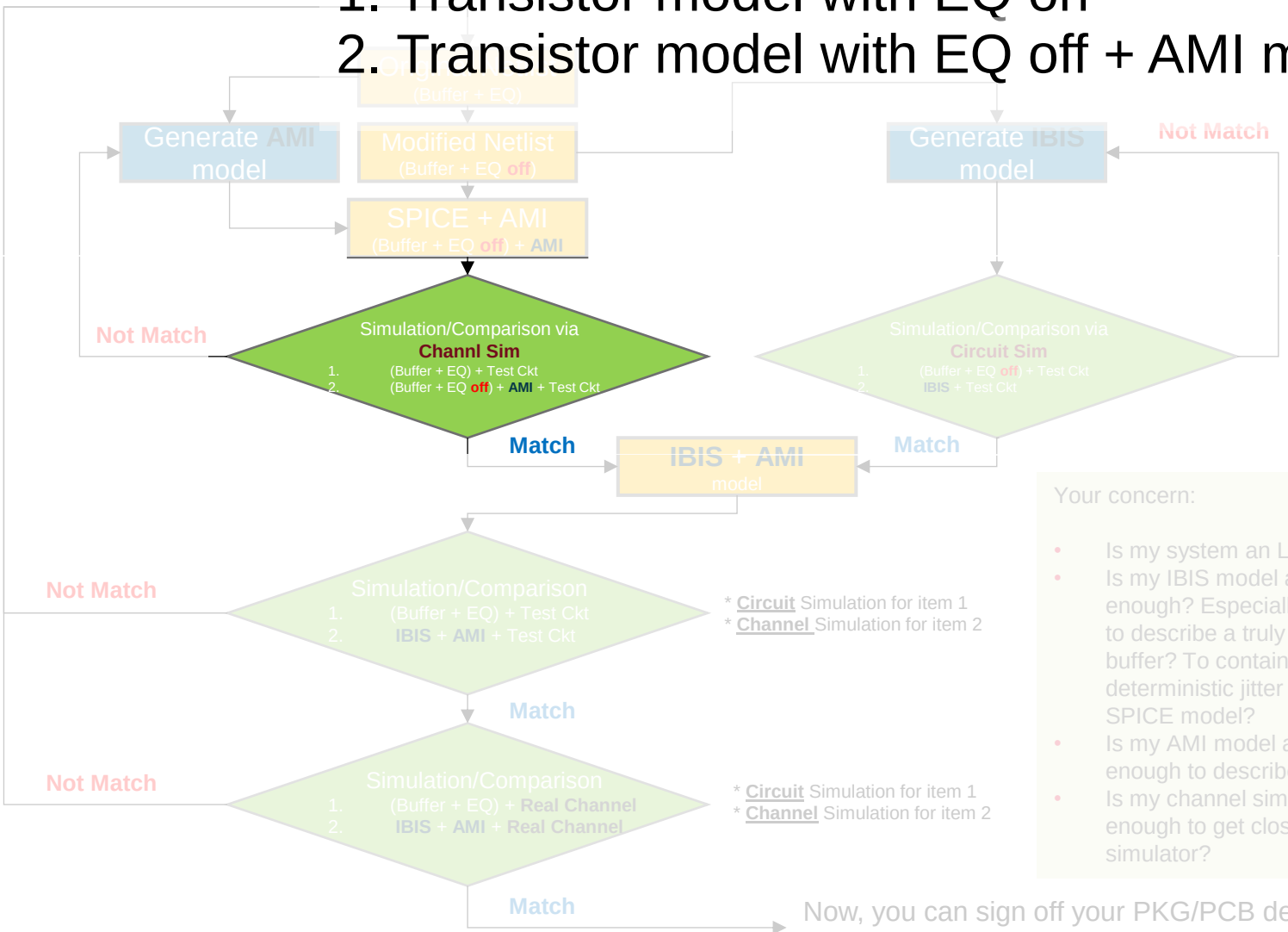
Your concern:

- Is my system an LTI channel?
- Is my IBIS model accurate enough? Especially being used to describe a truly differential buffer? To contain the deterministic jitter existed in my SPICE model? V
- Is my AMI model accurate enough to describe my EQ? V
- Is my channel simulator accurate enough to get close to circuit simulator? V

Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated

Validation 1: Channel Simulation for

1. Transistor model with EQ on
2. Transistor model with EQ off + AMI model



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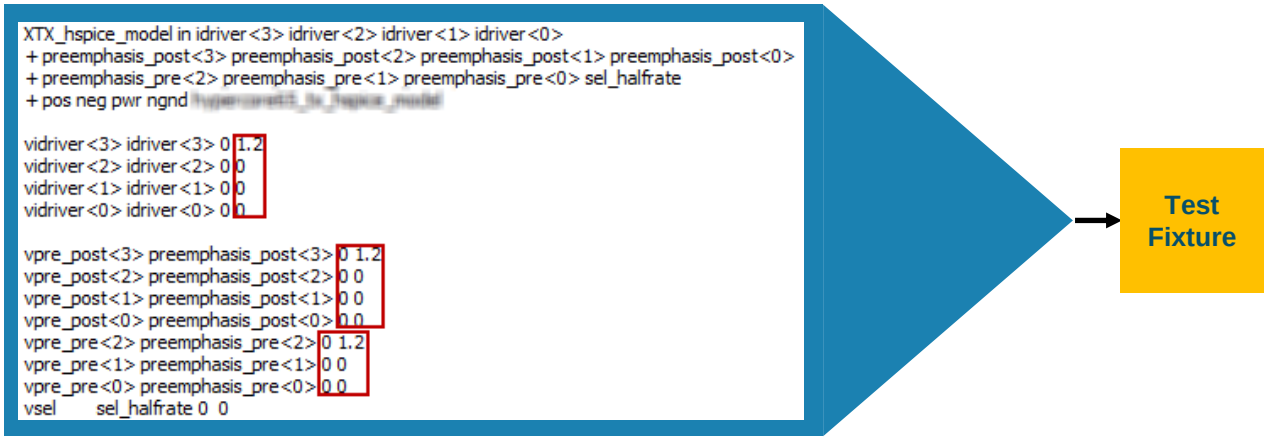
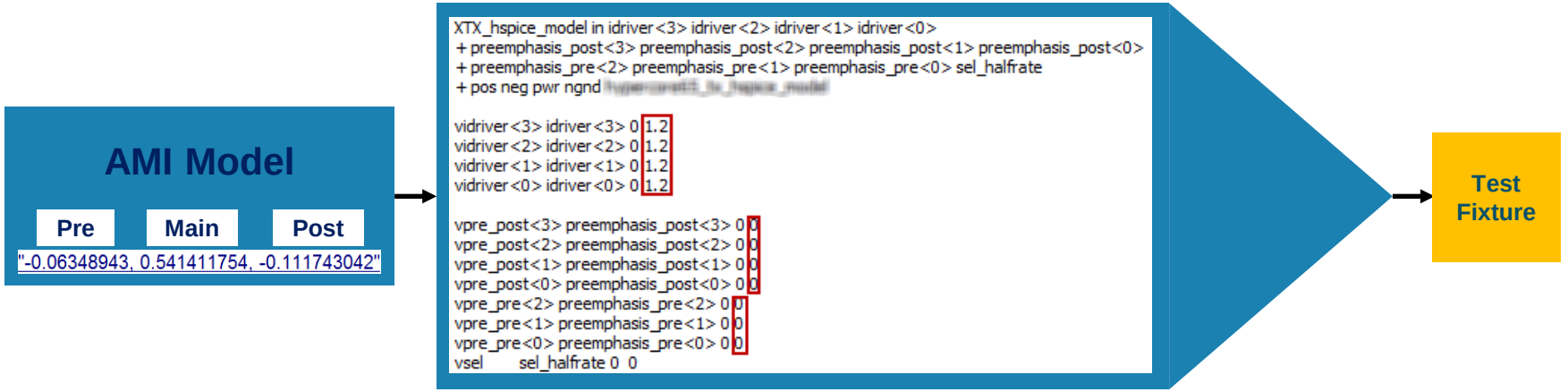
Validation 1: Channel Simulation for

1. Transistor model with EQ on

To qualify the AMI model so generated.



2. Transistor model with EQ off + AMI model



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Validation 1: **Channel Simulation** for

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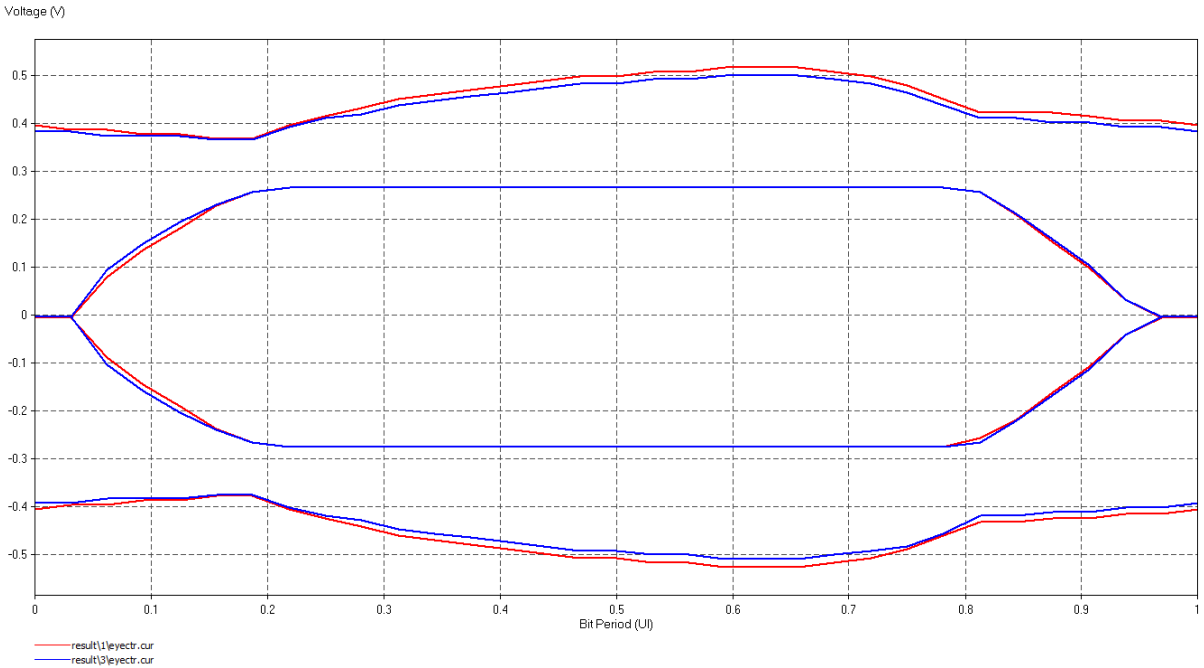
To qualify the AMI model so generated.



Why **Channel Simulation**?:

1. AMI model can only be used in **Channel Simulation**
2. Put transistor models under **Channel Simulation** will narrow down the possible cause for any difference happened here to the AMI model so generated.

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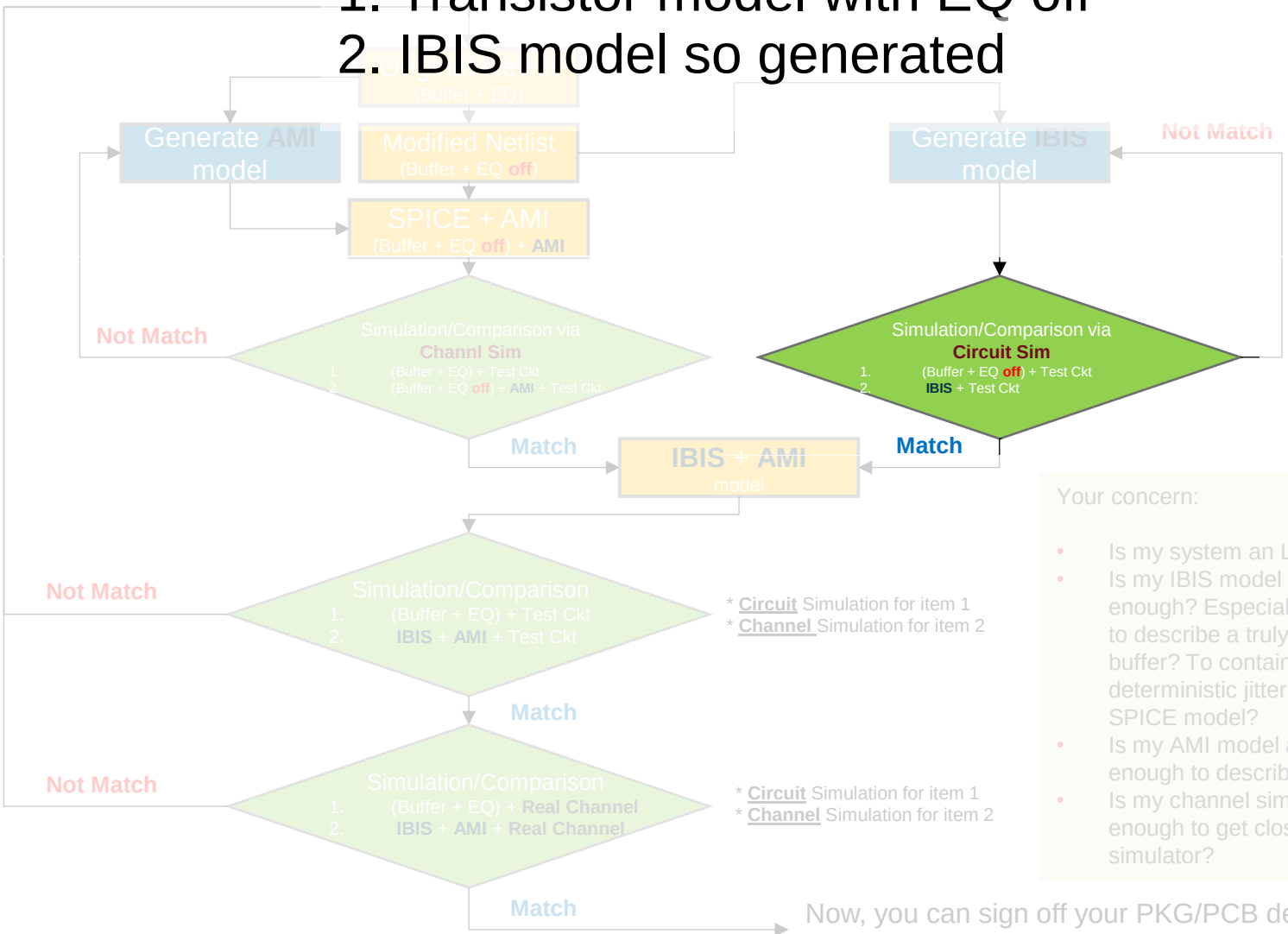
Validation 2: Circuit Simulation for

1. Transistor model with EQ off
2. IBIS model so generated



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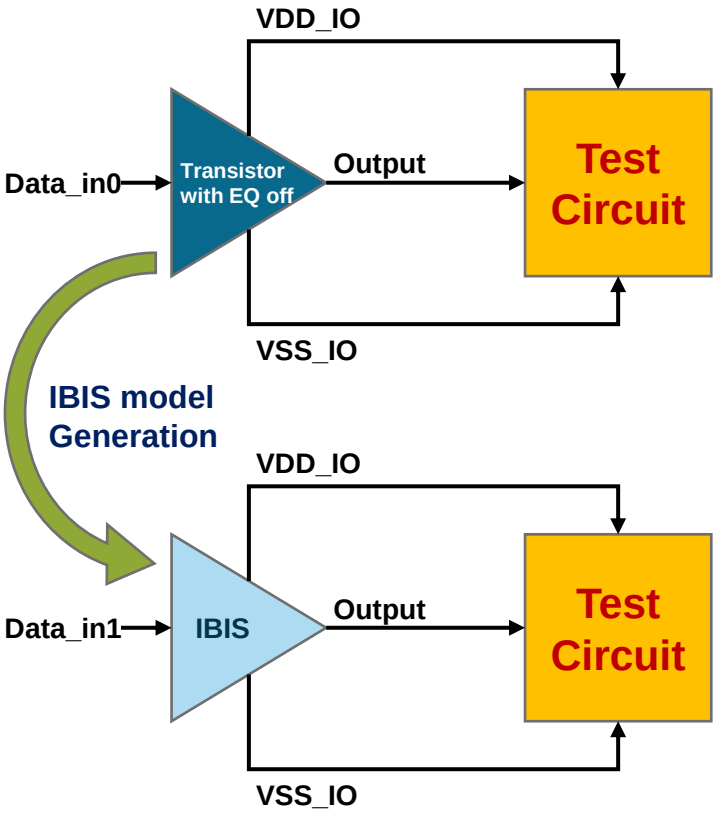
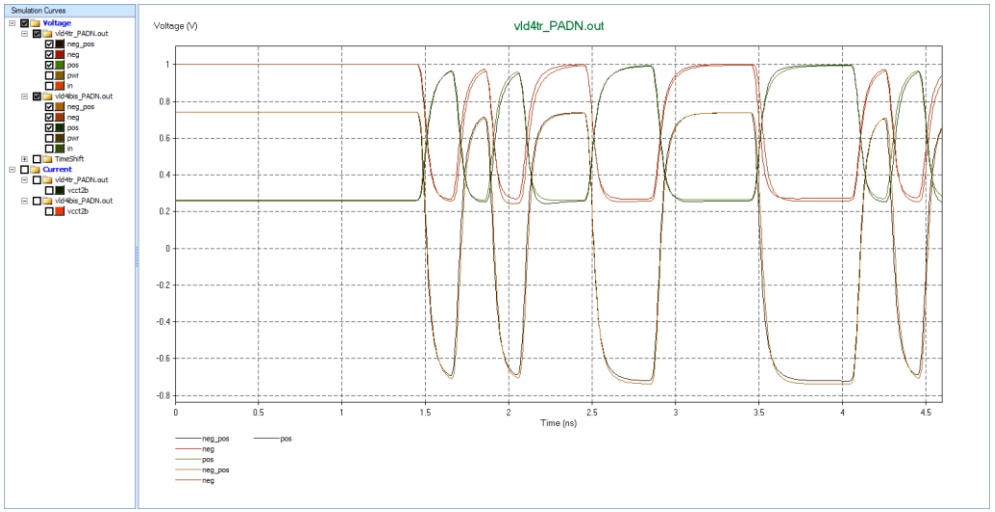
Validation 2: Circuit Simulation for

1. Transistor model with EQ off
2. IBIS model so generated

To qualify the IBIS model so generated.



Validated by Circuit Simulator



Validation 2: Circuit Simulation for

To qualify the IBIS model so generated.

1. Transistor model with EQ off
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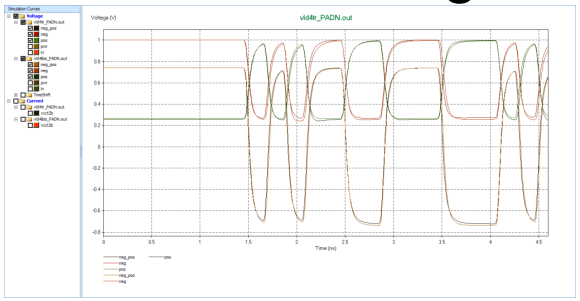

Define a "mark" and a "target" to tell the quality of the IBIS model so generated

$$FOM = 100 \bullet \left[1 - \frac{\sum_{i=1}^{N} \left| Y_i(LAB) - Y_i(IBIS) \right|}{\Delta Y \bullet N} \right]$$

ΔY: (Max-Min) of Circuit Simulation Waveform

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T2B Validation Report

Date: 15:05 October 11, 2016

1 General Information

T2B version: 16.0.2.09201 005

File names and locations:

- T2B project file: HyperCore_TX.t2b
- File location: D:/Case_CDNS_20160616_IBIS_AMI/Modelize_TX/

2 IBIS Correlation Result Summary

FOM lower limit : 97%

Model Name	Buffer Type	Load	Figure of Merit (%)	Status
CDNS_5G_TXN	Driver	S/P/G RLC	99.4	PASS
CDNS_5G_TXN	Driver	S/P/G RLC	94.3	FAIL
CDNS_5G_TXN	Driver	S/P/G RLC	98.2	PASS
CDNS_5G_TXN	Driver	S/P/G RLC	98.2	PASS

3 Simulation Results

3.1 Model Validation Task 1

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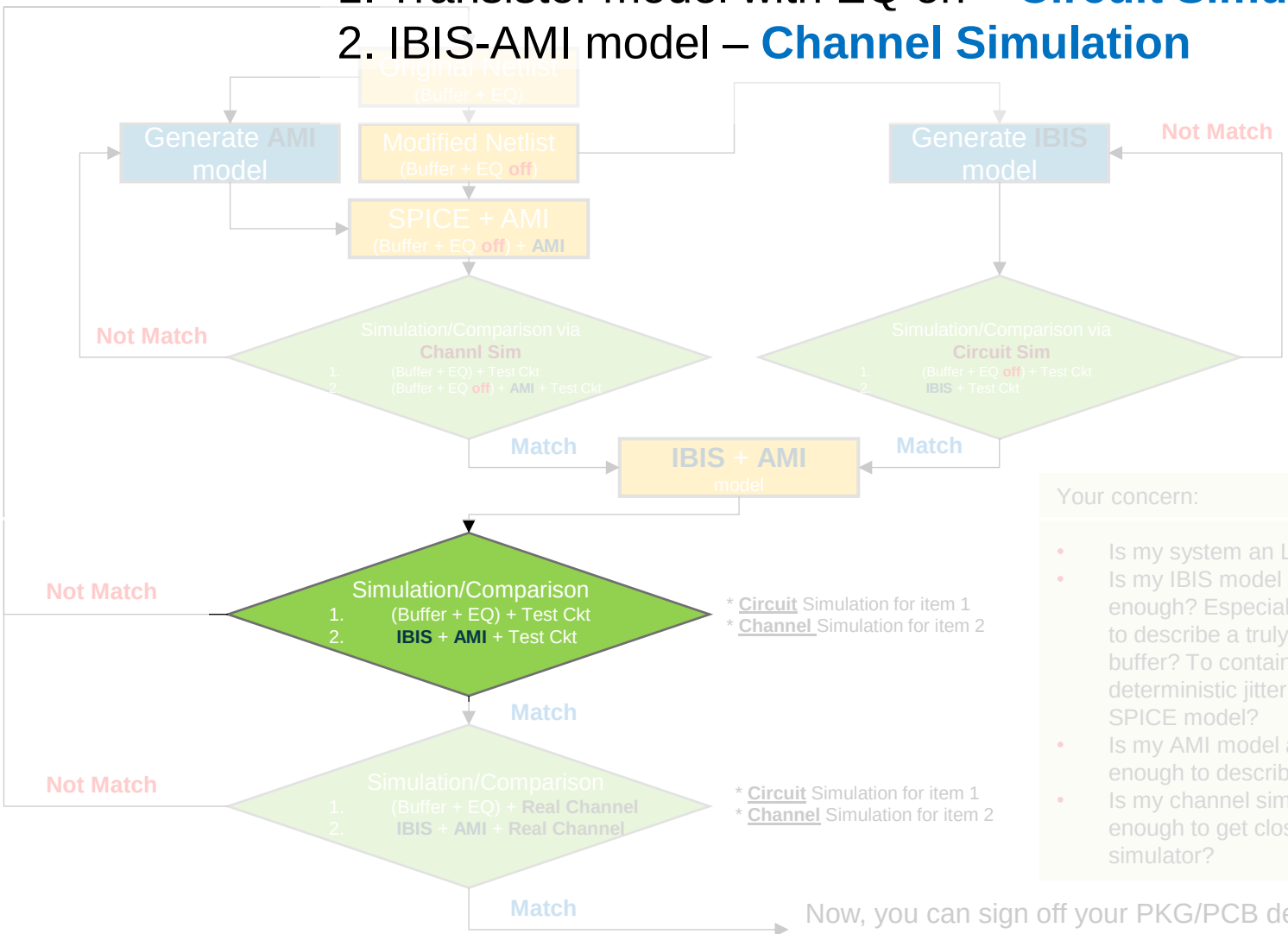
Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**



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Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**

To qualify the IBIS-AMI model so generated.

```
XTX_hspice_model in idriver<3> idriver<2> idriver<1> idriver<0>
+ preemphasis_post<3> preemphasis_post<2> preemphasis_post<1> preemphasis_post<0>
+ preemphasis_pre<2> preemphasis_pre<1> preemphasis_pre<0> sel_halfrate
+ pos neg pwr ngnd [redacted]

vidriver<3> idriver<3> 0 1.2
vidriver<2> idriver<2> 0 0
vidriver<1> idriver<1> 0 0
vidriver<0> idriver<0> 0 0

vpre_post<3> preemphasis_post<3> 0 1.2
vpre_post<2> preemphasis_post<2> 0 0
vpre_post<1> preemphasis_post<1> 0 0
vpre_post<0> preemphasis_post<0> 0 0
vpre_pre<2> preemphasis_pre<2> 0 1.2
vpre_pre<1> preemphasis_pre<1> 0 0
vpre_pre<0> preemphasis_pre<0> 0 0
vsel      sel_halfrate 0  0
```

Test Fixture

2. IBIS-AMI model – **Channel Simulation**

AMI Model

Pre | Main | Post

"-0.06348943, 0.541411754, -0.111743042"

```
[Model] CDNS_5G_TXP
Model_type Output
Polarity        Non-Inverting
C_comp    2.120pF           2.104pF           2.272pF
C_comp_pullup    0.354pF           0.347pF           0.36
C_comp_pulldown    0.749pF           0.738pF           0.
|
[Temperature Range]    27.000           100.000
[Voltage Range]         1.200V            1.080V
[Pulldown]
|Voltage    I(typ)           I(min)           I(max)
|
-1.200V    -1.2082A          -1.4705A          -1.1135A
-1.163V    -1.0791A          -1.3481A          -0.9816A
-1.126V    -0.9501A          -1.2258A          -0.8511A
```

Test Fixture

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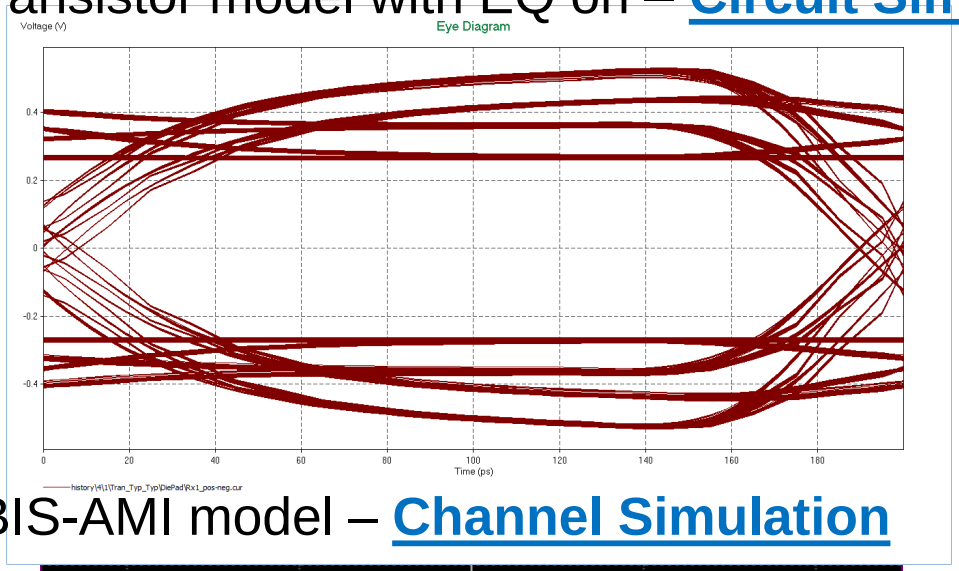
Validation 3: **Test Circuit** follows

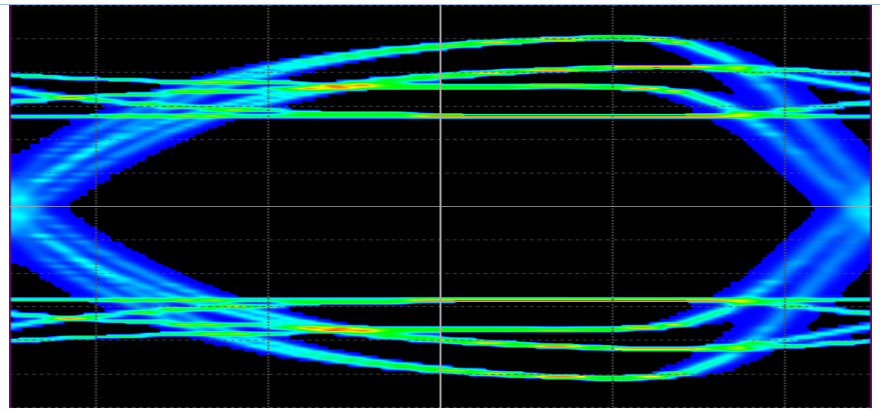
To qualify the IBIS-AMI model so generated.

1. Transistor model with EQ on – **Circuit Simulation**



(1,024 bits transmitted)

2. IBIS-AMI model – **Channel Simulation**

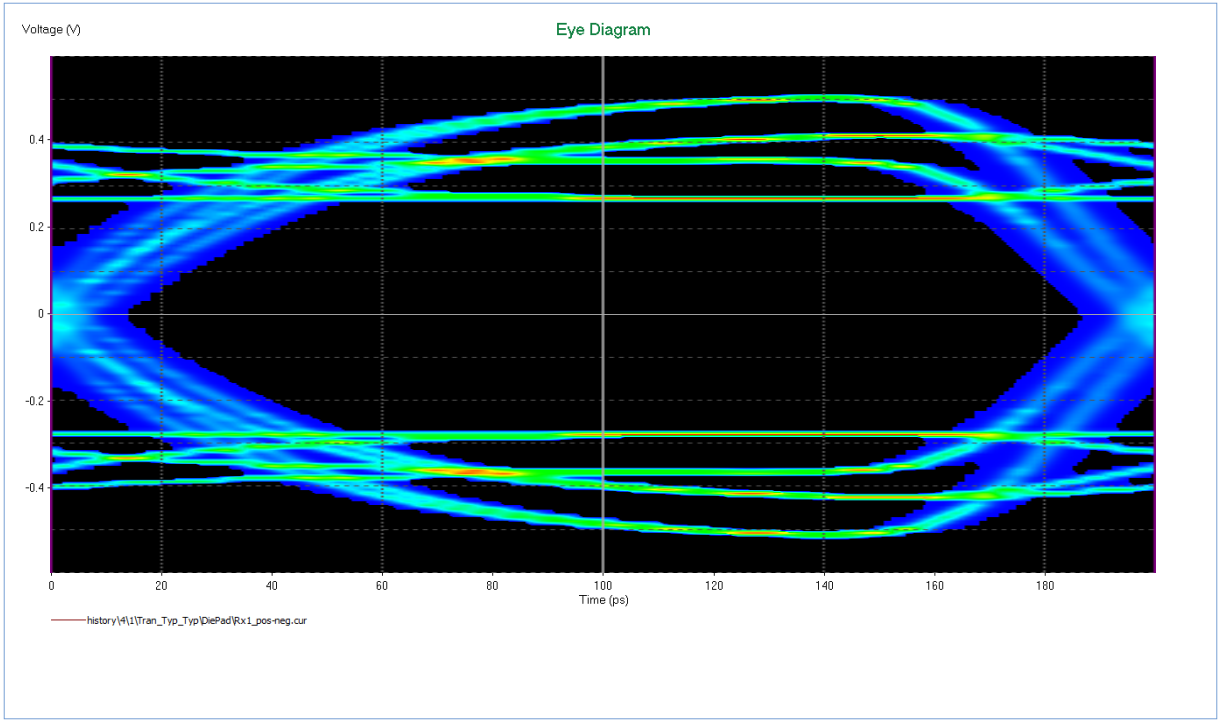


(1e+16 bits transmitted)

Validation 3: **Test Circuit** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

To qualify the IBIS-AMI model so generated.



Also, to qualify the Channel Simulator – if the Channel Simulator behavior close enough to the Circuit Simulator.

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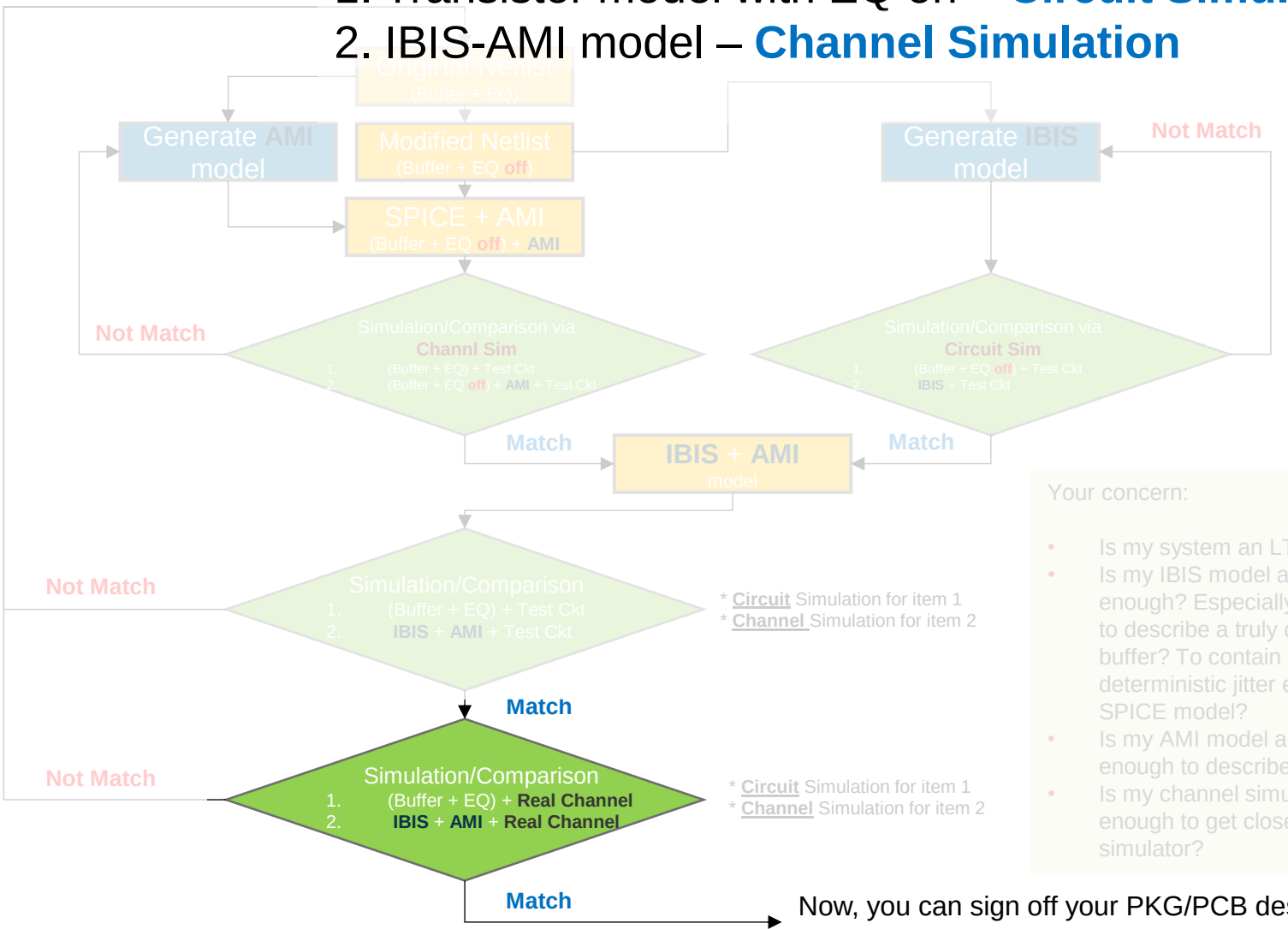
Validation 4: **Real Channel** follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**



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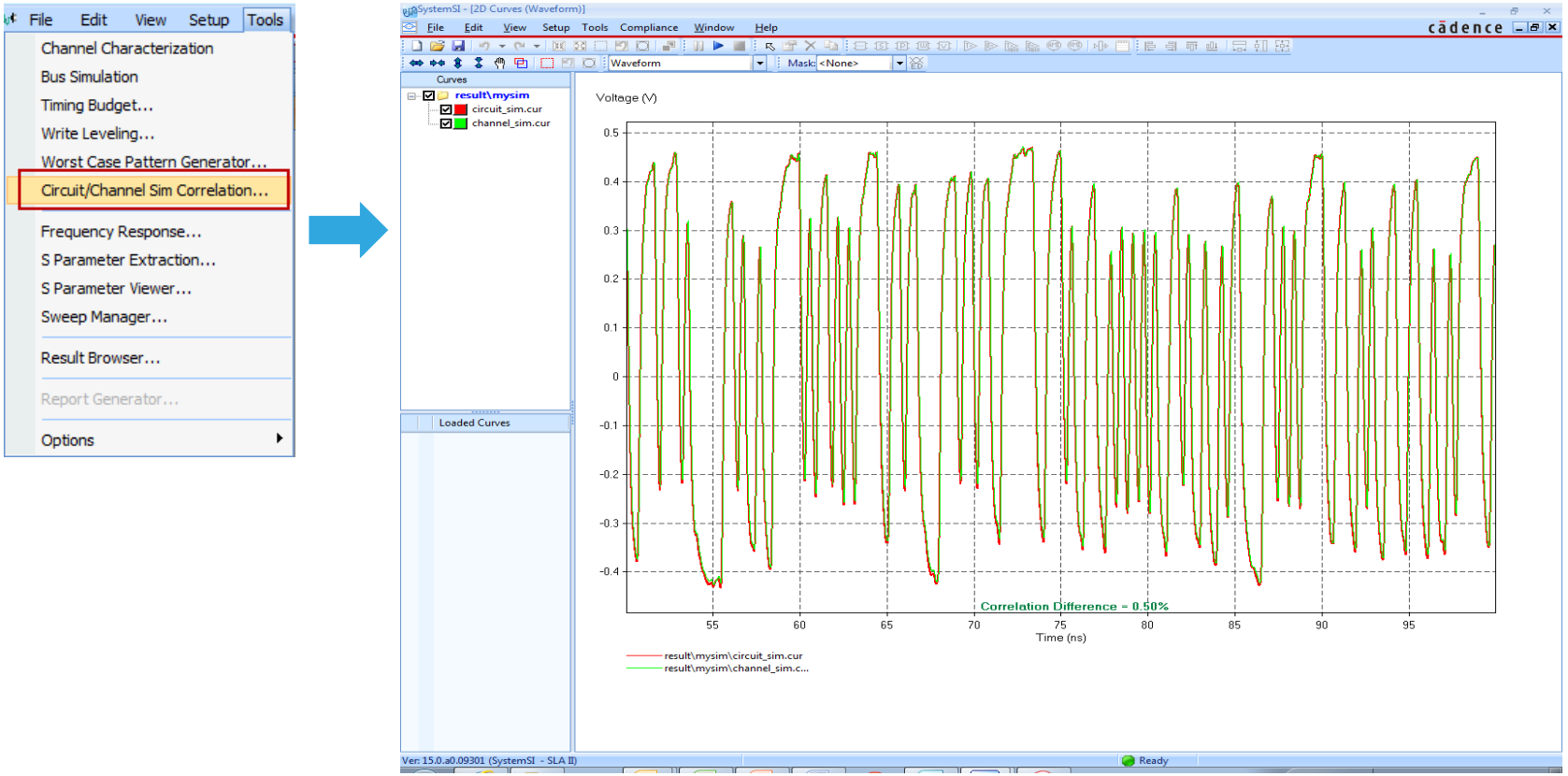
Now, you can sign off your PKG/PCB design with the IBIS+AMI model so generated

Validation 4: Real Channel follows

1. Transistor model with EQ on – **Circuit Simulation**
2. IBIS-AMI model – **Channel Simulation**

- First of all, check if your system/channel to be analyzed can be treated as LTI or not:



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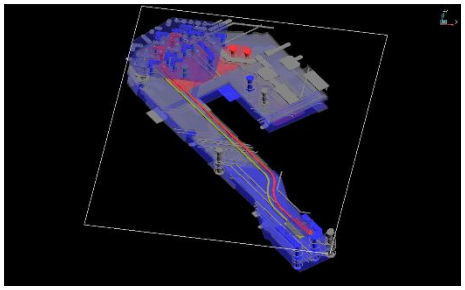
Validation 4: Real Channel follows



1. Transistor model with EQ on – **Circuit Simulation**
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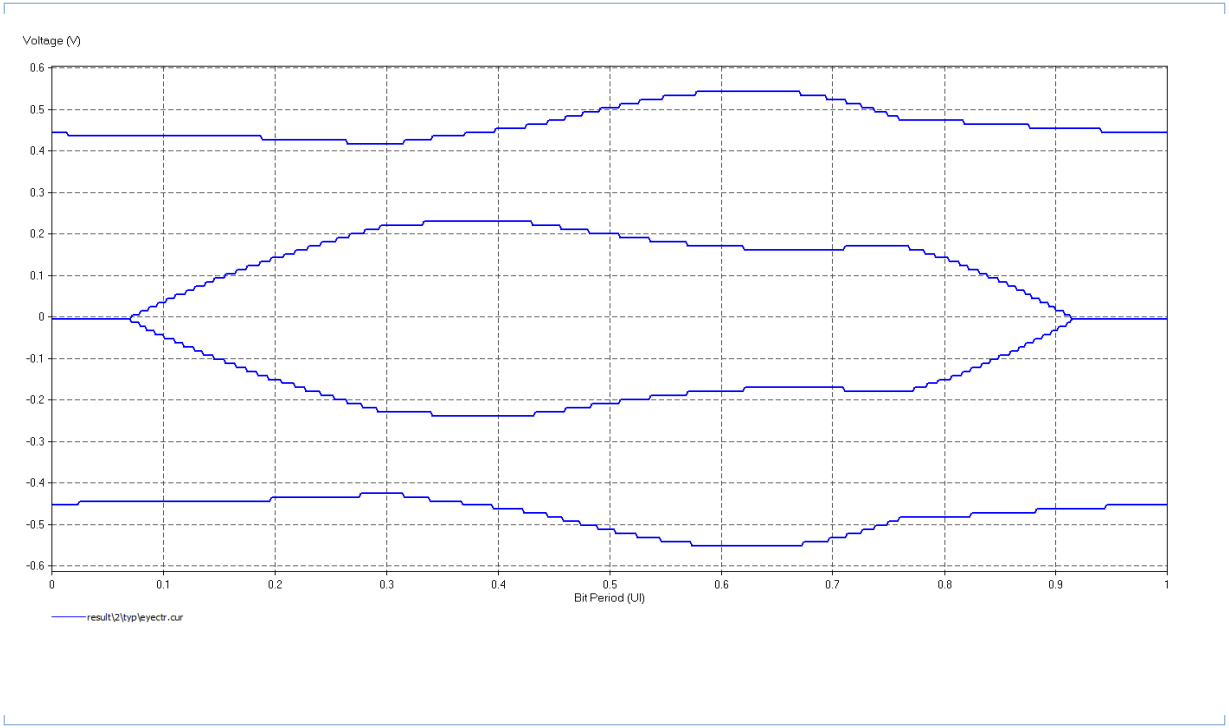

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Circuit Simulation

Channel simulation
- LTI system
- Channel simulation

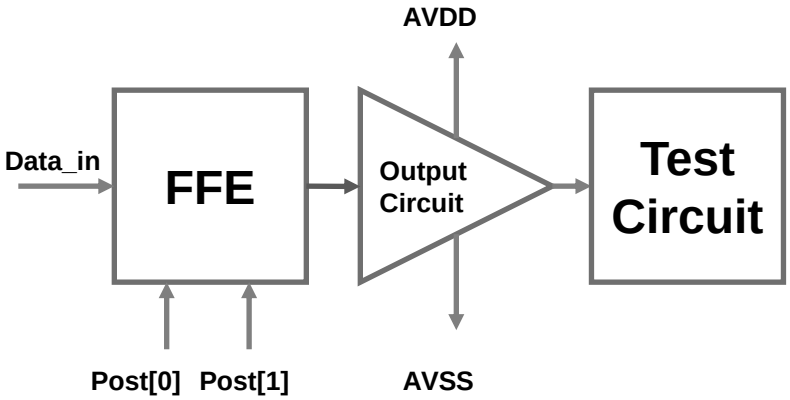
IBIS+AMI model
- What is IBIS+AMI model
- And your concerns?

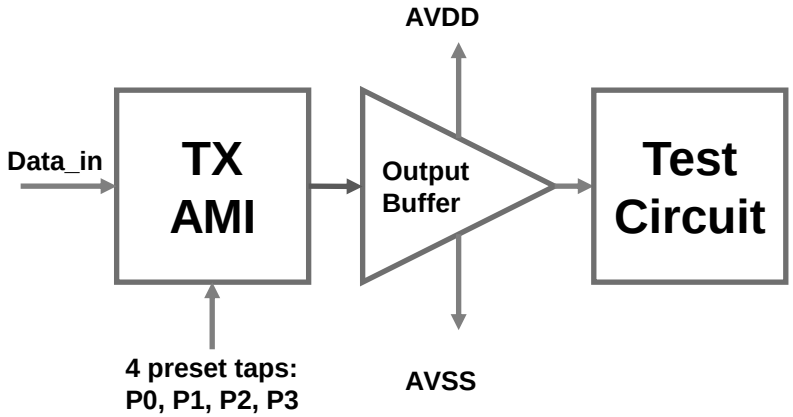
IBIS+AMI model generation flow – Validation is the KEY!!

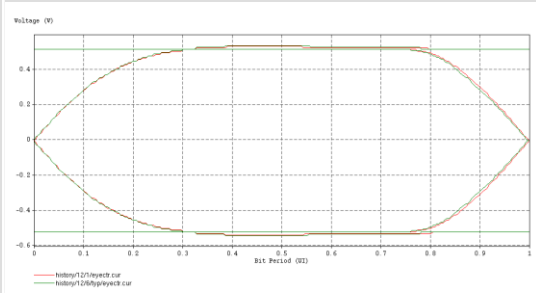
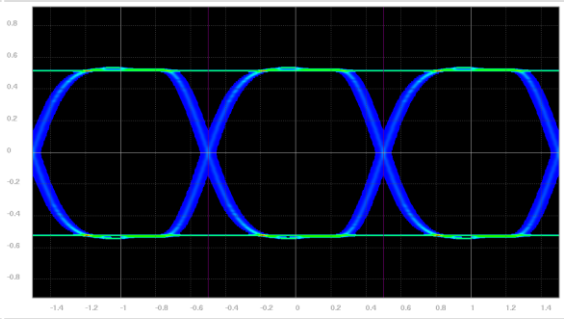
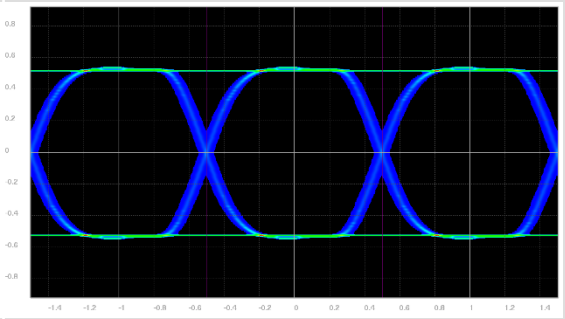
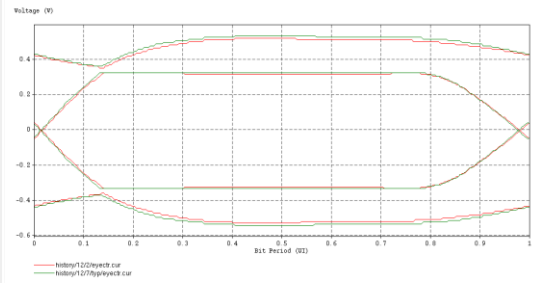
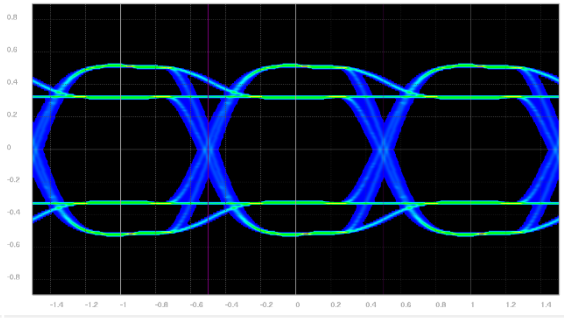
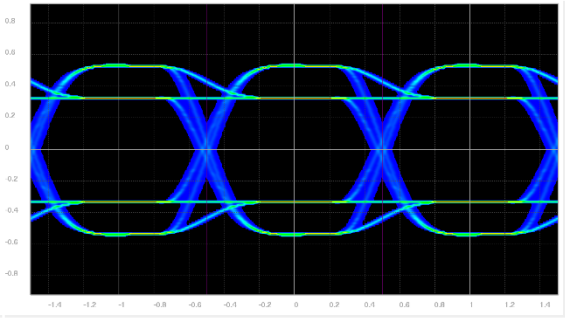
Successful Stories:
1. USB 3.0 TX – An Output Buffer + FFE
2. USB 3.0 RX – An Input Buffer + AGC + CTE
3. A System – USB 3.0 TX + Channel (PCB+Conn+3m Cable) + USB 3.0 RX

Conclusion

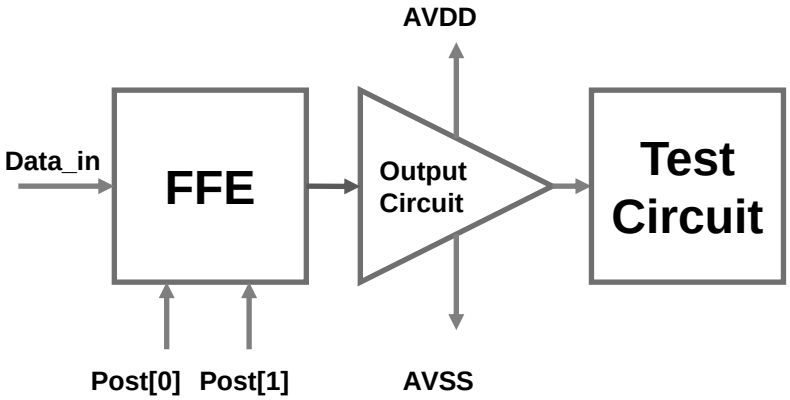
USB 3.0 TX

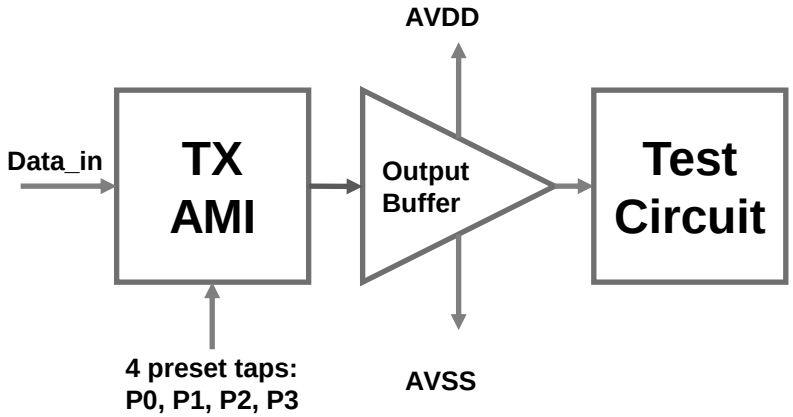


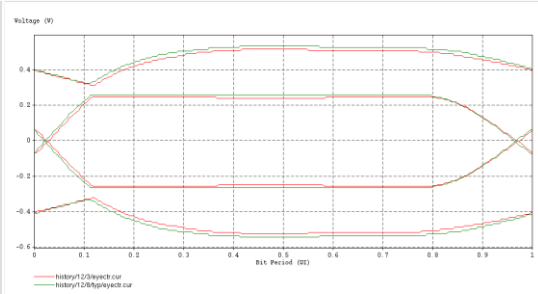
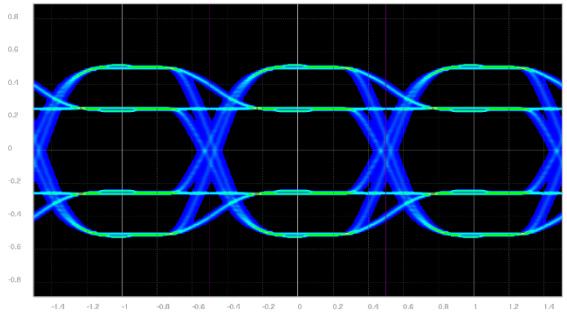
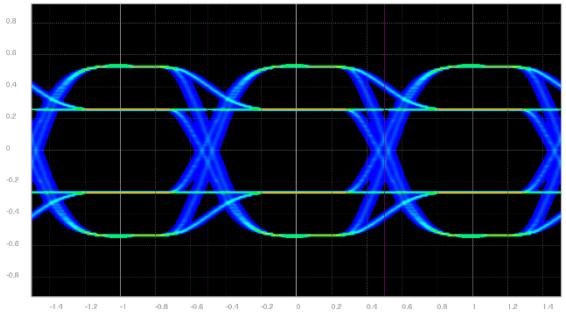
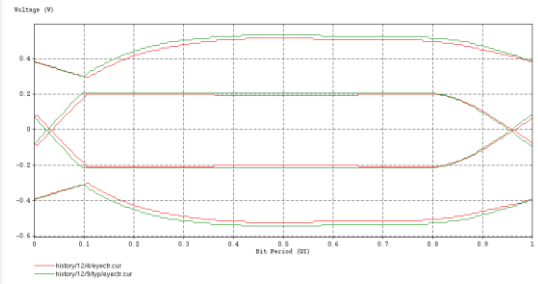
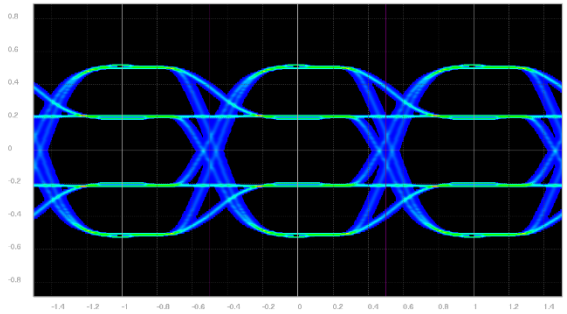
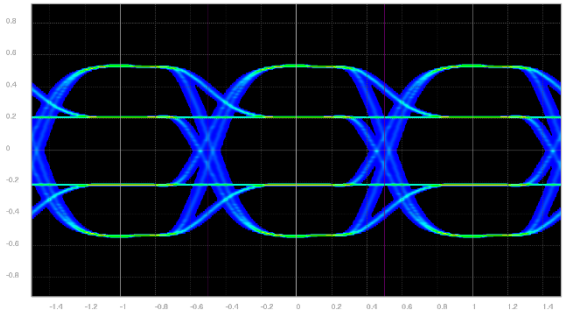


	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
0dB			
3dB			

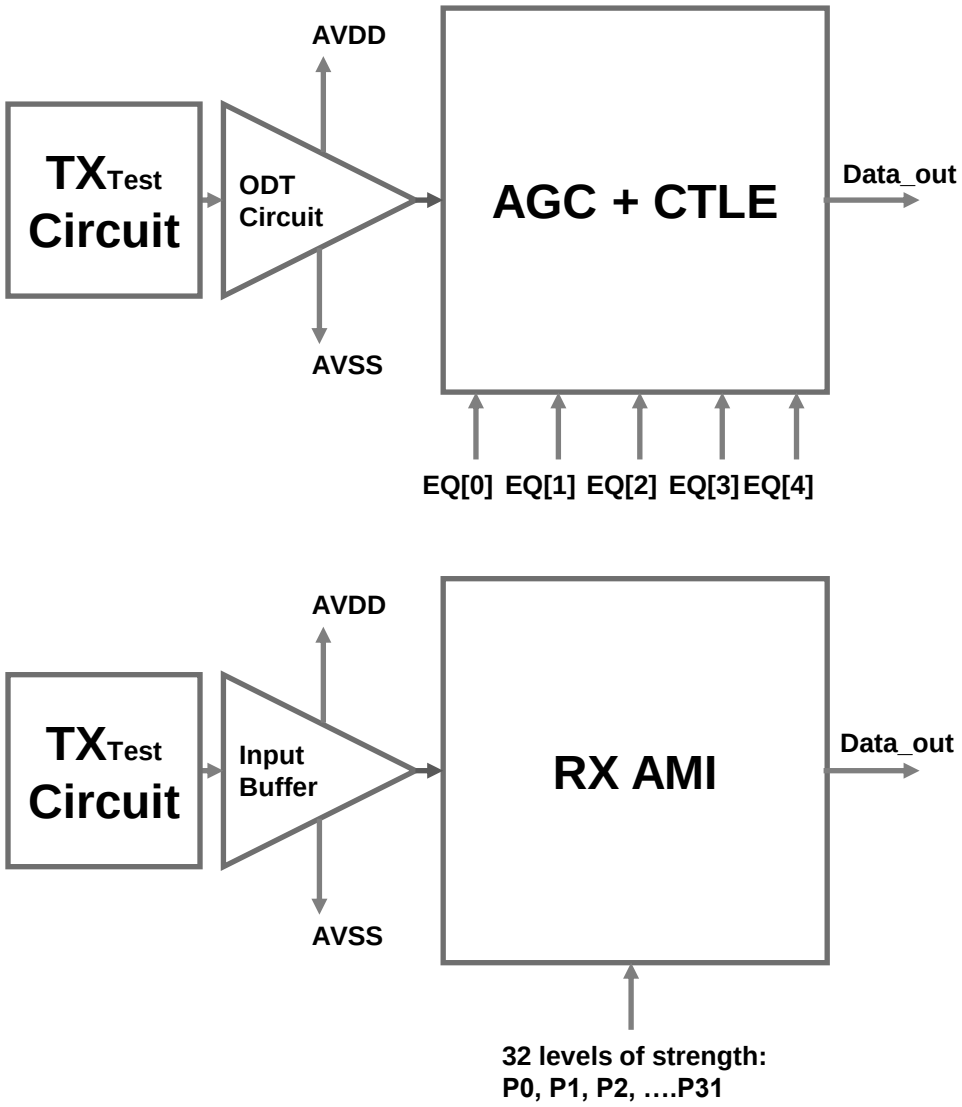
USB 3.0 TX



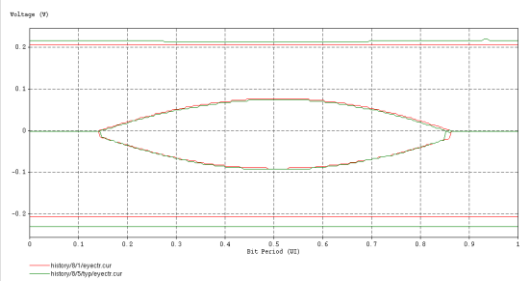
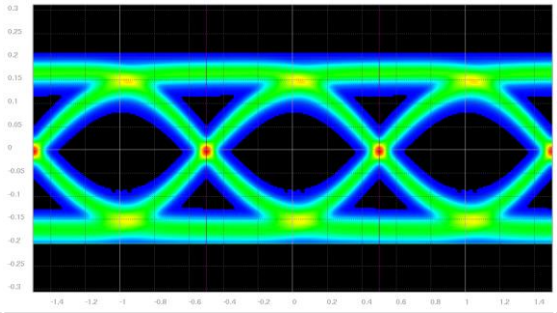
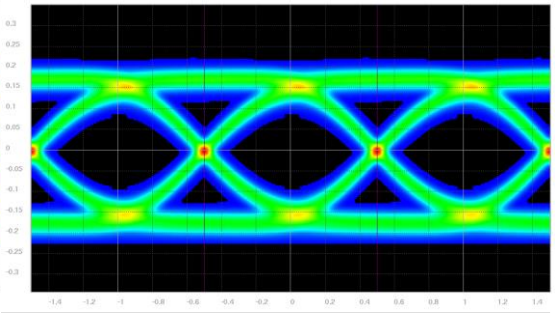
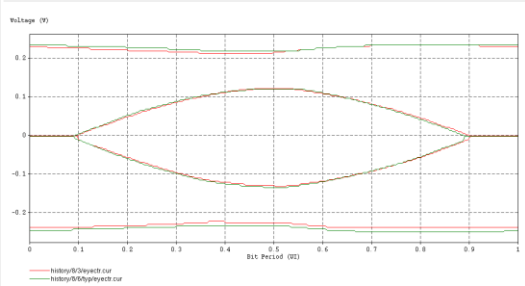
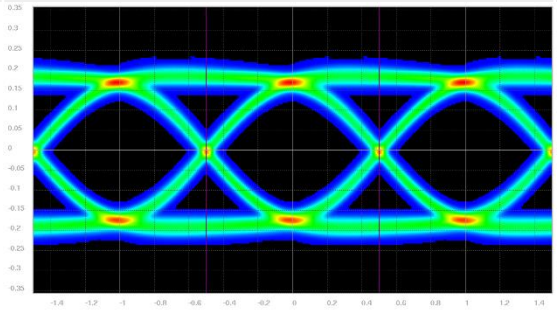
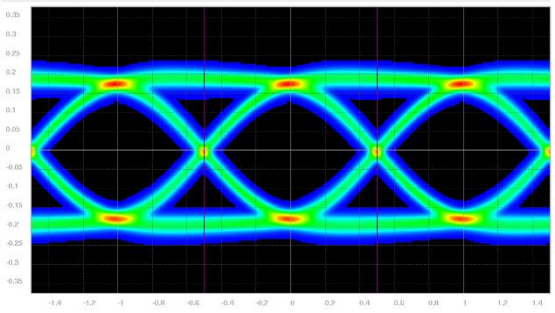
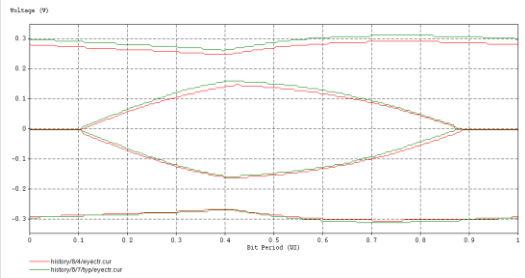
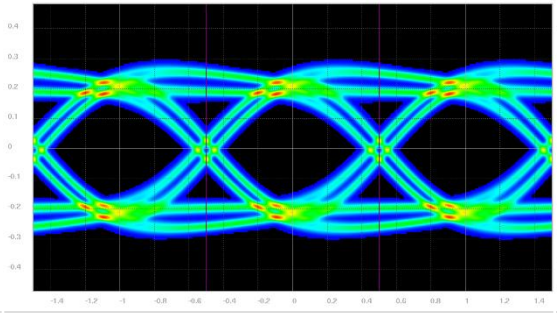
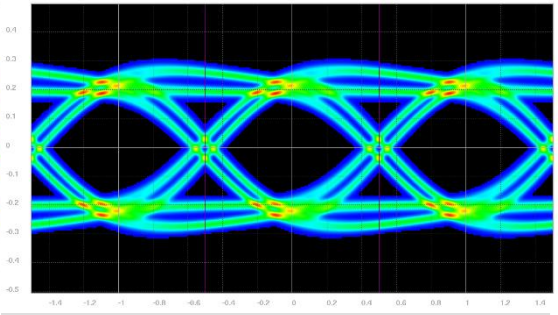


	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
6dB			
8dB			

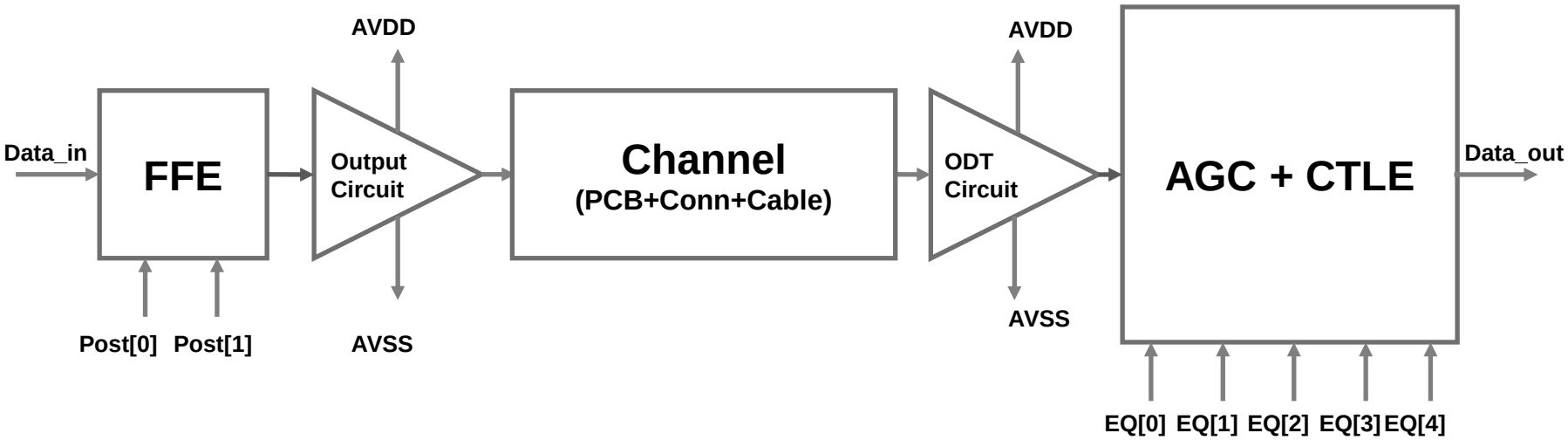
USB 3.0 RX



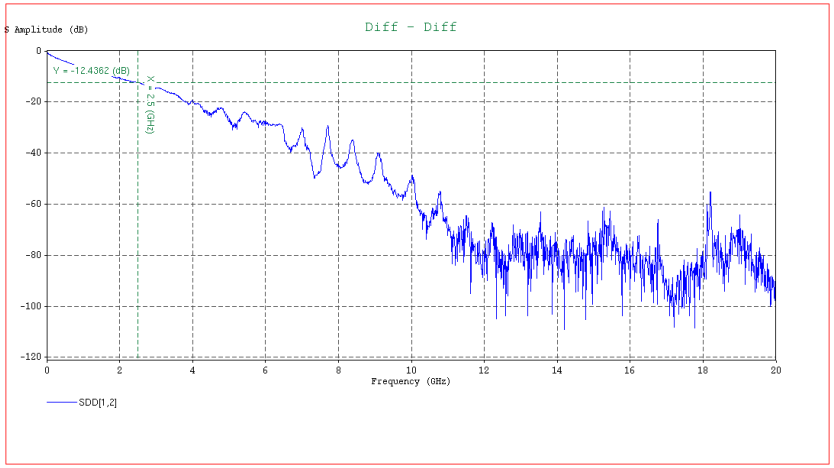
USB 3.0 RX

	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
00100			
00110			
01010			

A System –
USB 3.0 TX + Channel + USB 3.0 RX

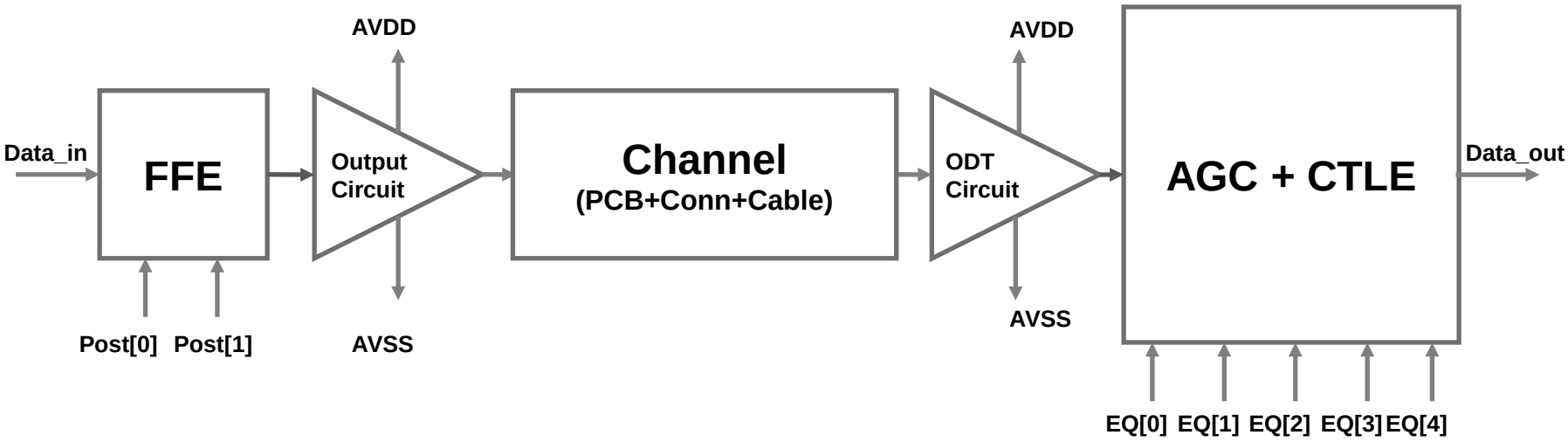


- Channel Insertion Loss

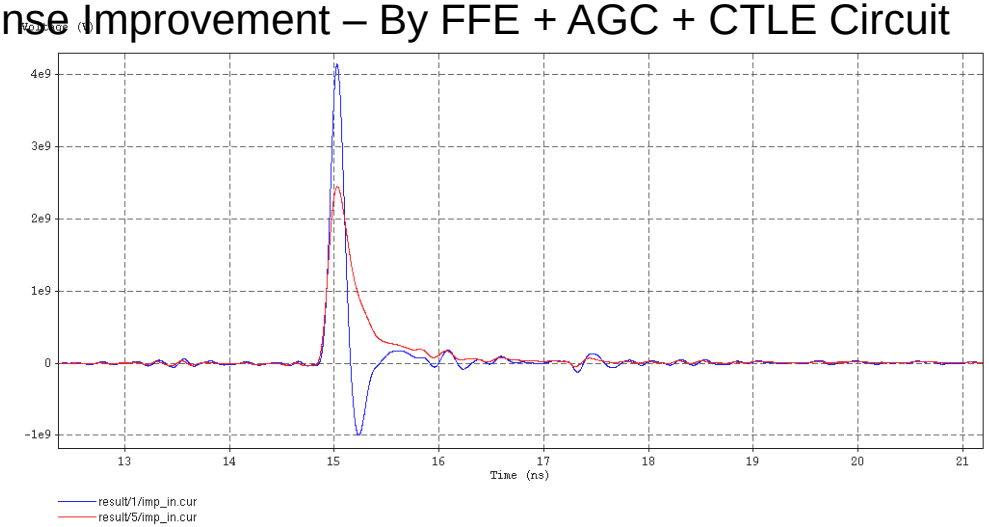


cadence

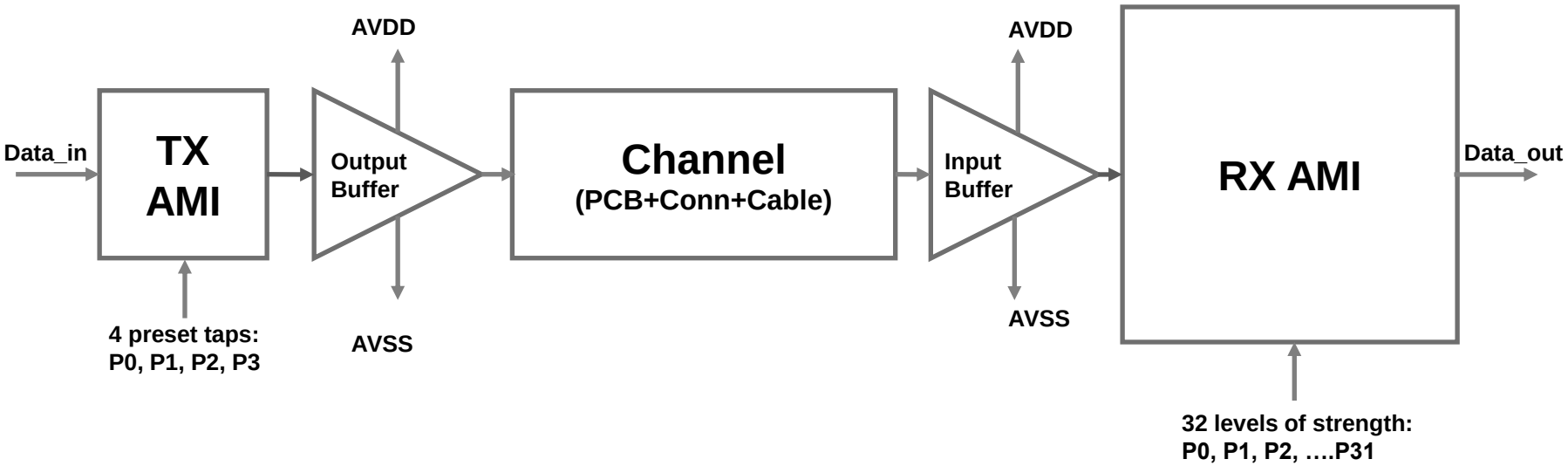
A System –
USB 3.0 TX + Channel + USB 3.0 RX

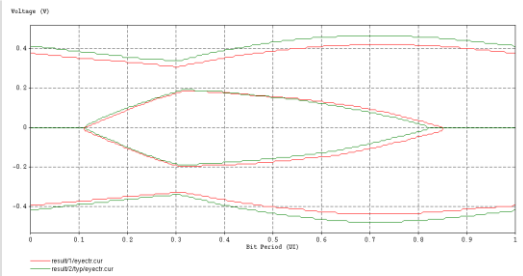
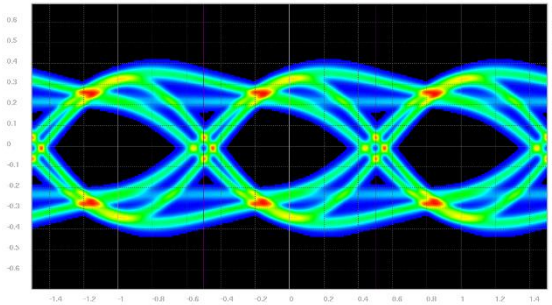
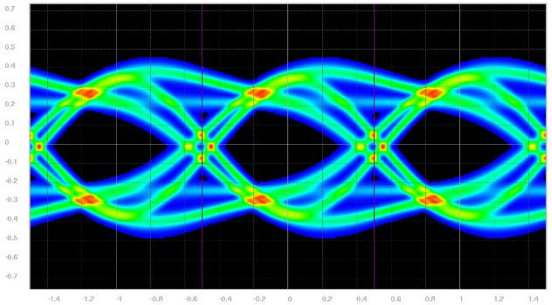


- Impulse Response Improvement – By FFE + AGC + CTLE Circuit



A System –
USB 3.0 TX + Channel + USB 3.0 RX



	Eye Contour	Distribution Eye – Circuit Netlist	Distribution Eye – IBIS+AMI model
TX=3dB RX= 00110			

Agenda

- Circuit Simulation
- Channel simulation
  - LTI system
  - Channel simulation
- IBIS+AMI model
  - What is IBIS+AMI model
  - And your concerns?
- IBIS+AMI model generation flow – Validation is the KEY!!
- Successful Stories:
  1. TX – An Output Buffer + FFE
  2. RX – An Input Buffer + AGC + CTE
  3. A System – TX + Channel + RX
- Conclusion

Conclusion

- An accurate IBIS+AMI model could be an alternative approach to validate your “system” design versus a transistor netlist model
- An accurate IBIS-AMI model consists of two parts – an **accurate IBIS model** and **an accurate AMI model** – **validation** is the key
- An accurate IBIS should be generated by a tool which can well describe a **truly differential pair** in all V/I, V/T and I/T curves.
- An accurate AMI model should be generated by a tool with a rich library such that the generation tool can use all available means in the library to describe all your possible designs.
- A simulation environment which supports transistor netlist models is fundamental for IBIS+AMI model generation/validation.