Necessity for integrating FEC functionality for PAM4 in AMI simulations

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Agenda

- Review of AMI simulation methodology

- FEC simulation introduction for PAM4 link

- Summary and suggestion

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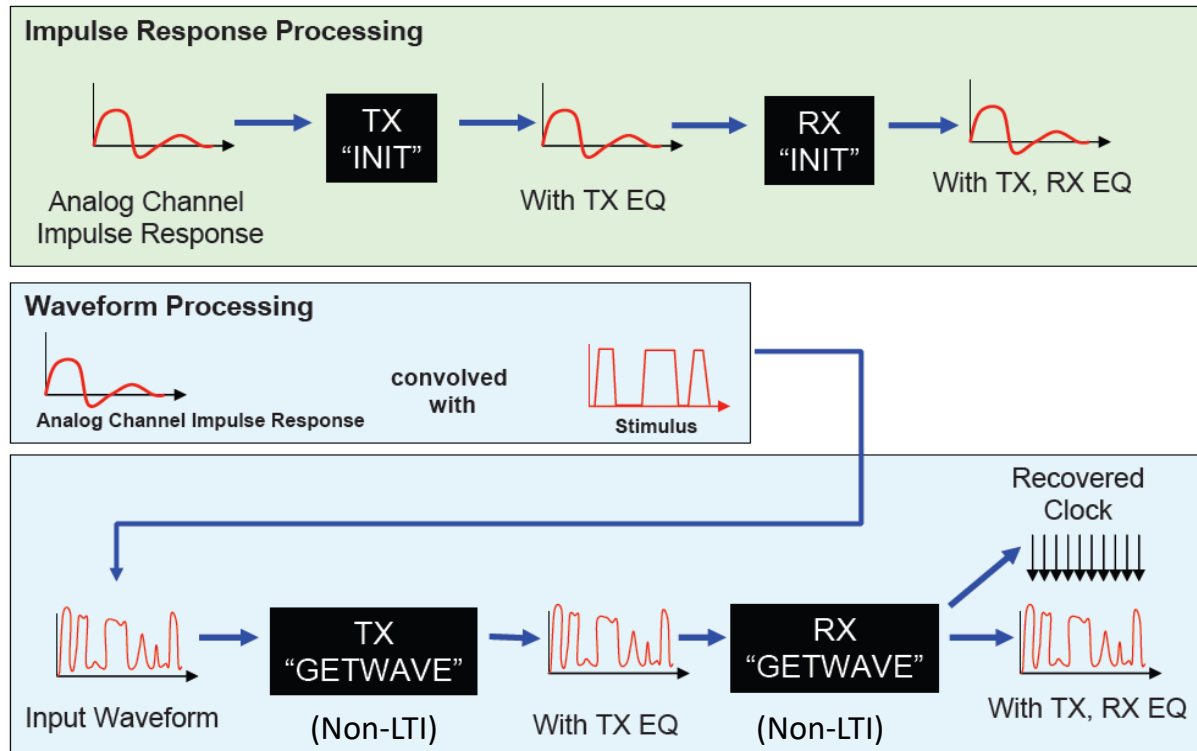# General AMI simulation methodology

Figure cited from IBIS summit proposal archive

- TX FFE, RX linear equalization is processed in *AMI_Init* function;

- RX CDR, DFE are mostly modeled in *AMI_GetWave* function;

- Converged equalization parameters can be output using *AMI_parameters_out;*

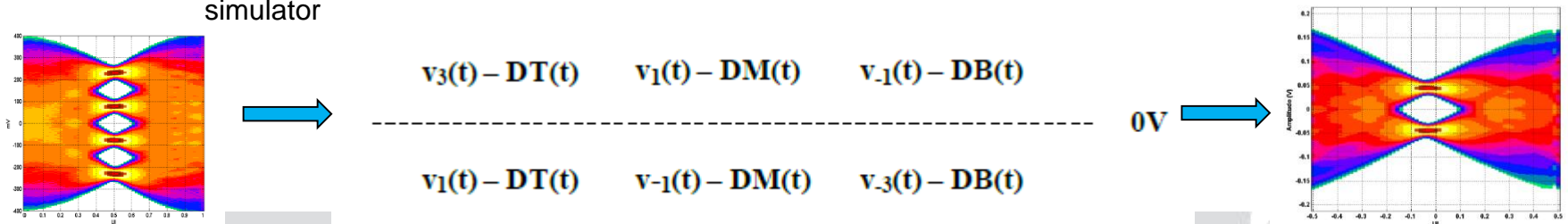- BER targets are set by users to monitor link qualities.

PAM4 simulations in AMI

- AMI defines SerDes behavioral modeling interface and an efficient channel simulation methodology. A graphical representation is given in Figure below.
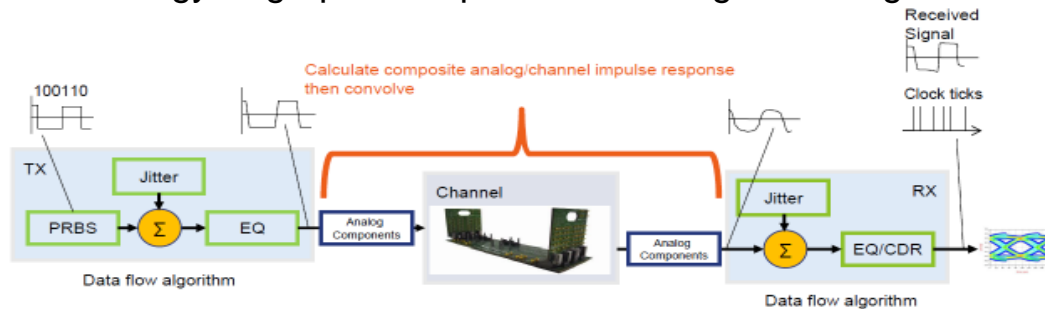

Reference: Hongtao Zhang , Fangyi Rao, Xiaoqing Dong, Geoff Zhang, IBIS-AMI Modeling and Simulation of 56G PAM4 Link Systems, Designcon 2015

- Minimum modifications are proposed in order for the current AMI model to handle PAM4 signal simulations:
  - It is proposed that {0.5V, 0.5/3V, -0.5/3V, -0.5V} are used to represent the 4 levels in PAM4, {3, 1, -1 and -3}.
  - It is proposed to add RX slicer levels to the reserved parameter list in *AMI_GetWave* with Usage Out.
  - It is proposed that a merged NRZ-equivalent eye can be formulated through post processing in a simulator

$$v_3(t) - DT(t) \qquad v_1(t) - DM(t) \qquad v_{-1}(t) - DB(t)$$
$$\text{---} \qquad 0V$$
$$v_1(t) - DT(t) \qquad v_{-1}(t) - DM(t) \qquad v_{-3}(t) - DB(t)$$

The industry existing/emerging PAM4 standards

➢ 28G generation: IEEE-802.3bj-KR4
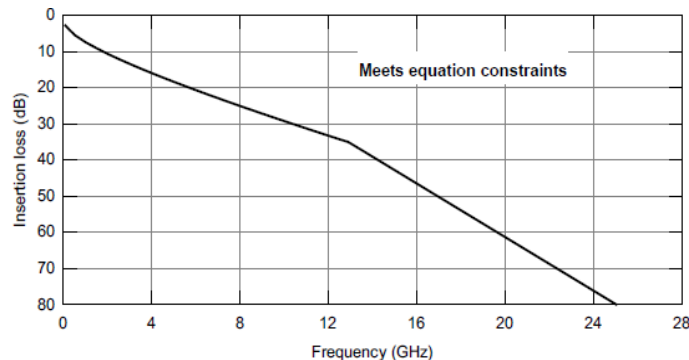
1.4.53b 100GBASE-KR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 2-level pulse amplitude modulation over four lanes of an electrical back-plane, with a total insertion loss up to 35 dB at 12.9 GHz. (See IEEE Std 802.3, Clause 93.)

The receive path of the RS-FEC sublayer may have the option to perform error detection without correction to reduce the data delay (see 91.5.3.3). When the receive path of the RS-FEC sublayer performs error correction, the link is required to operate with a BER of 10^{-5} or better. When the RS-FEC sublayer is configured to bypass error correction, the link is required to operate with a BER of 10^{-12} or better. In this

FEC is mandatory in major PAM4 standards to assure basic link BER target!

➢ 56G generation: OIF-CEI-56G

A raw BER better than or equal to 1E-4 is required per lane. A compliant receiver, when receiving from a compliant transmitter over a compliant channel, shall deliver the specified raw BER to the subsequent FEC decoder, including burst errors. The burst error length delivered to the PAM4 decoder having more than 65 PAM4 symbol errors shall have a probability of less than 1E-20. (see, 18.A Appendix -, 18.B Appendix -)

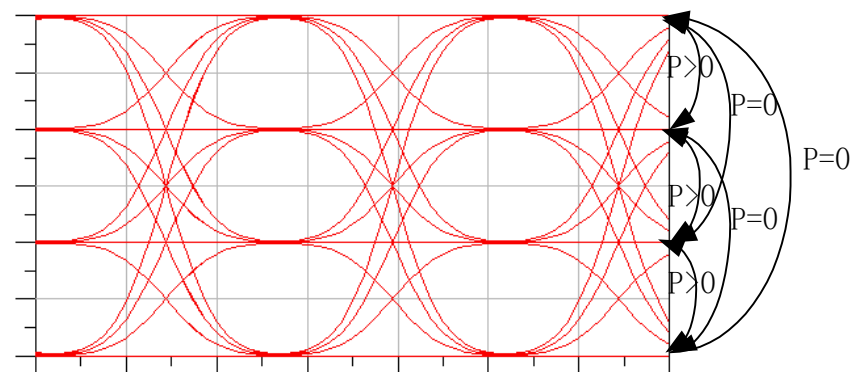➢ Emerging commercial simulators support BER simulations up to no better than 1e-5 or 1e-4 for PAM4, according to industry standards. This works for NRZ, but considering FEC has become crucial to enable basic link performance for PAM4, and error propagation of different SerDes makes different error distribution features in an actual link, it is suggested that FEC functionalities be integrated in AMI for PAM4.

PAM4 vs. NRZ: error propagation mechanism

- Given span-symbol error has very low occurrence probability, symbol error is assumed to occur across adjacent levels in PAM4. This approach simplifies the calculation of erroneous voltages, and makes an uniform calculation procedure of PAM4 and NRZ.

- For PAM4, errors only occur between (1,1/3), (1/3,-1/3) and (-1/3,-1). The scaling factor for erroneous voltage offset is 2/3 x DFE coefficients.

- $1+Z^{-1}$ coding scheme can't solve the error propagation issue introduced from DFE.

$$
\frac{11}{\underline{}} \quad \frac{10}{\underline{}}
$$

```
11          10
―――         ―――
10          11    Gray
―――  Linear ―――
01          01
―――         ―――
00          00
```

Binary bits to PAM4 mapping
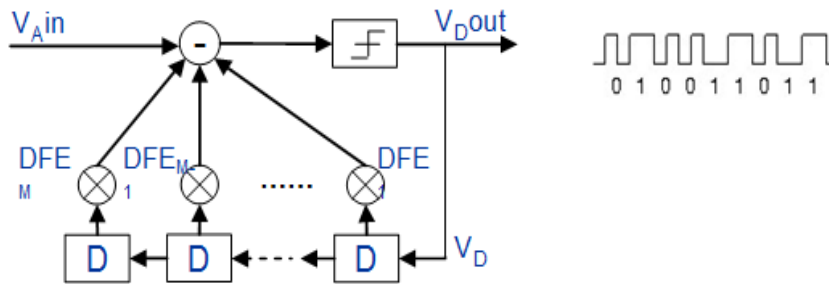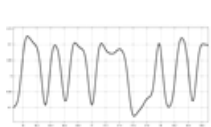

P>0 P=0 P=0 P>0 P=0 P>0

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FEC simulation methodologies

- There are multiple approaches to enable FEC simulation in industry. The one we implemented, is based on burst error probability calculation, where burst error length is set to be long enough to assure calculation accuracy, given converged DFE coefficients and error propagation probabilities.

$$BER = \sum_{i=1}^{rll_{max}} \sum_{allE} p(rll = i, E) \cdot W(E) \cdot p_1 \cdot (1 - p_1)^{n - rll_{max} - i}$$

- random error probability
- the probability that i bits in error among a n bit block
- all the combinations of the error pattern when error propagation length is i
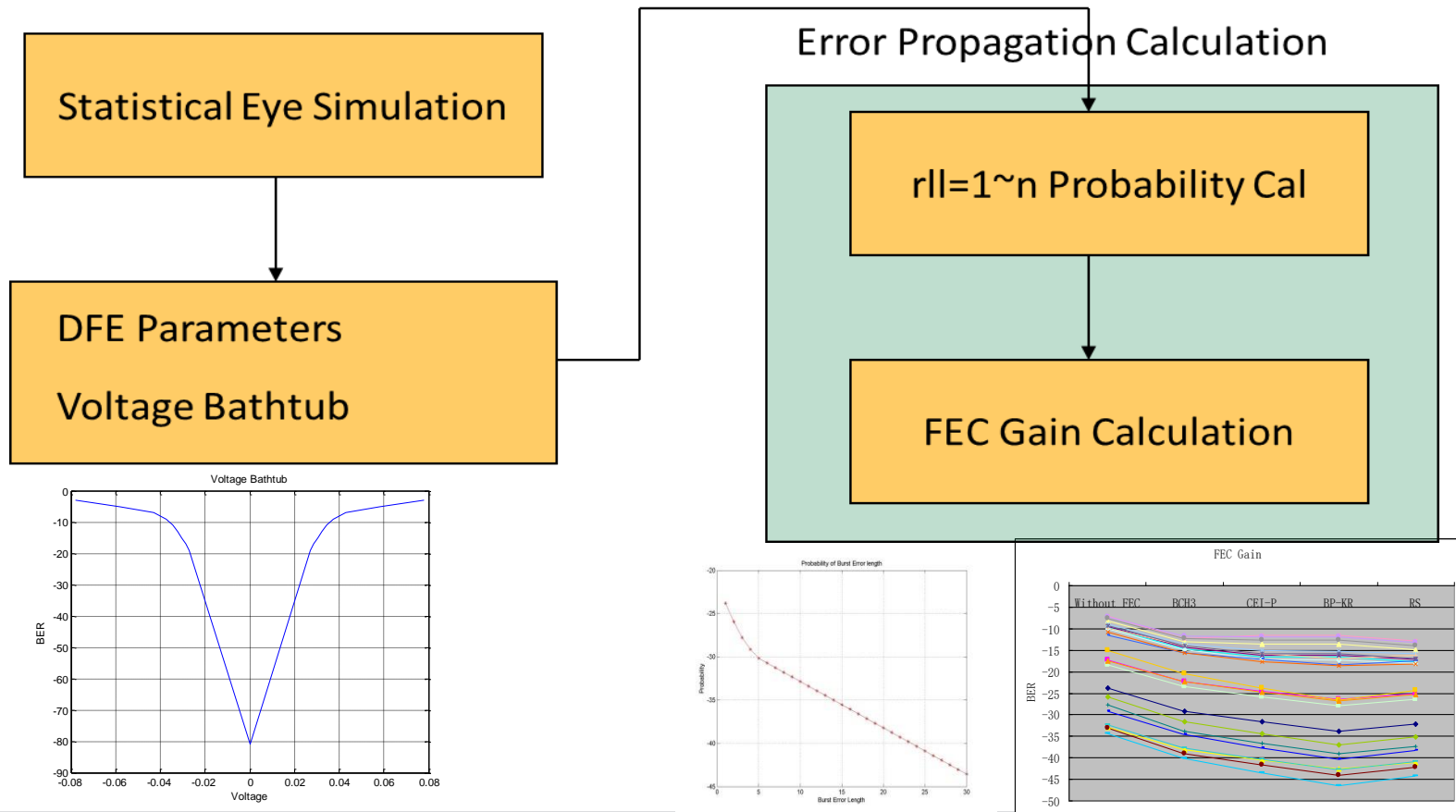- maximum error propagation length

$V_A in$ $V_D out$

0 1 0 0 1 1 0 1 1

DFE$_M$ DFE$_{M1}$ ...... DFE$_1$

D ← D ← ···· ← D ← V_D

$$V_D out(t_0) = V_A in(t_0) - DFE_1 \cdot V_D(t_{-1}) - DFE_2 \cdot V_D(t_{-2}) - ... - DFE_M \cdot V_D(t_{-M})$$

Probability of Burst Error length

DEMO

Probability vs Burst Error Length

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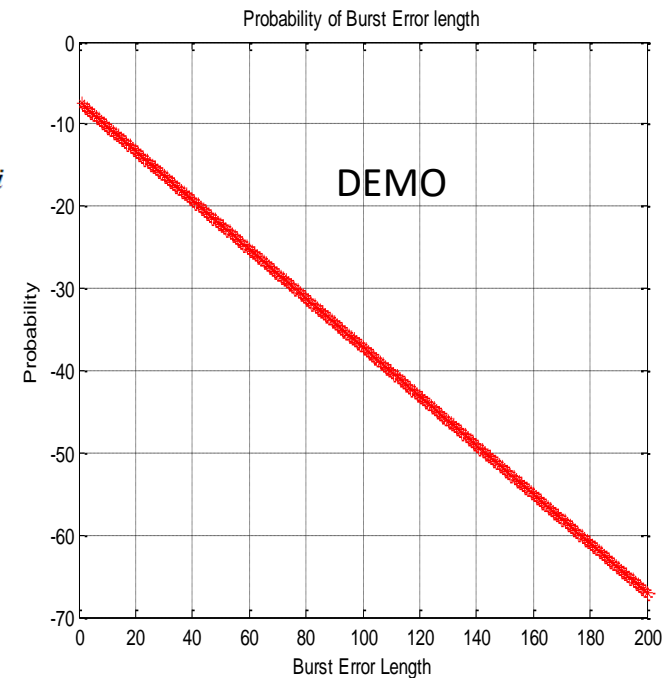
FEC simulation methodologies – cont'd

- The proposed methodology supports one-tap DFE error propagation simulation that is routinely used in standards, it also supports multi-tap DFE, multi-type RS codes simulation scenarios, which are more practical for engineering applications.

System simulation case study: PAM4 vs. NRZ

Simulation condition:

- One-tap DFE model adopted;
- One symbol error causes error propagation spanning two-bit length. RS(544,514) defined in KP4 standard does not gain much compared to RS(528,514) in KR4 standard.
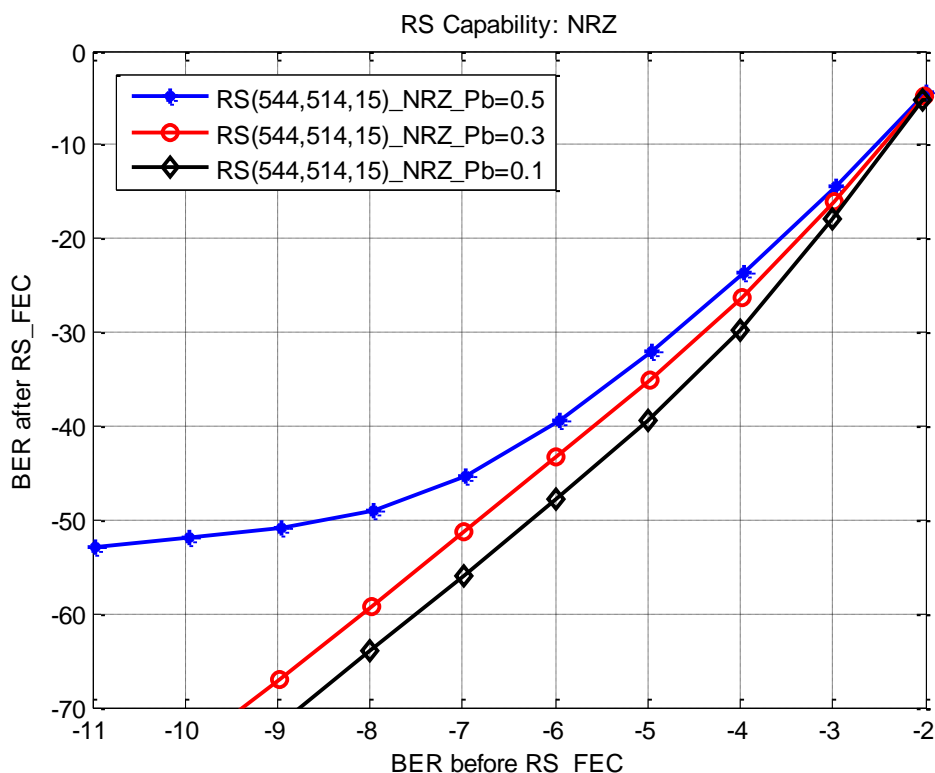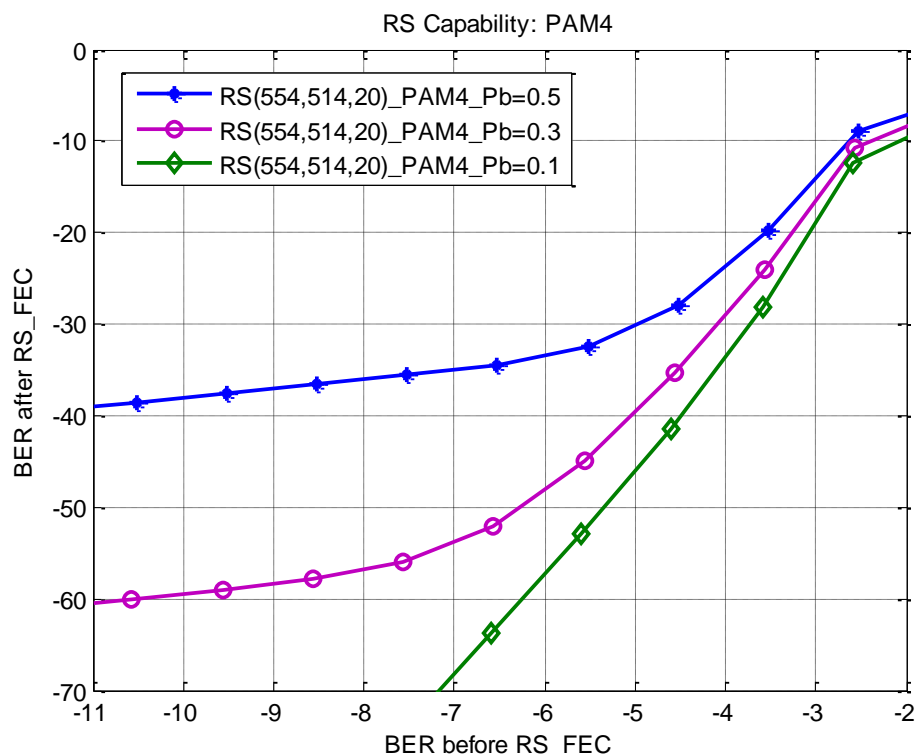
System simulation case study: RS solutions

PAM4 link information：

- 29.877dB, ICN=2mV,

- DFE=[0.5;0.0105591419033788;-0.0838646291817282;-0.0411341054292222;-0.0330967146894018;-0.0126712251463267;-0.00584431523805114;-0.00244702521890698;0.00384402448806175;-0.0240163300157797;-0.00748279553106418;0.0522180947613083]];

Performance comparison for different PAM4 RS solutions:

RS Type	RS(544，514)	RS(528，514)	RS(544，504)
BER	6.0e-6	6.0e-6	1.3350e-39
SER after FEC	1.7073e-29	3.7614e-14	1.3350e-39
BER after FEC	5.0247e-31	5.7090e-16	5.1558e-41

Summary

- Conventional AMI simulation does not take into account FEC functionalities.
- Industry standards on PAM4 requires FEC to achieve basic BER targets (1e-12/15 for example), given same/similar channel insertion loss as NRZ systems.

- FEC gain can be modeled using error propagation theories.
  - Burst error length should be long enough to assure calculation accuracy(≥200 bits for RS(544,514) solution)
  - FEC simulation algorithm should support multi-tap DFE, multi-type RS codes simulation scenarios.

- Concept has been proved for feasibility of PAM4 simulation to integrate FEC functionalities through two case studies.

- From system application's perspective, it is recommended that IBIS-AMI to consider integrating FEC simulation functionality for PAM4.

Thank you