socionext™
for better quality of experience

DDR4 SI/PI Analysis Using IBIS5.0

Socionext Inc.
Yumiko Sugaya

Asian IBIS Summit,
Tokyo, Japan
November 16, 2015

Outline

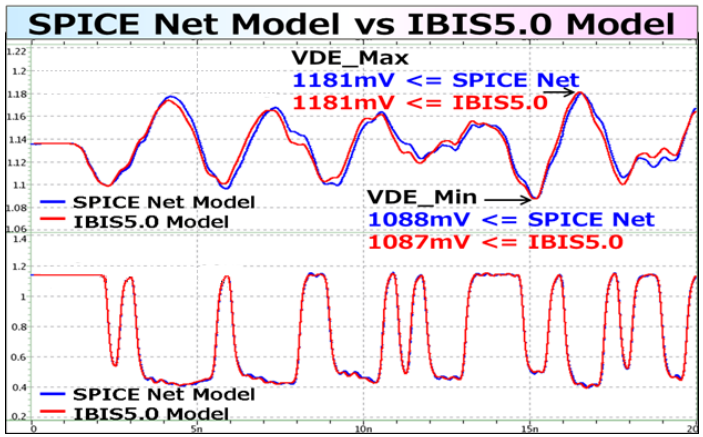
- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

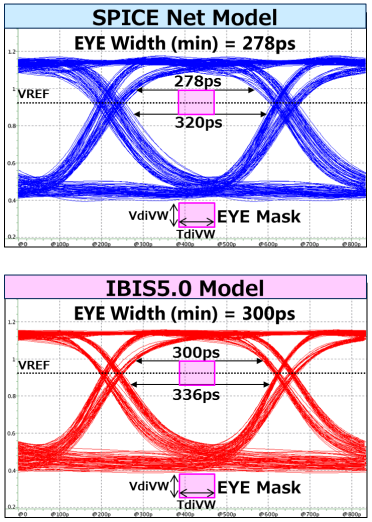
Outline

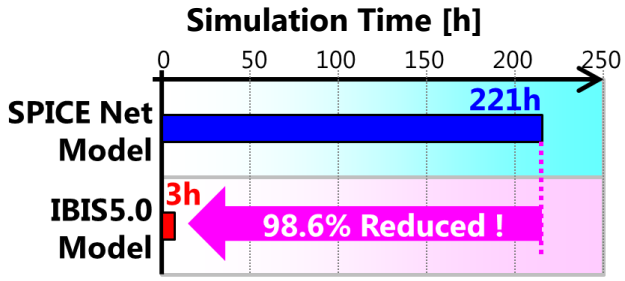
- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

Overview

- Because of the Over Clocking issue, we could not use IBIS5.0 for high speed analysis, such as for DDR4.
- Modification of the EDA software has removed the Over Clocking issue.
  Therefore, the accuracy of IBIS5.0 at high speed has improved.
- **IBIS5.0 can analyze DDR4 SI/PI with high accuracy in a short time!**





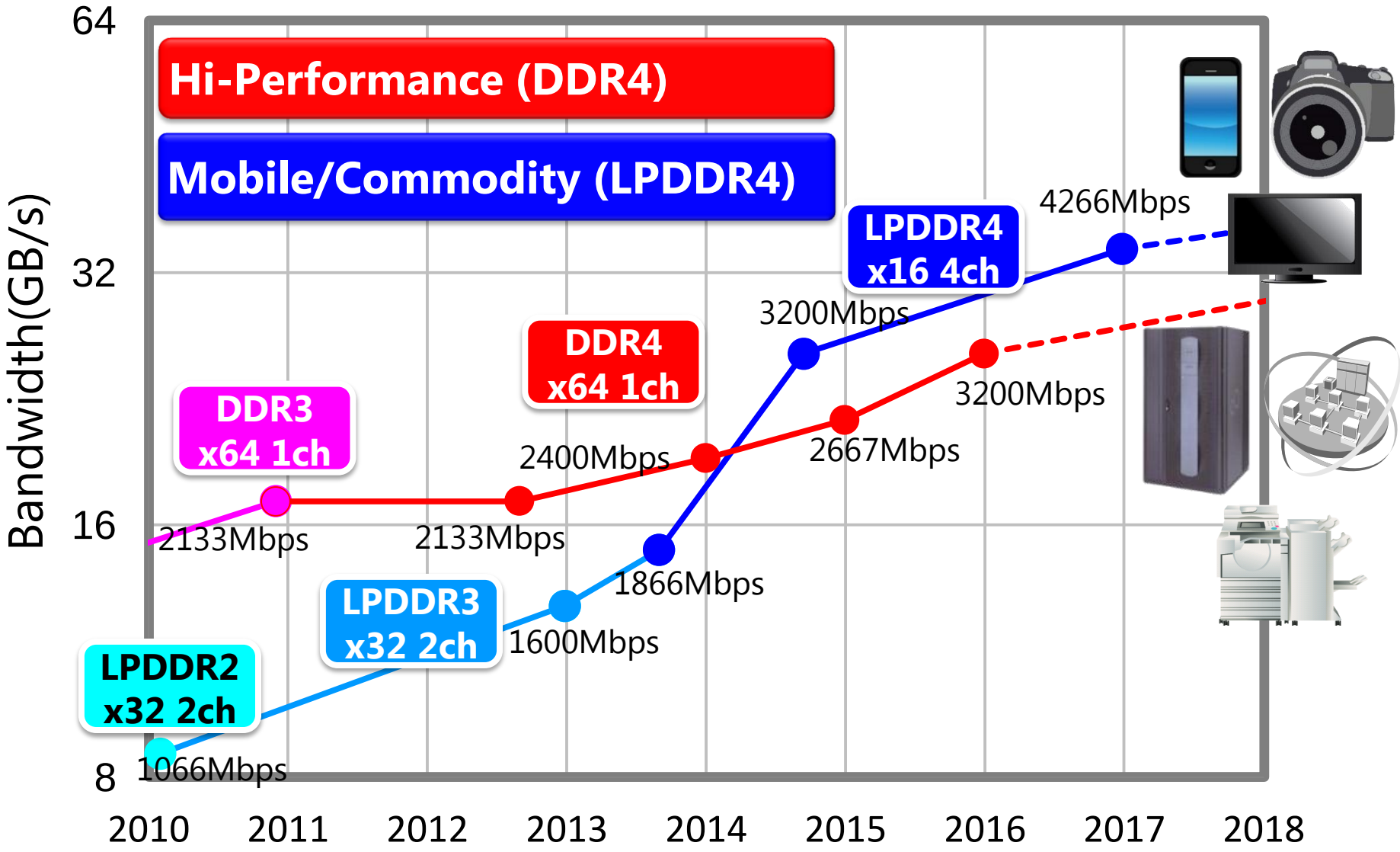


Outline

- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

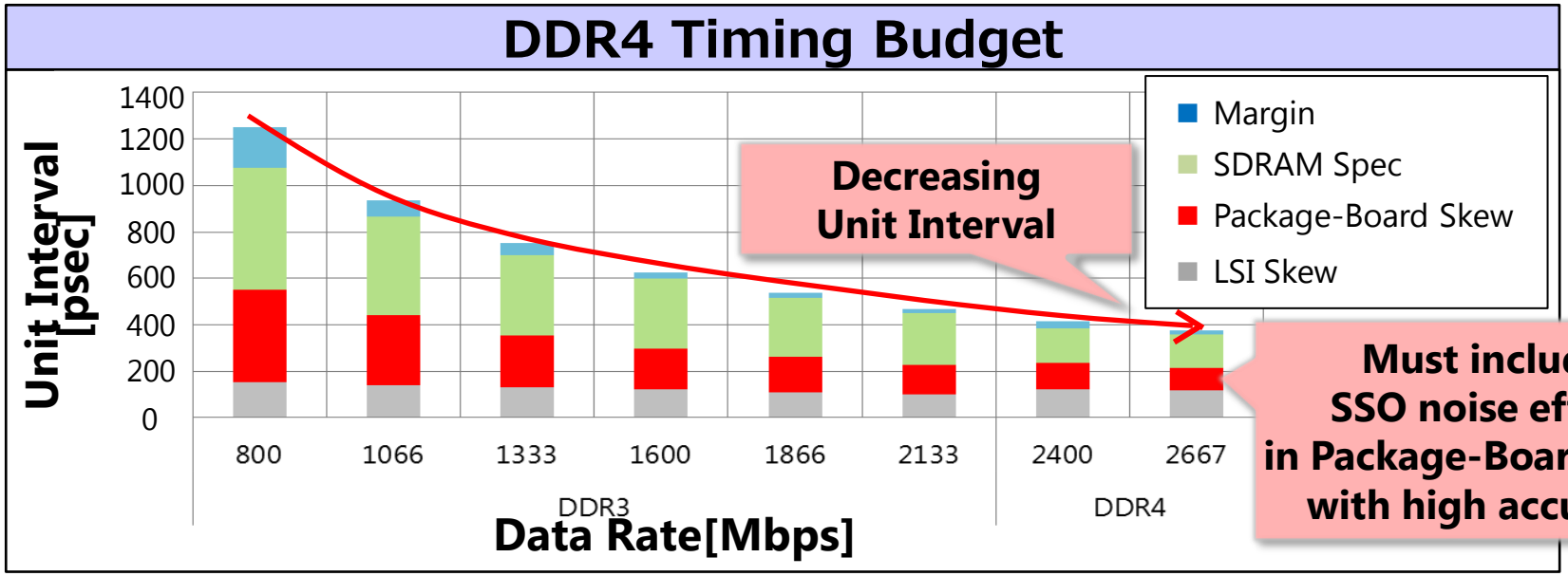
Memory Trend

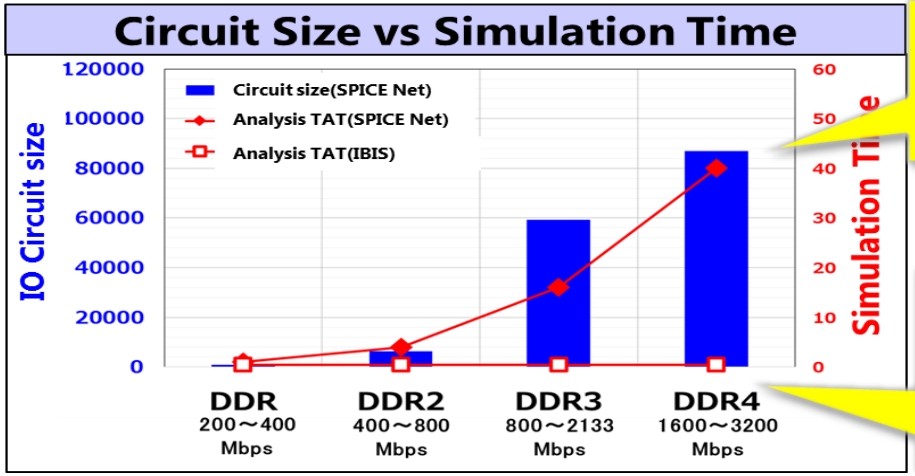
DDR3 is replaced by DDR4.



Necessity of IBIS5.0 for DDR4 simulation

IBIS5.0 can analyze SSO noise with high accuracy in a short time.





SPICE Net:
SSO accuracy :high
Simulation Time: too long

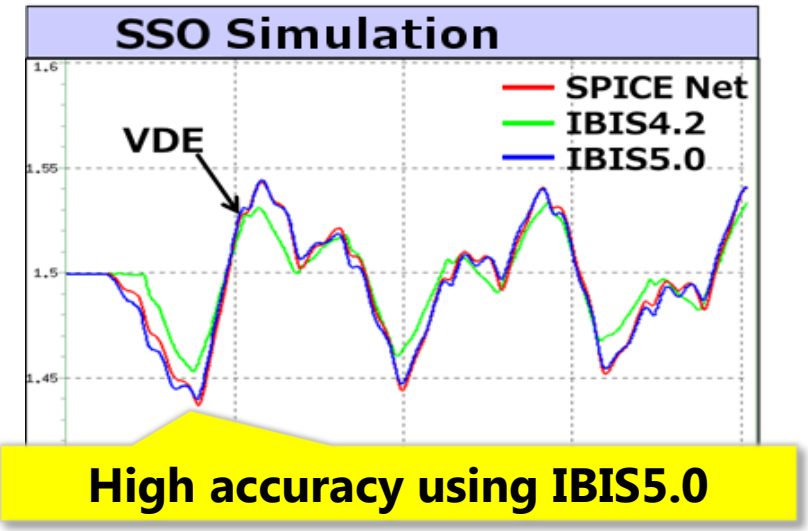
IBIS5.0:
SSO accuracy : high
Simulation Time : short

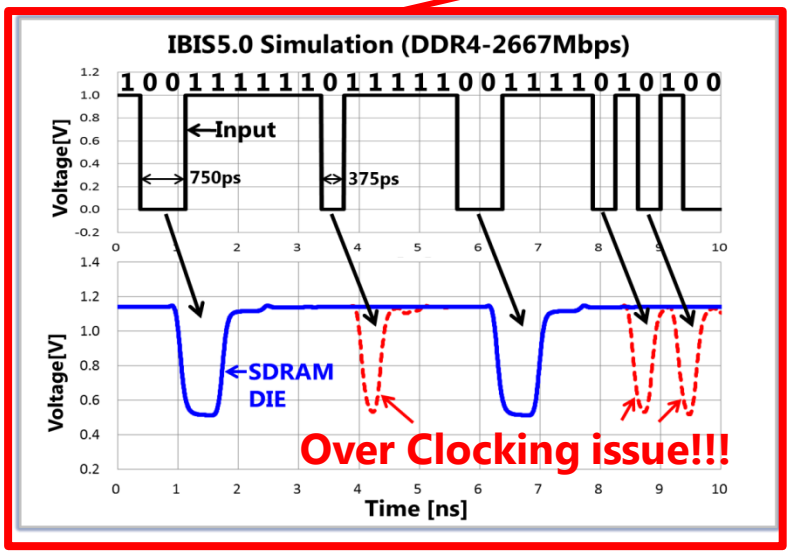
socionext

We solved the Over Clocking issue in cooperate with EDA developer.

- Comparison of the simulation models.

	SPICE Net	IBIS4.2	IBIS5.0
Simulation Time	Longer	Shorter	Shorter
SSO accuracy	High	Low	High
SI accuracy (~1600Mbps)	High	High	High
SI accuracy (1866Mbps~)	High	High	Low



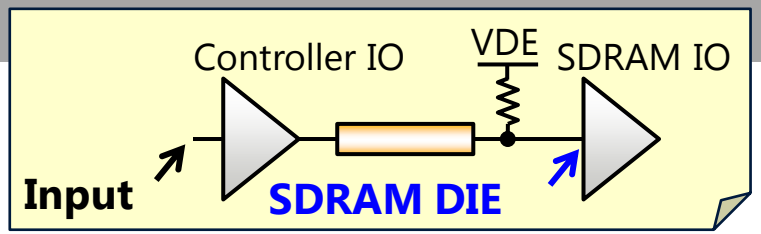


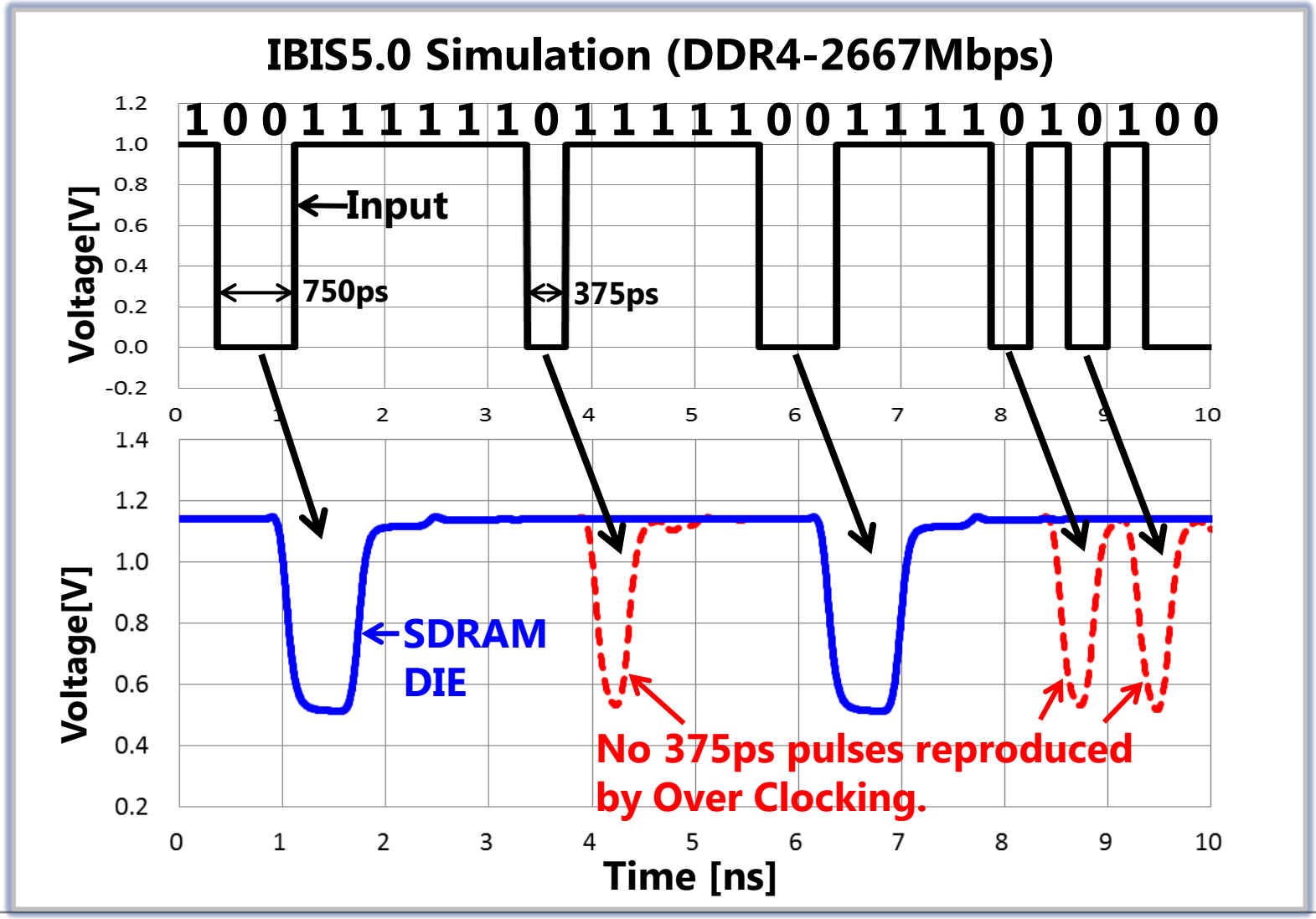
Outline

- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

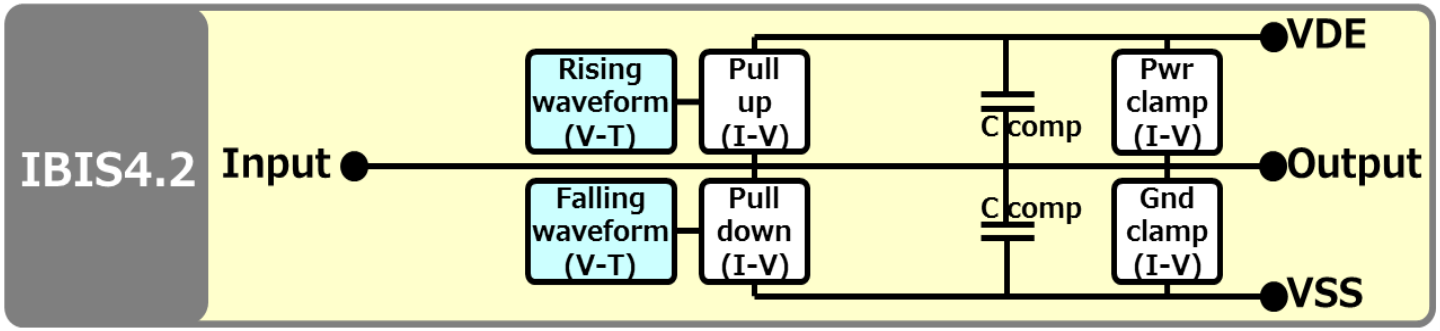
What is the Over Clocking?

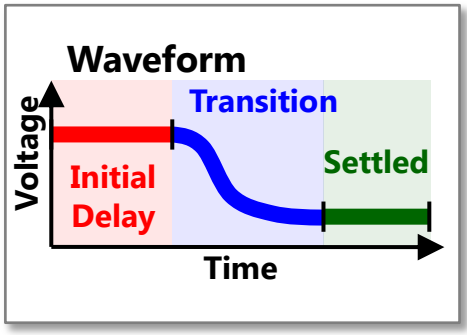
- **Old and new issue (Over Clocking)**



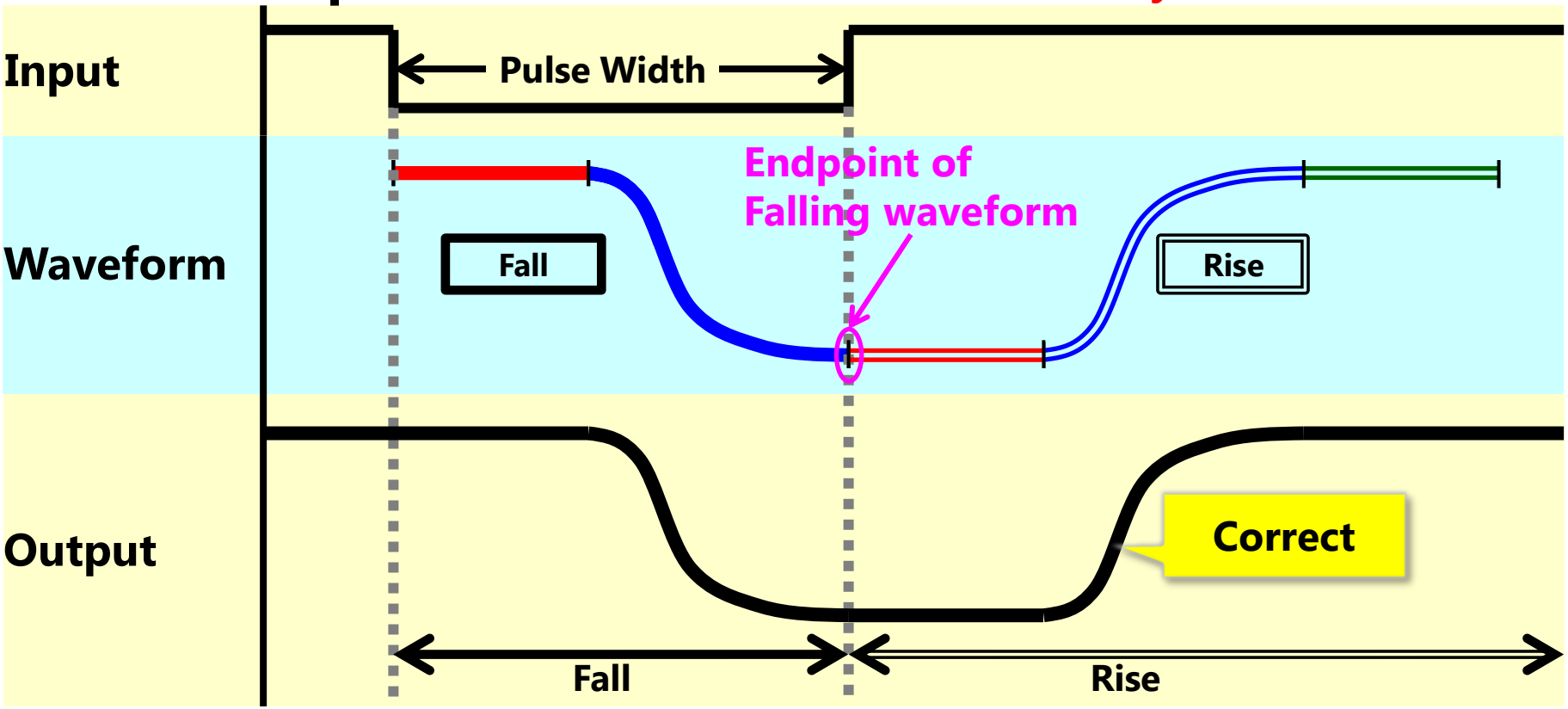


IBIS Over Clocking mechanism(1/4)

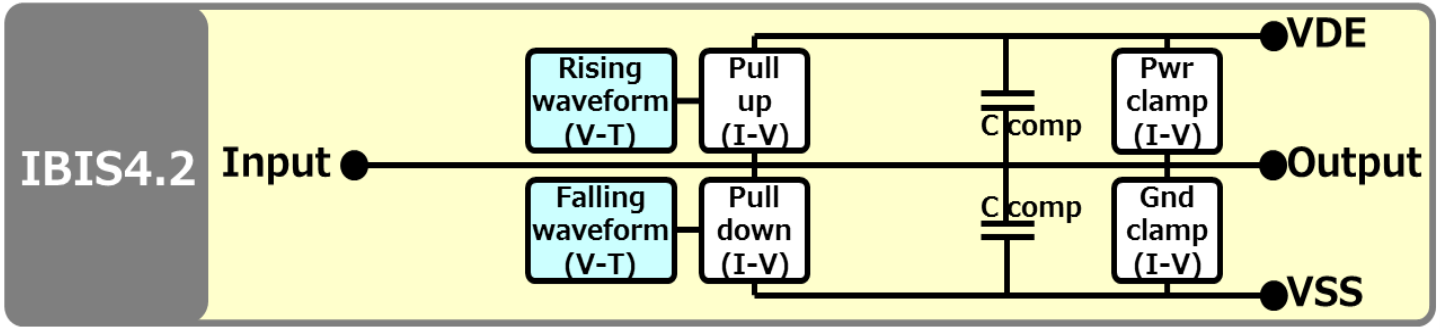


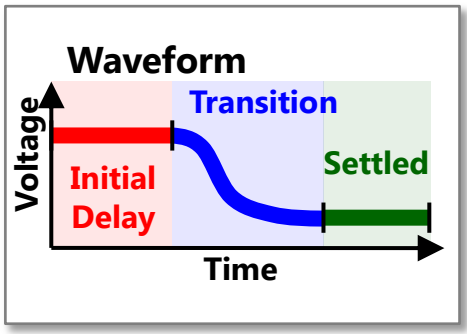


■ IBIS Low Speed Mode Pulse Width ≧ Initial Delay+ Transition Time

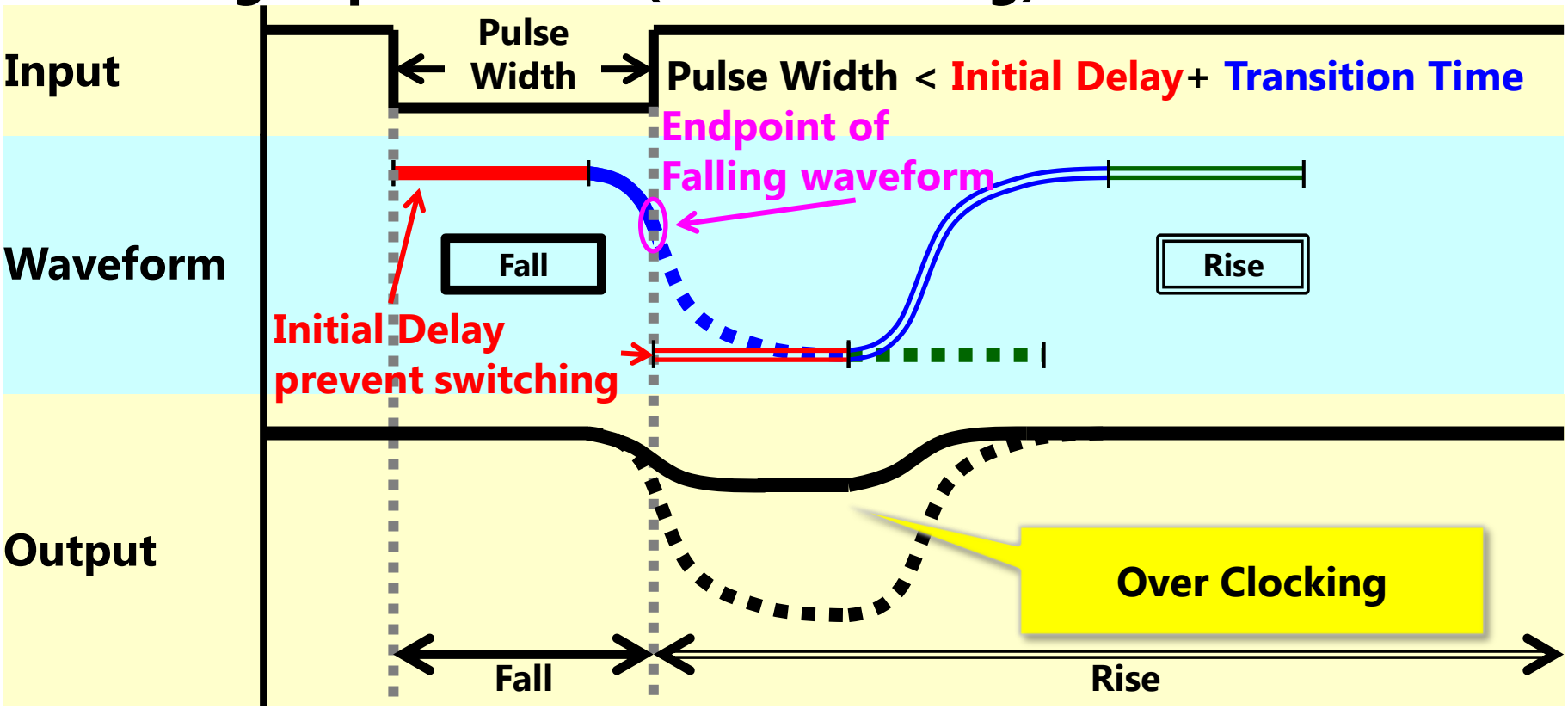


IBIS Over Clocking mechanism(2/4)



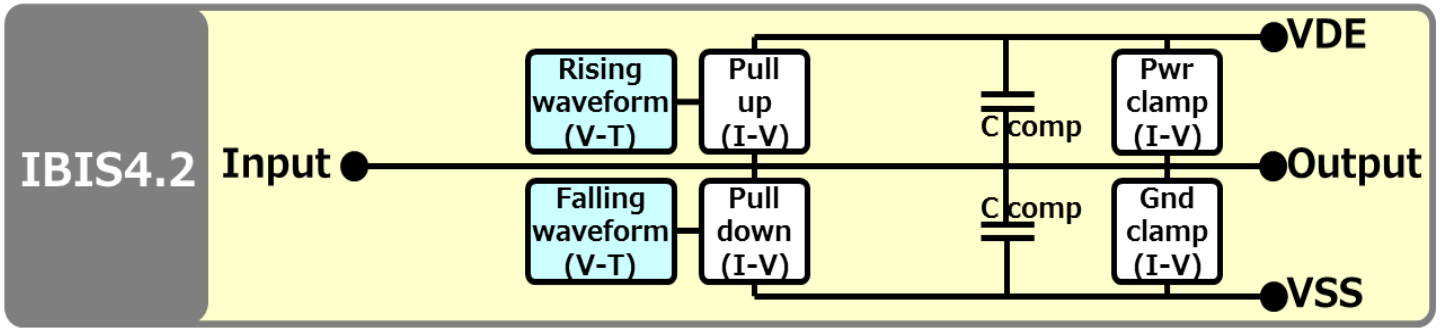


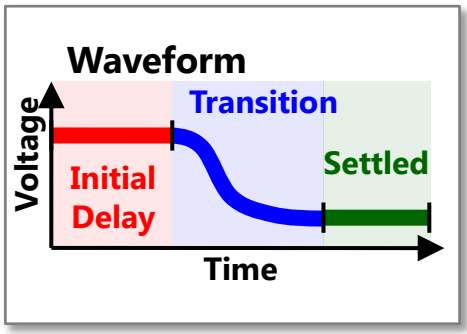
■IBIS High Speed Mode(Over Clocking)



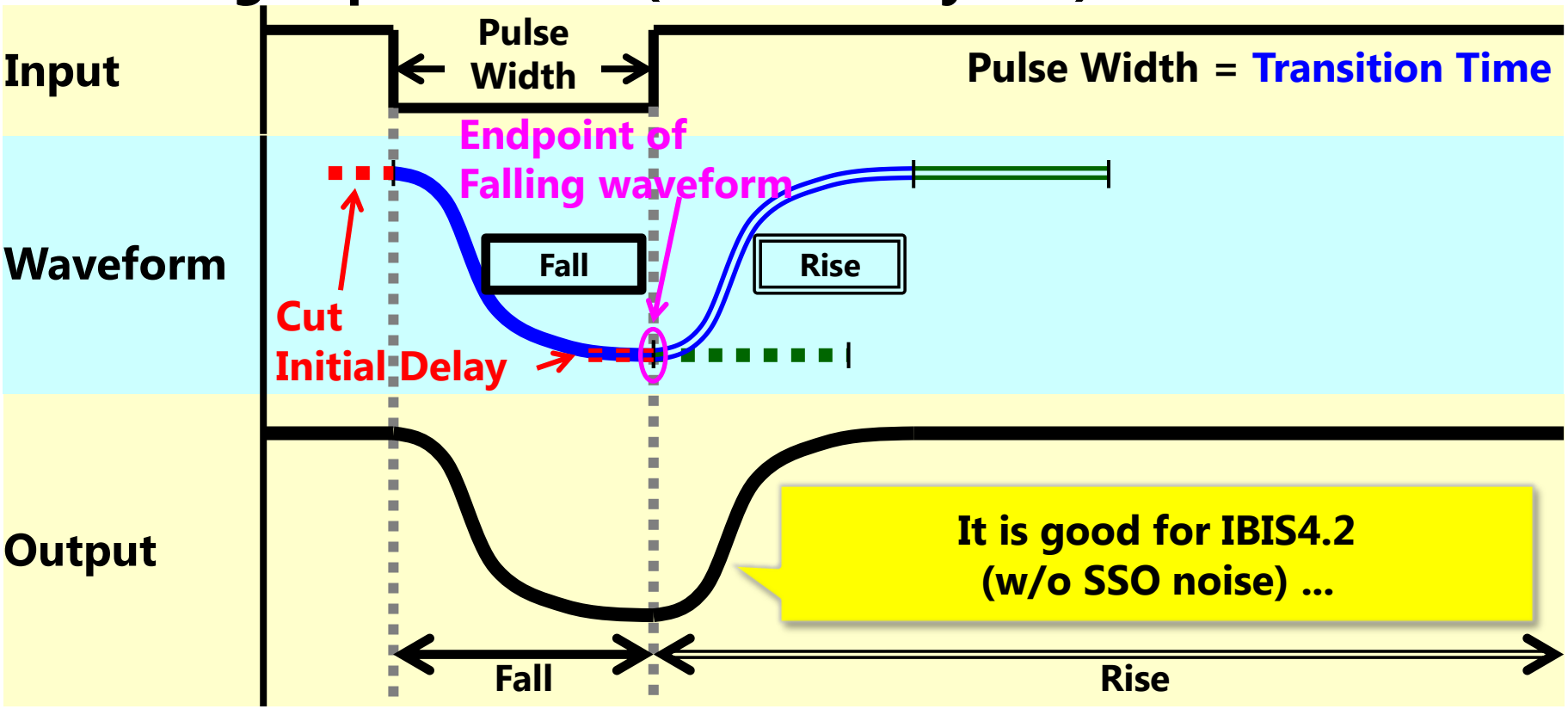
socionext

IBIS Over Clocking mechanism(3/4)

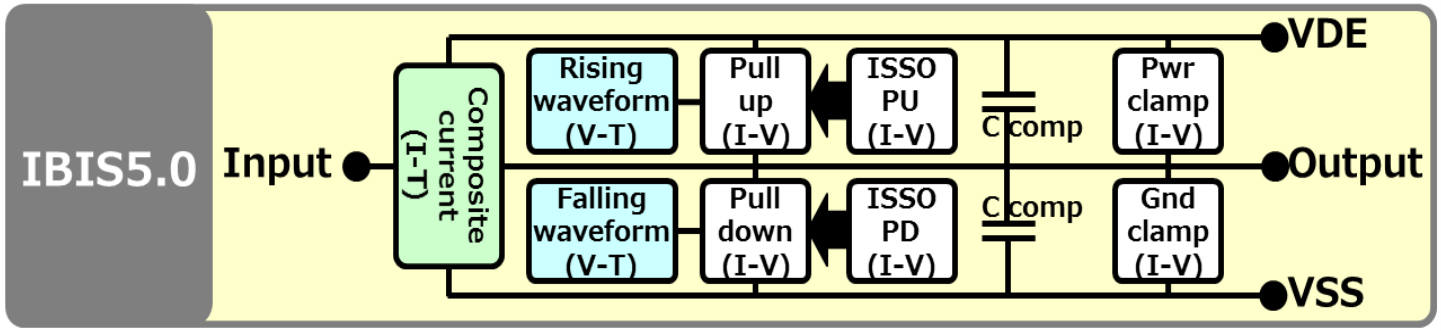


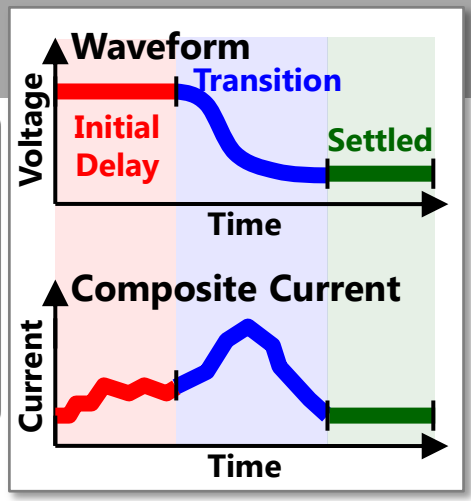


■ IBIS High Speed Mode(Initial Delay Cut)

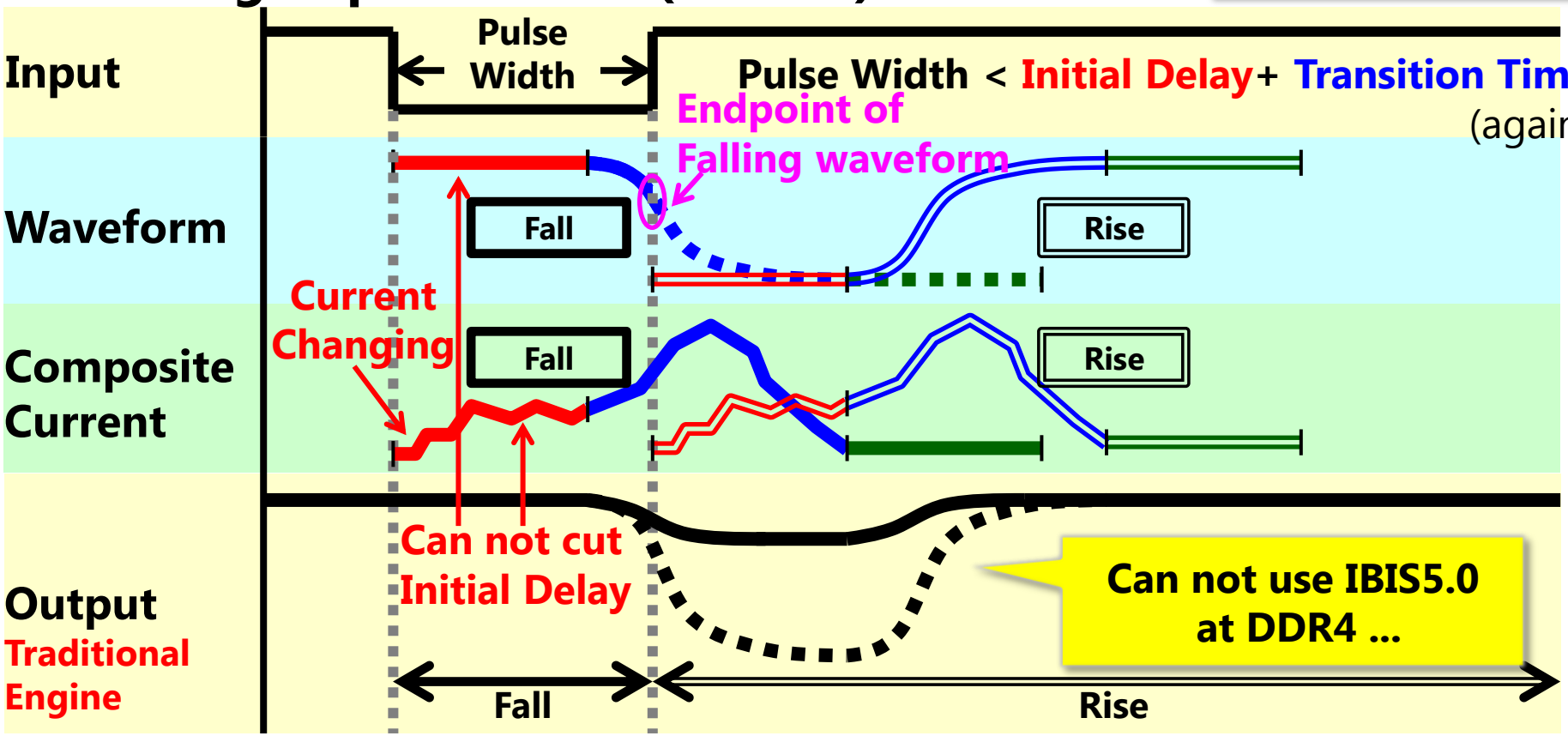


IBIS Over Clocking mechanism(4/4)





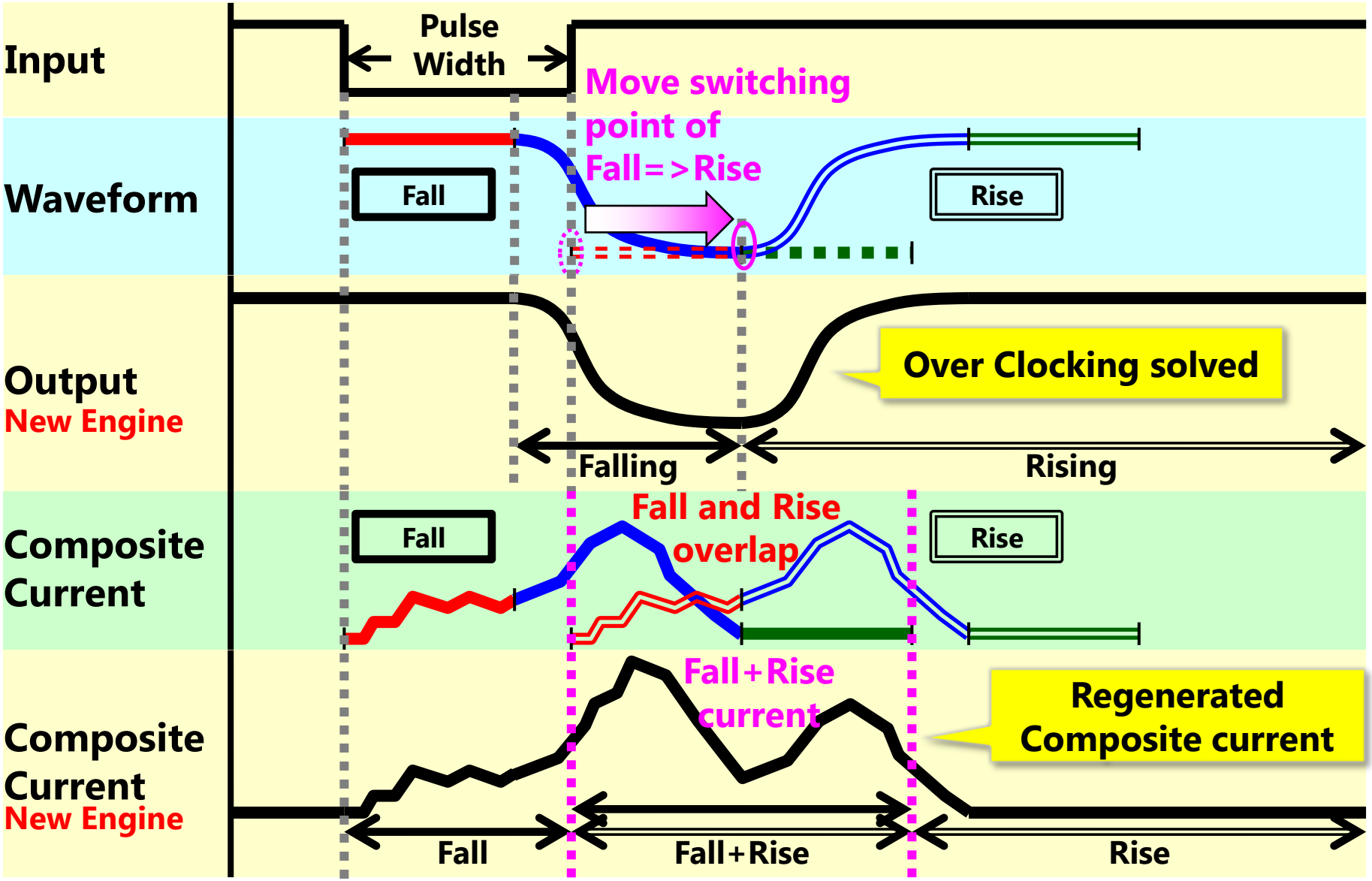
■IBIS High Speed Mode (IBIS5.0)



Over Clocking modified in the EDA Software

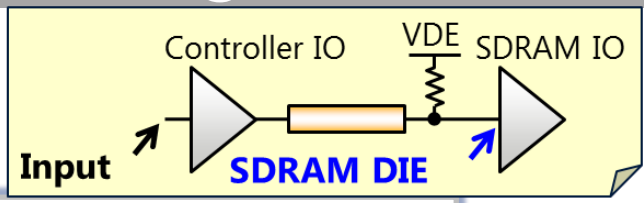
■ **IBIS High Speed Mode (IBIS5.0)**

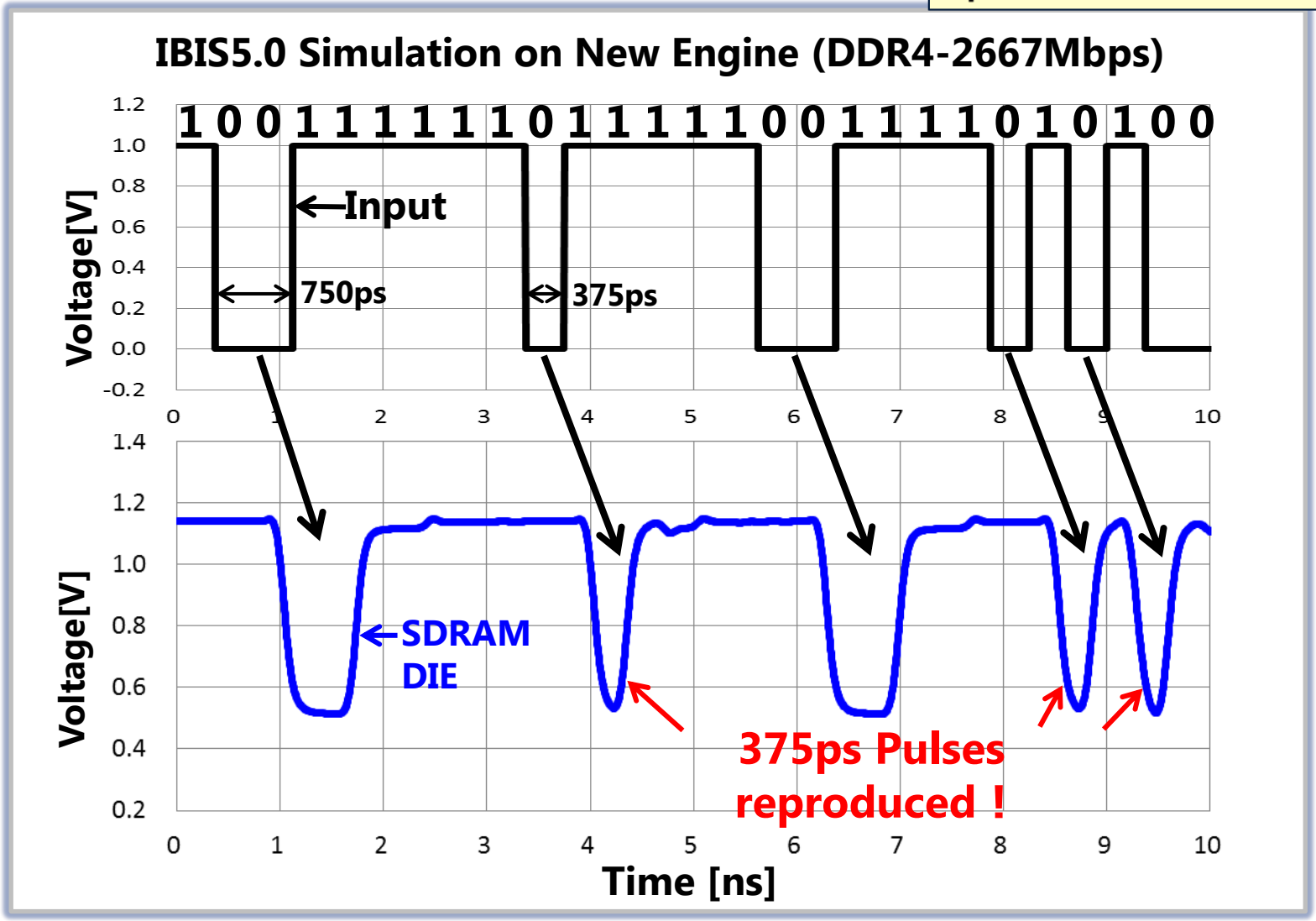
Pulse Width = Transition Time



New Engine Simulation Result (Over Clocking solved)

- Over Clocking issue of IBIS5.0 is solved!!



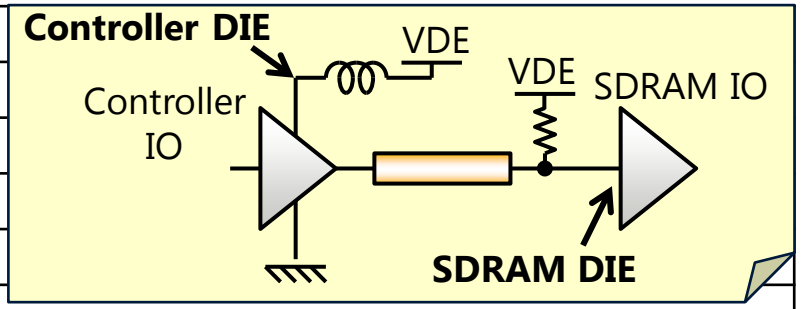


Outline

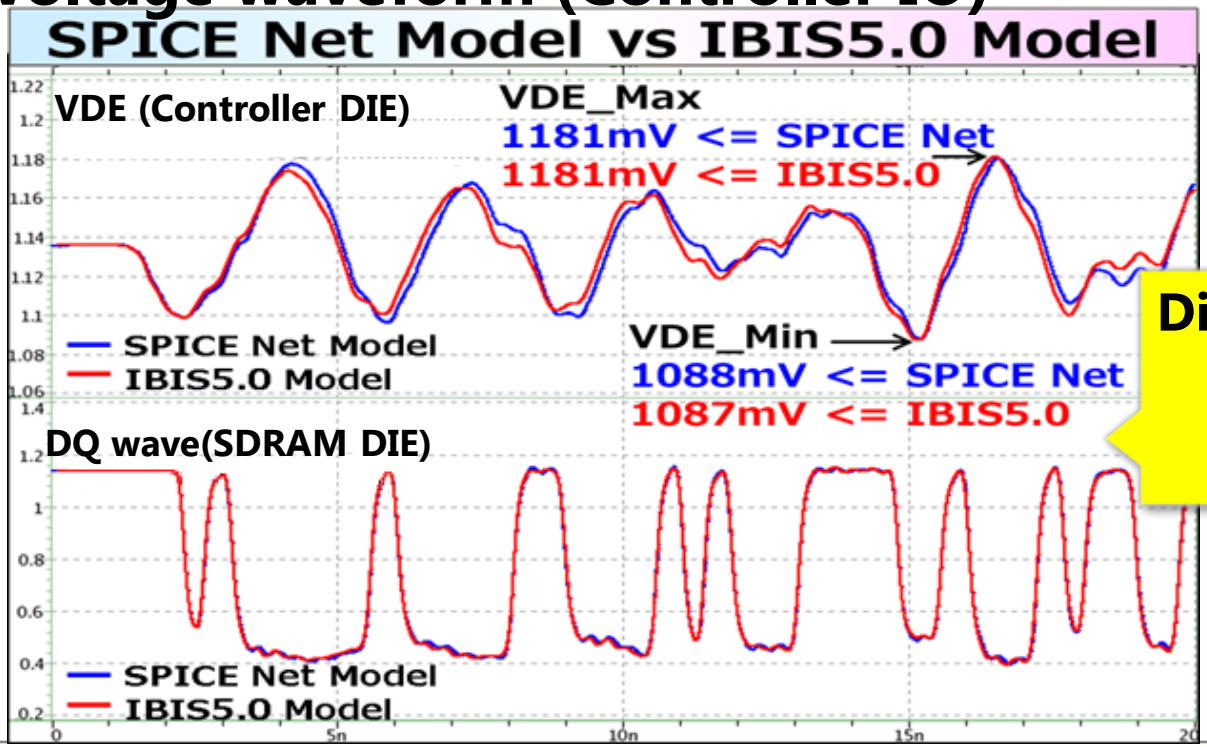
- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

Waveform of the SSO noise : Very Good !!

Stimulus	CK	Toggle	
	A/C, CNTL	PRBS7	
	DQ	Victim	PRBS7
		Aggressor	PRBS7
	DQS	Victim	Toggle
		Aggressor	PRBS7



VDE Voltage waveform (Controller IO)



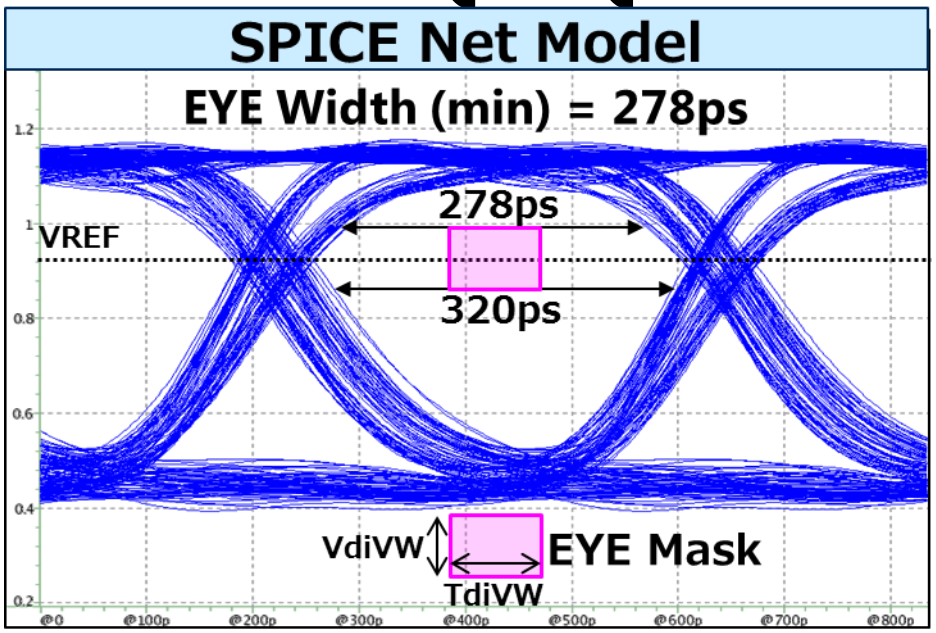
Difference in peaks is less than 1mV!!

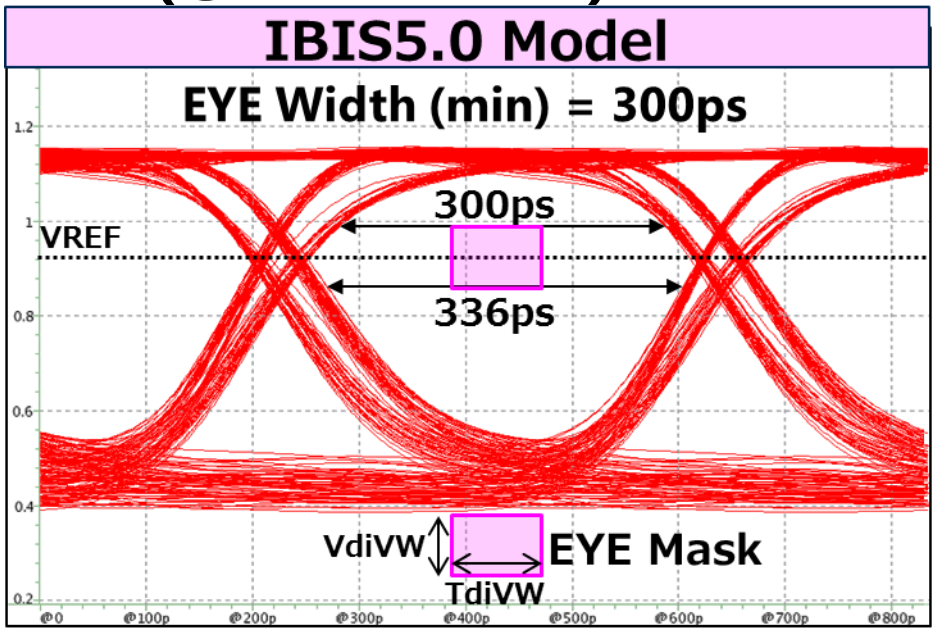
socionext

Width of the EYE : Seems Good
(see "Expectation for future IBIS")

Stimulus	CK	Toggle	
	A/C, CNTL	PRBS7	
	DQ	Victim	PRBS7
		Aggressor	PRBS7 (Even/Odd 2pattern)
	DQS	Victim	Toggle
		Aggressor	Toggle

- **DDR4 TX DQS-DQ EYE Waveform (@SDRAM DIE)**



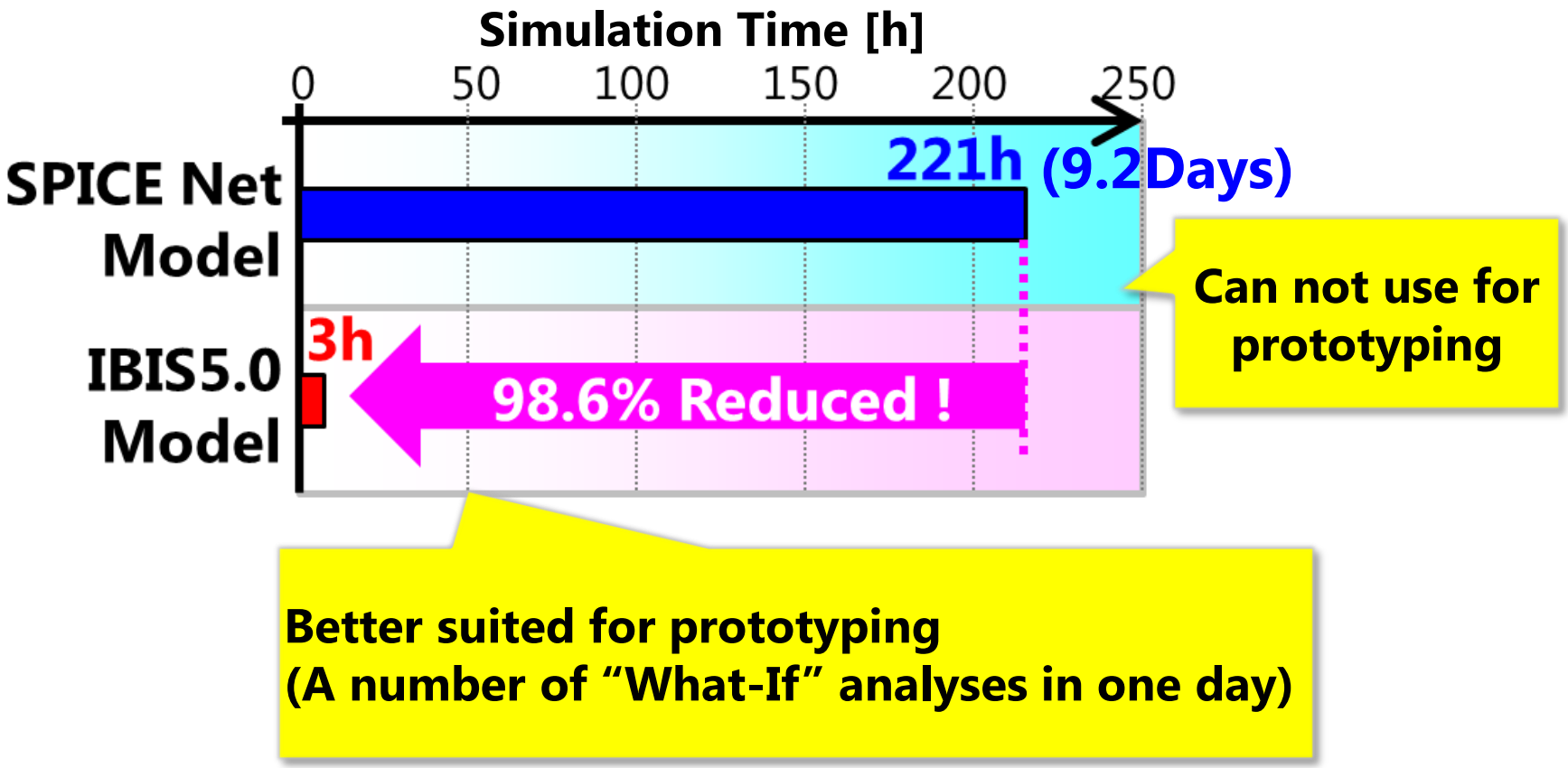


socionext

DDR4 SI/PI Analysis Using IBIS5.0(3/3)

Simulation Time : Excellent !!!

- Transition Analysis Time:60ns(one cycle of PRBS7)

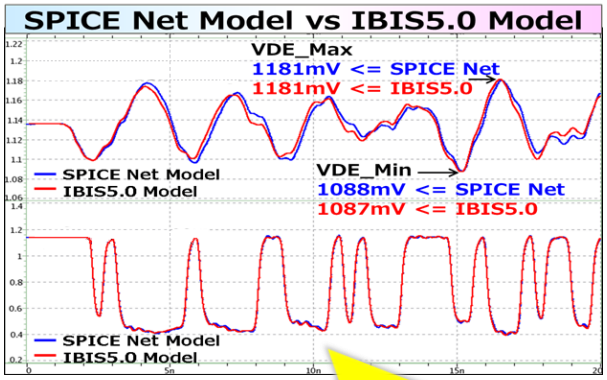


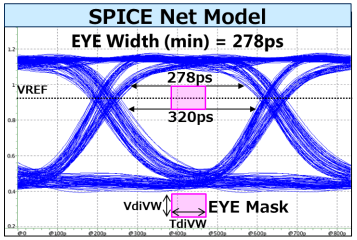
Outline

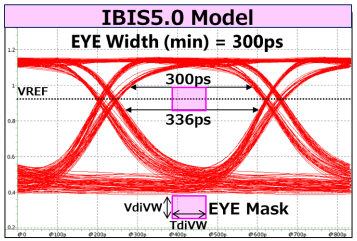
- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

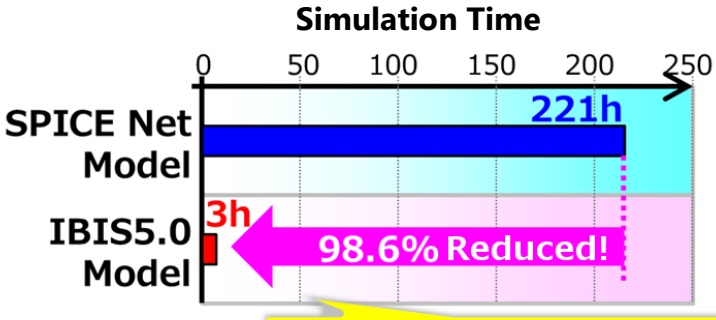
Summary

- Because of the Over Clocking issue, we could not use IBIS5.0 for high speed analysis, such as for DDR4.
- Modification of the EDA software has removed the Over Clocking issue.
  Therefore, the accuracy of IBIS5.0 at high speed has improved.
- **IBIS5.0 can analyze DDR4 SI/PI with high accuracy in a short time!**









IBIS5.0 result: High accuracy

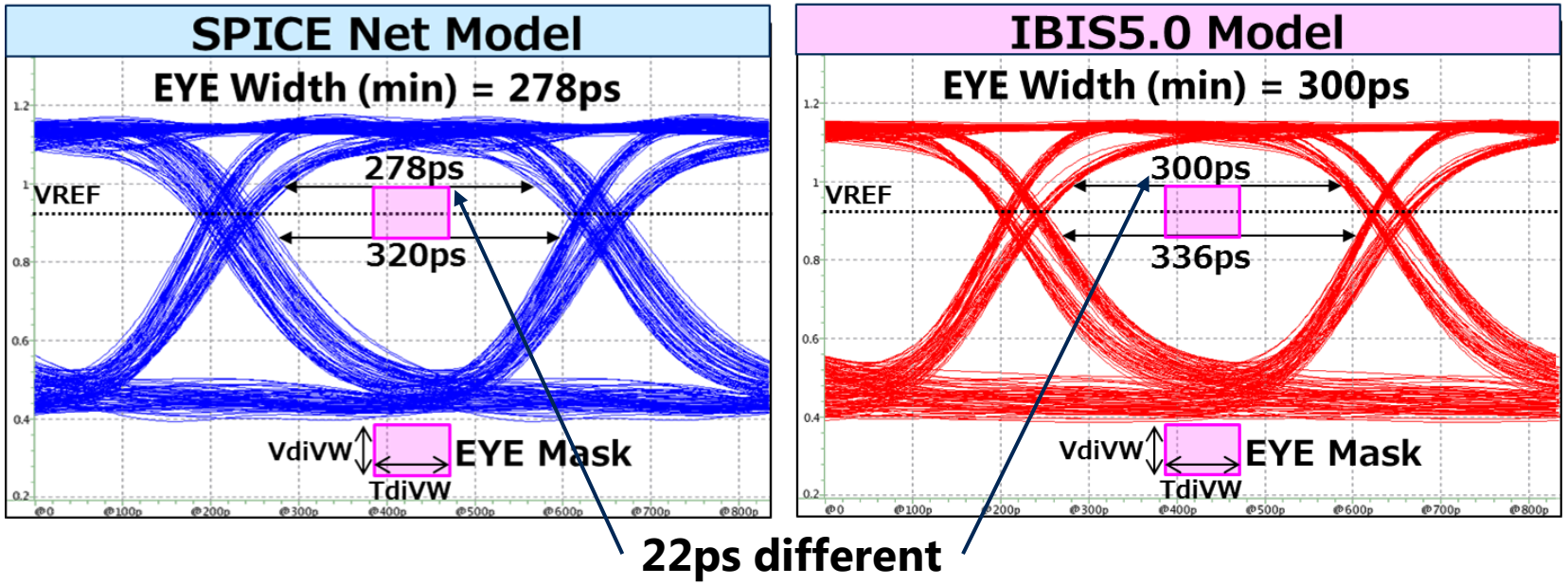
Short simulation time

Outline

- Overview
- DDR4 SI/PI Analysis Issue
- Over Clocking issue
- DDR4 SI/PI Analysis Using IBIS5.0
- Summary
- Expectation for future IBIS

Remaining issue on IBIS5.0

- IBIS5.0 does not show IO Delay Penalty accurately
  - ✓ IBIS5.0 modeling only final-buffer, pre-buffer Delay Penalty can not be considered.



For further simulation accuracy and capability, support of the pre-buffer delay penalty is strongly desired.

socionext

socionext™

for better quality of experience