Board design and IBIS simulation in consideration of the delay control

Asian IBIS Summit

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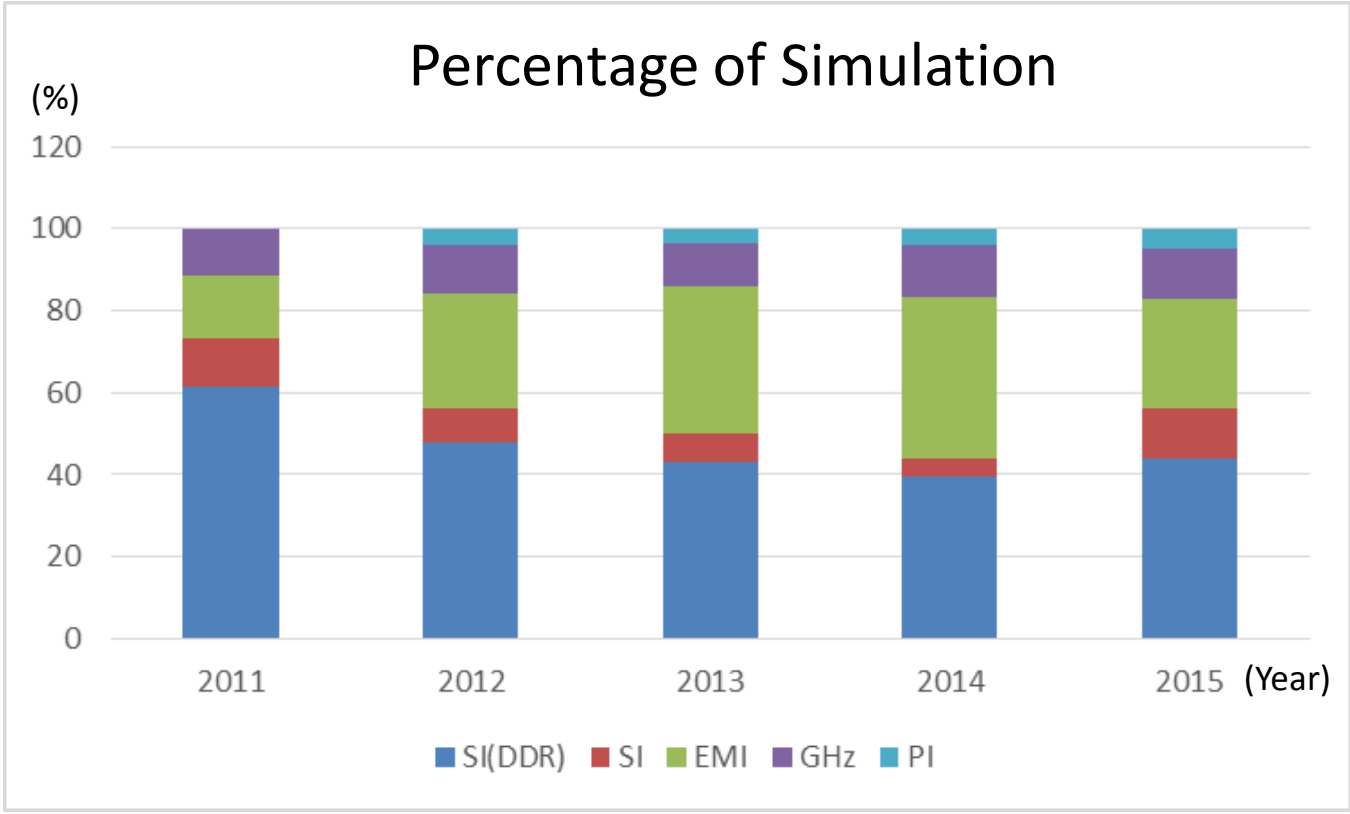
Agenda

- Results of the simulation
- Delay only of wiring
- Calculation delay in PKG
- The design which considered package delay
- Problem and future's request

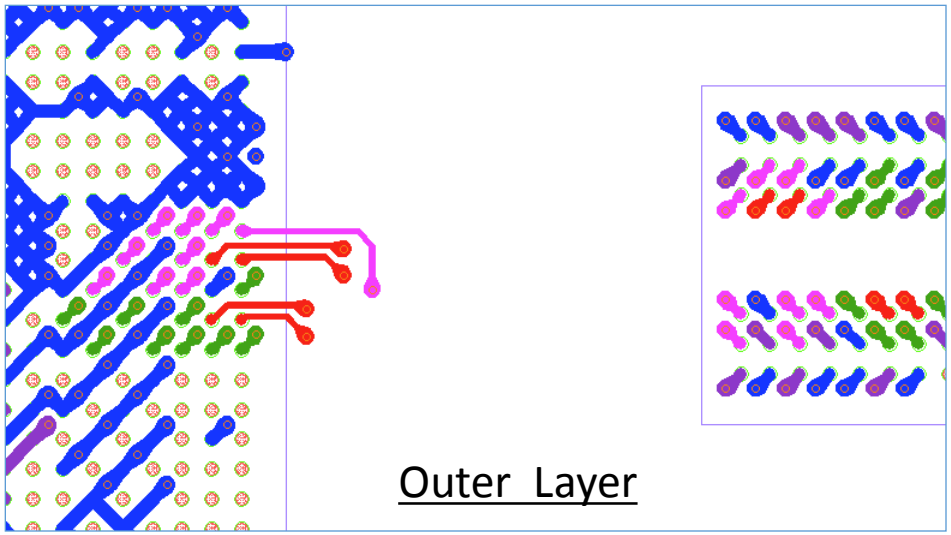
Results of the simulation



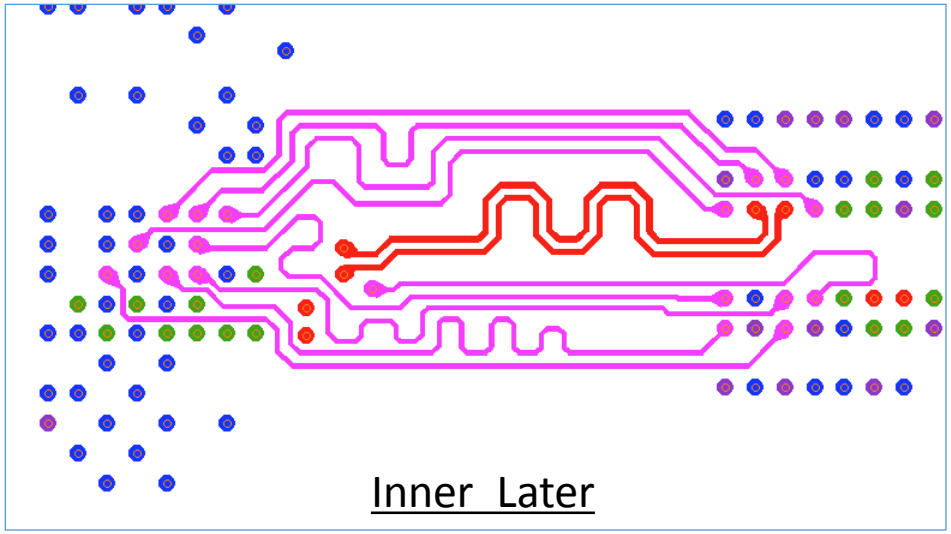
before 2013 results is Include 'IBITECH'.

The ratio of SI analysis including the High-Speed memory accounts for around 50% every year.

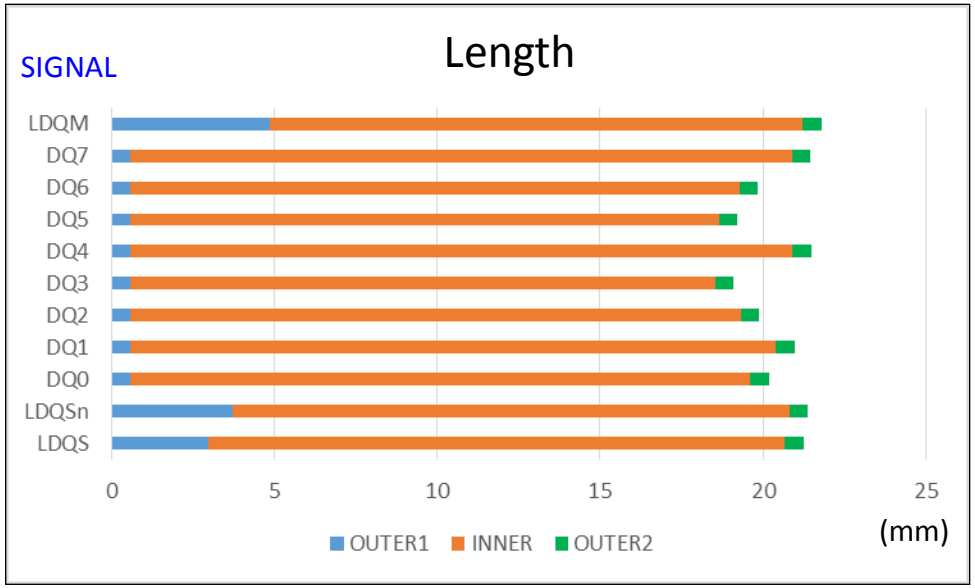
PCB design example for DDR3 interface

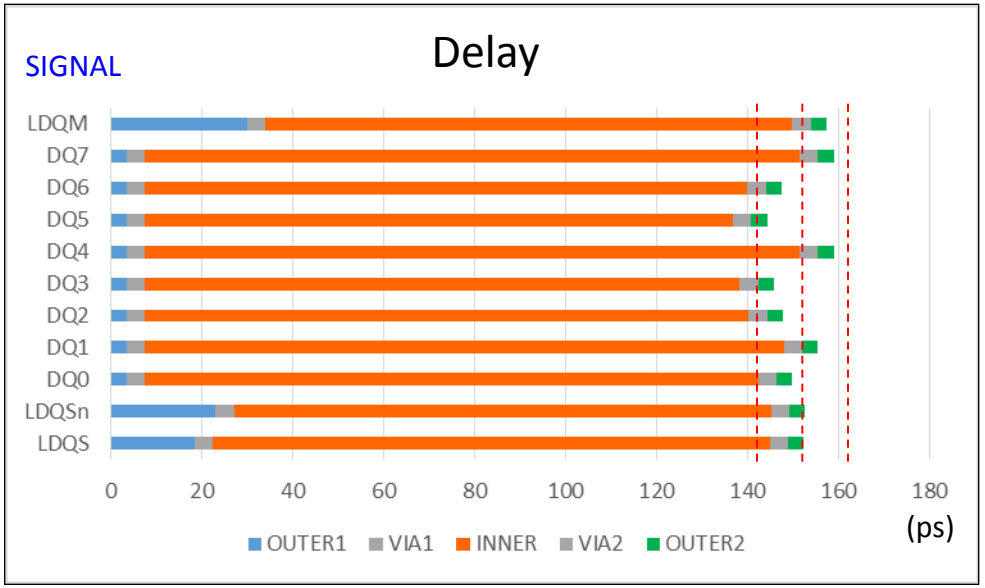


SPEC : ±10ps against for DQS.



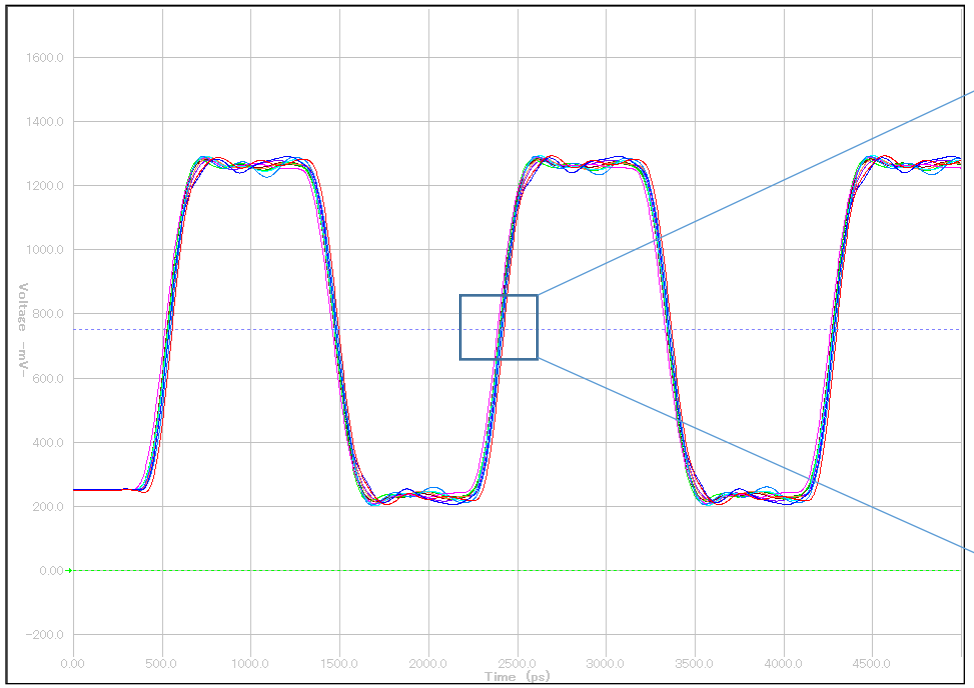
Skew adjustment control on PCB

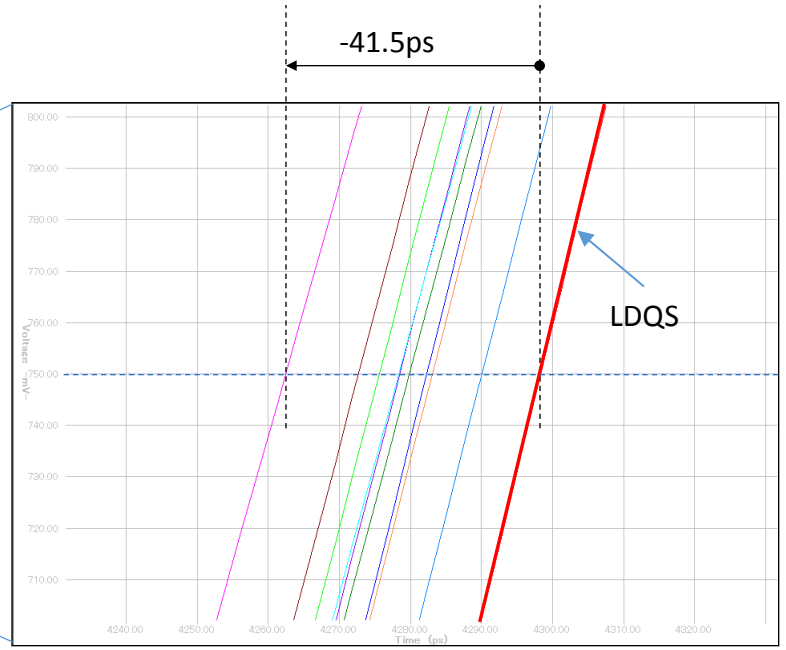




SPEC : ±10ps against for DQS.
Calculation : -7.6ps to 8ps for DQS.

Simulation waveform at receiver node





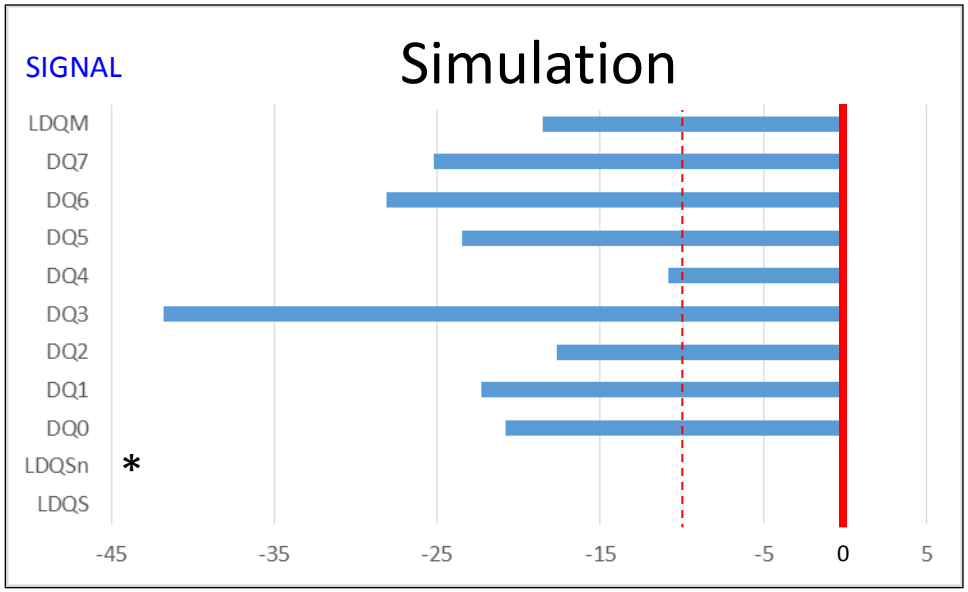
*LDQSn excludes

SPEC : ±10ps against for DQS
Calculation : -7.6ps to 8ps
Simulation: -41.5ps to -12.6ps

Fail

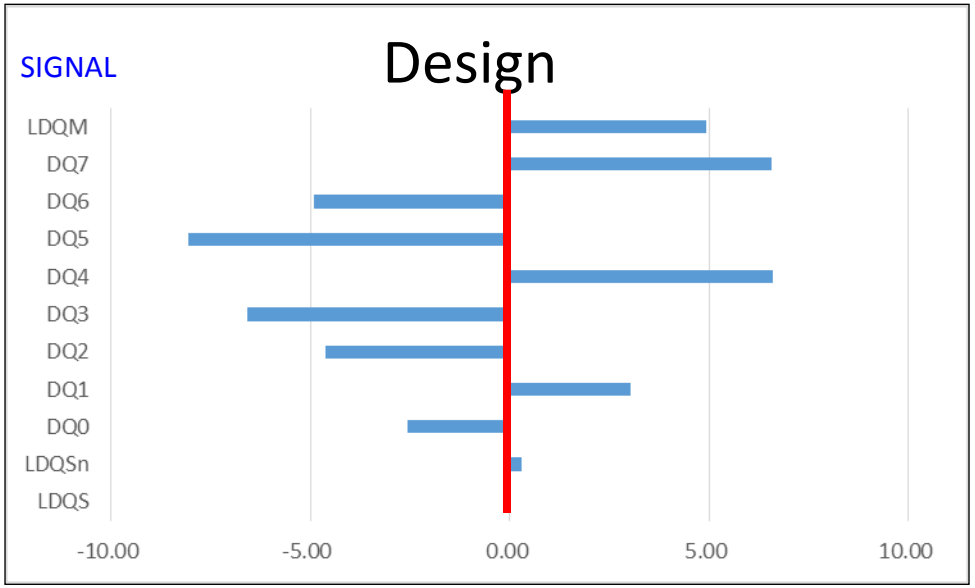
Skew adjustment analysis including PKG

+ : Progress , - : Delay



*LDQSn excludes

(ps)



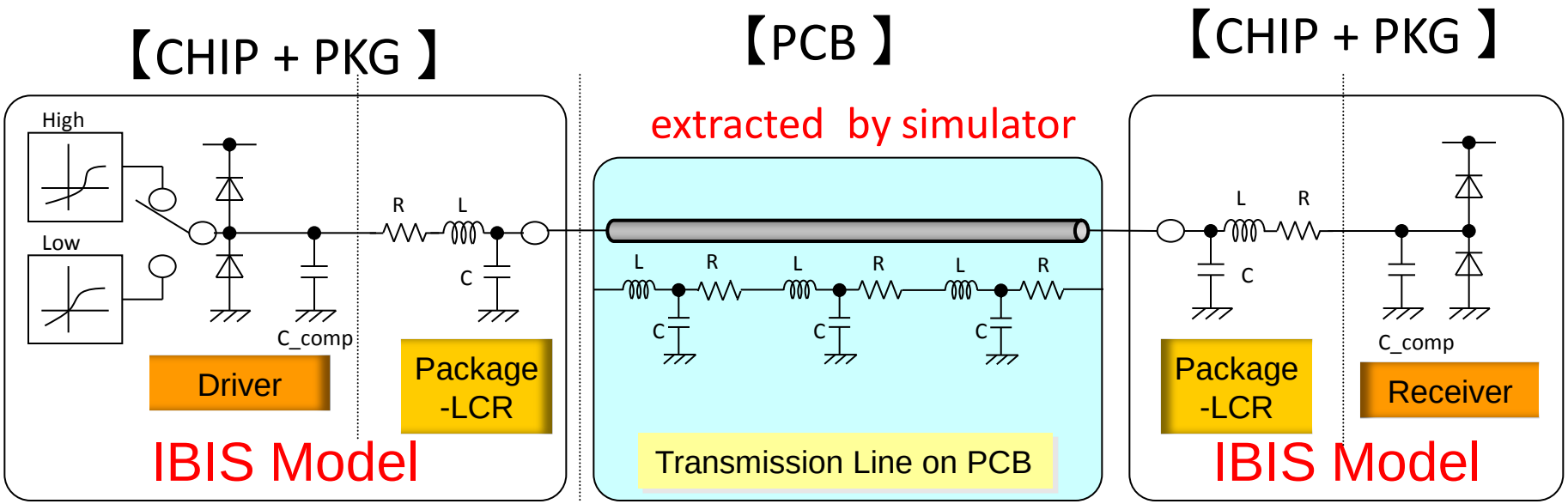
(ps)

Different

- What is a Factor ?

Whole transmission line model of H-S signal

IBIS model includes die capacitance and package-RLC parameters.



Delay in the PKG section compare to PCB ?

- Big or small ?
- Skew adjustment applies for PKG signals ?

Calculation delay in PKG from IBIS

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
AU27	DDR_DQS0	DQS	497.40m	6.62nH	2.69pF
AT27	XDDR_DQS0	DQSN	505.69m	6.22nH	2.63pF
AP28	DDR_DQ0	DQ	892.42m	5.68nH	1.80pF
AT28	DDR_DQ1	DQ	964.77m	6.42nH	1.93pF
AR28	DDR_DQ2	DQ	935.77m	6.14nH	1.89pF
AN27	DDR_DQ3	DQ	781.75m	5.16nH	1.67pF
AP26	DDR_DQ4	DQ	798.77m	5.32nH	1.74pF
AR27	DDR_DQ5	DQ	924.82m	6.04nH	1.86pF

[Model Data]
[Inductance Matrix]
Sparse_matrix

[Row]	AU27
AU27	6.62nH
AU25	390.56pH

[Capacitance Matrix]
Sparse_matrix

[Row]	AU27
AU27	2.69pF
AU25	-7.44fF

Delay

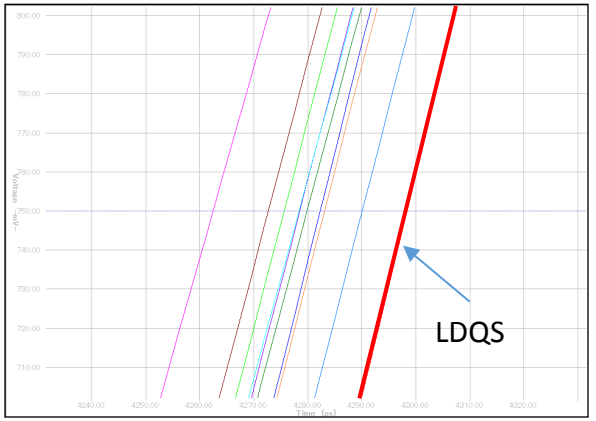
$$T_d = \sqrt{L \bullet C}$$

PKG delay calculation of Controller & Memory

	Controller			Memory				Total	Difference with
Signal	L(nH)	C(pF)	delay(ps)	L(nH)	C(pF)		delay(ps)	delay(ps)	LDQS
LDQS	6.62	2.69	133.45	1.35	0.31	0.00	20.58	154.02	0.00
LDQSn	6.22	2.63	127.90	1.61	0.34	0.00	23.29	151.19	-2.84
DQ0	5.68	1.80	101.11	1.70	0.37	0.00	25.02	126.14	-27.89
DQ1	6.42	1.93	111.31	1.24	0.32	0.00	19.76	131.08	-22.95
DQ2	6.14	1.89	107.72	1.85	0.41	0.00	27.70	135.42	-18.60
DQ3	5.16	1.67	92.83	1.55	0.35	0.00	23.12	115.95	-38.08
DQ4	5.32	1.74	96.21	1.88	0.44	0.00	28.83	125.05	-28.98
DQ5	6.04	1.86	105.99	1.73	0.35	0.00	24.63	130.63	-23.40
DQ6	5.97	1.89	106.22	1.38	0.32	0.00	21.06	127.29	-26.74
DQ7	4.78	1.64	88.54	1.61	0.38	0.00	24.78	113.32	-40.70
LDM	6.95	2.03	118.78	1.38	0.30	0.00	20.33	139.11	-14.92

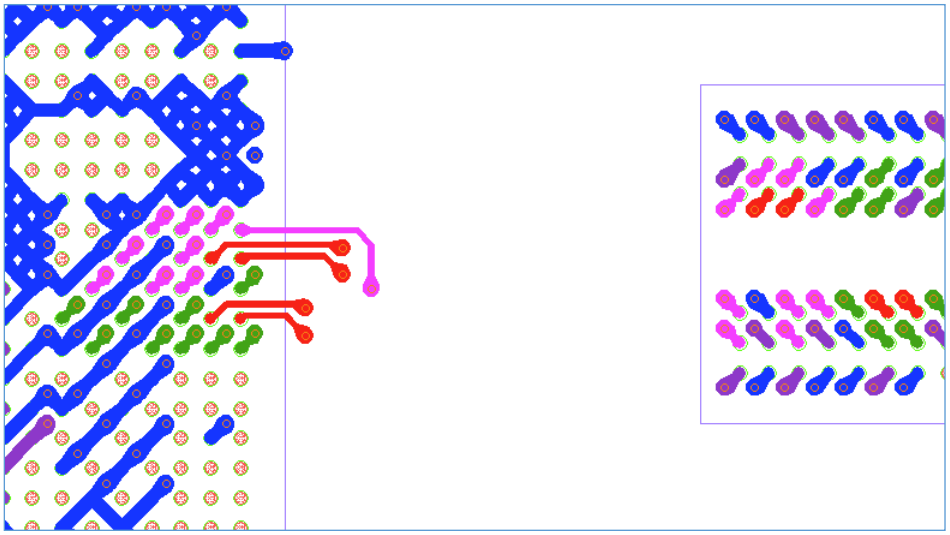
Delay of controller PKG is more than 100ps.

Delay LDQS signal is the biggest.

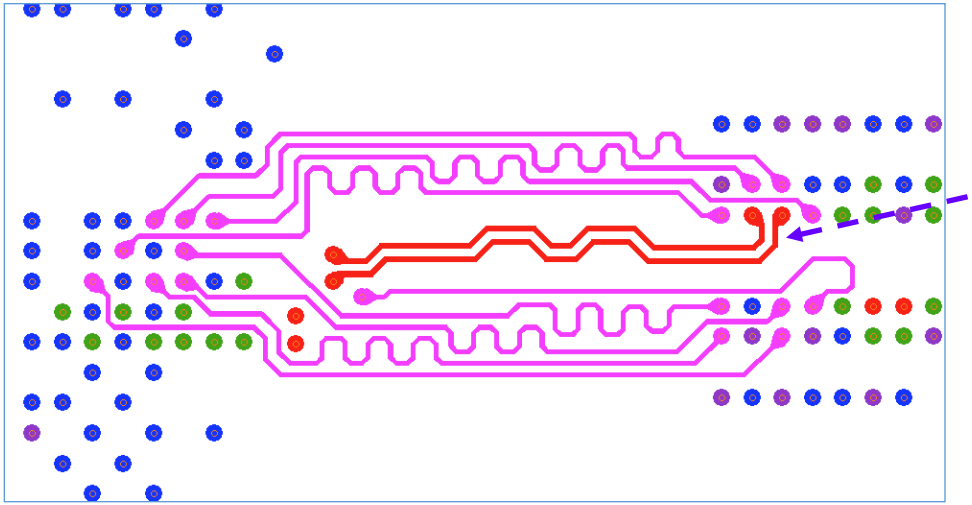


PCB design considering in skew ajustment

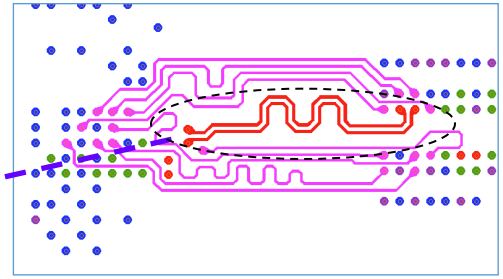
Outer Layer



Inner Layer

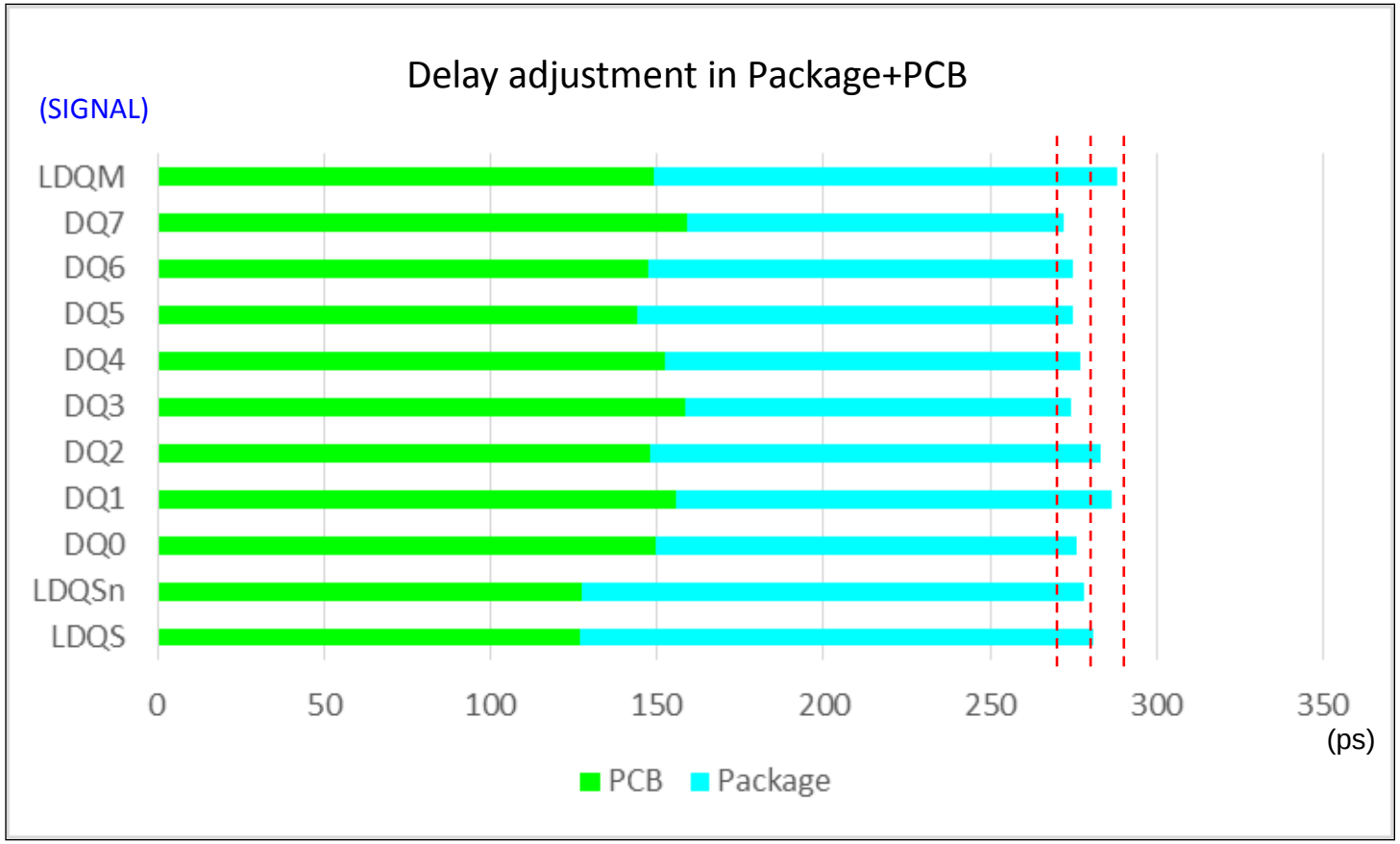


Before

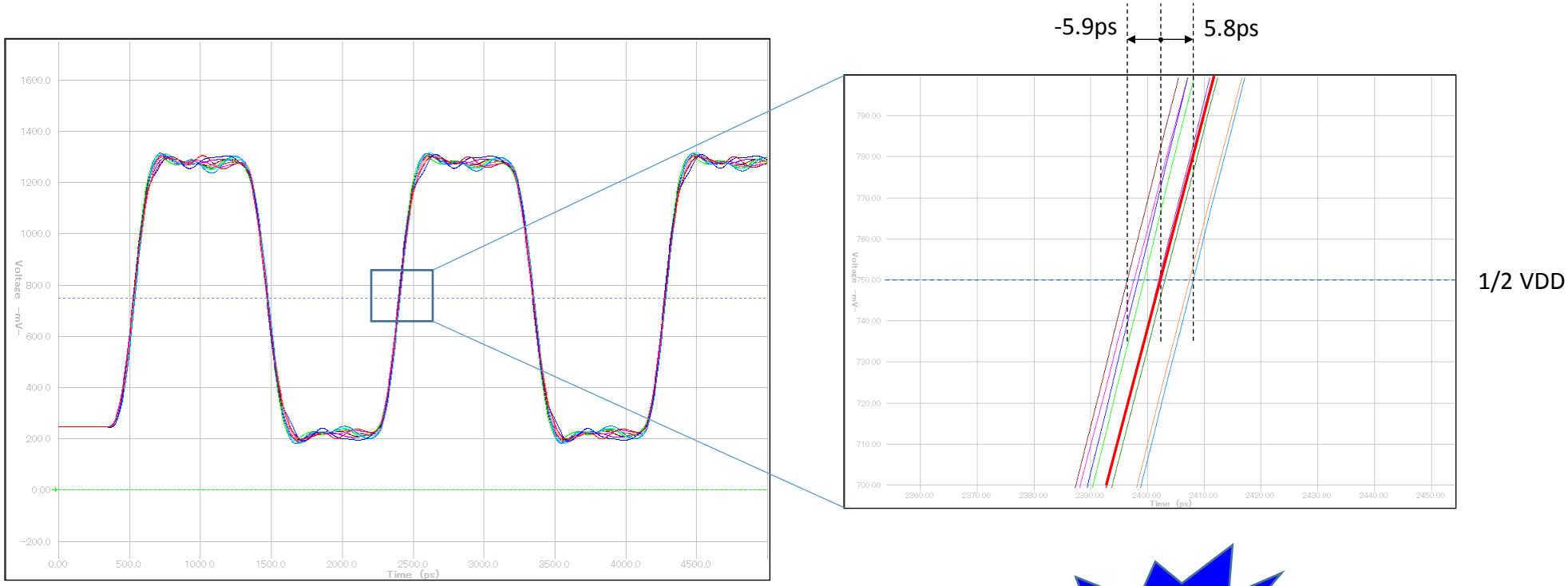


The results of delay adjustment in PKG + PCB

Adjust less than ±10ps skew considering PKG + PCB for each byte lane.



Simulation waveform after skew adjustment



SPEC ：±10ps against for DQS.
Simulation: -5.9ps to 5.8ps for DQS.

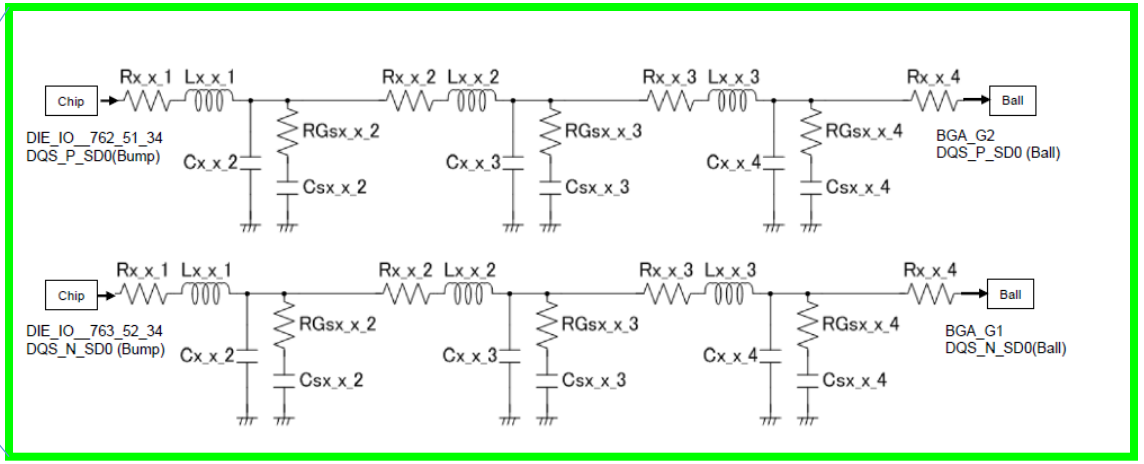
Pass

Using S-parameter for PKG model

IBIS S-parameter

I/O Buffer — PKG

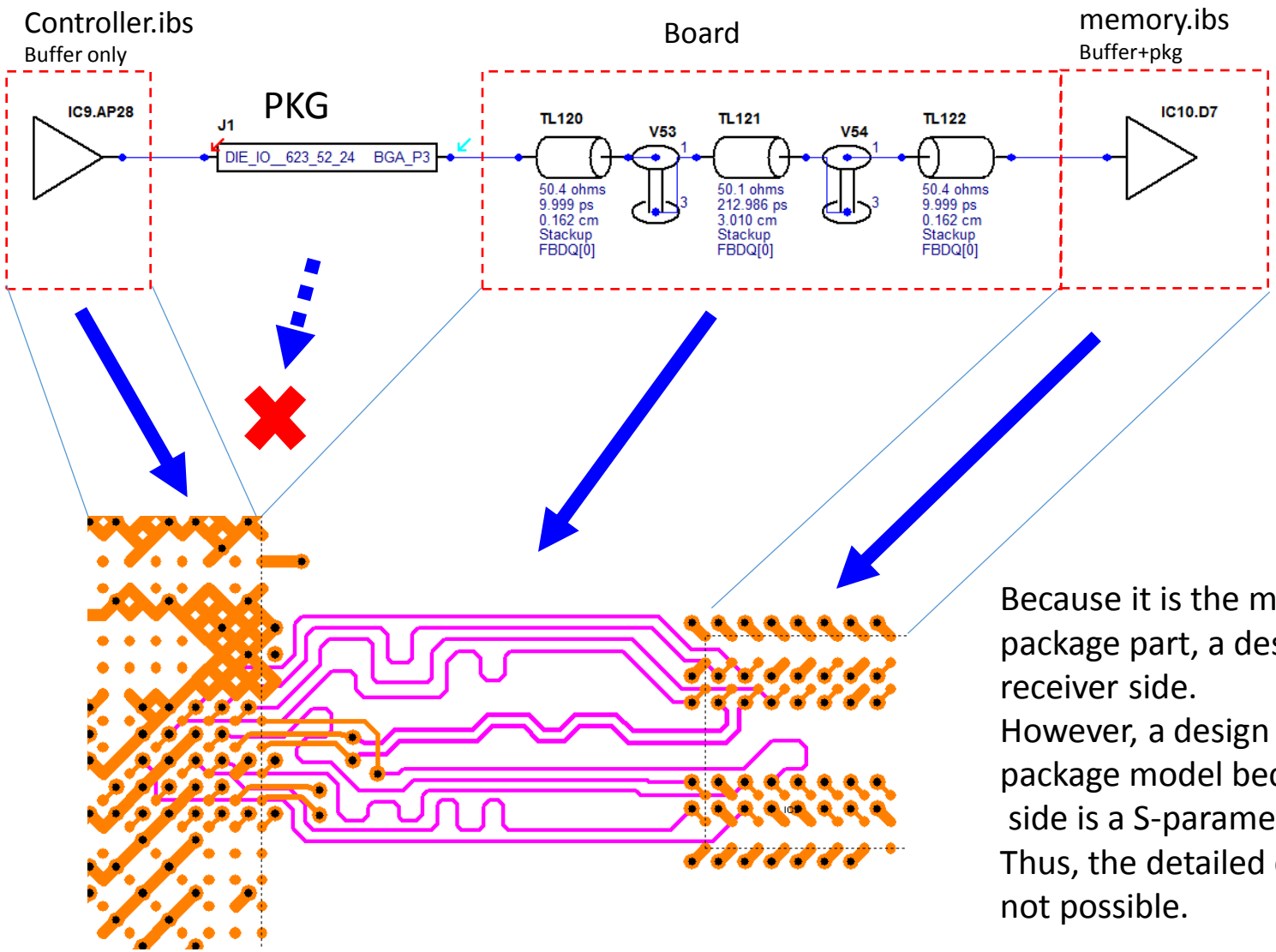
S-parameter consider the transmission-characteristic in frequency-domain.
But delay time can not be estimated by calculation.



Complicated

```
R66_66_1 DIE_IO__762_51_34 N_R66_66_1 0.181307
L66_66_1 N_R66_66_1 N_66_2 2.31553e-009
R66_66_2 N_66_2 N_R66_66_2 0.181307
L66_66_2 N_R66_66_2 N_66_3 2.38431e-009
R66_66_3 N_66_3 N_R66_66_3 0.181307
L66_66_3 N_R66_66_3 N_66_4 2.25772e-009
R66_66_4 N_66_4 N_R66_66_4 0.181307
L66_66_4 N_R66_66_4 BGA_G2 3.70628e-010
C66_66_2 N_66_2 Node__GND 4.9416e-013
RGs66_2 N_66_2 NCGs_66_2 7312.6
Cs66_2 NCGs_66_2 Node__GND 7.74022e-014
C66_66_3 N_66_3 Node__GND 6.32806e-013
RGs66_3 N_66_3 NCGs_66_3 7338.71
Cs66_3 NCGs_66_3 Node__GND 7.79633e-014
C66_66_4 N_66_4 Node__GND 1.00791e-012
RGs66_4 N_66_4 NCGs_66_4 7334.89
Cs66_4 NCGs_66_4 Node__GND 8.32936e-014
.
.
```

Using S-parameter for PKG model (continued)



Because it is the model including the package part, a design file can read the receiver side.
However, a design file cannot read a package model because the controller side is a S-parameter.
Thus, the detailed crosstalk analysis is not possible.

Conclusion

・In the actual PCB layout design such as DDR3 interface , crosstalk noise must be considered both on PKG and PCB.
However, to calculate the delay from IBIS RLC model and estimate the optimal trace length on PCB are effective in the early design stage.

・Therefore, propose to add the delay data of HS signals to IBIS model.

・PKG-PCB co-design becomes easy when there is delay data in the S-parameter at header section.

・Hope to EDA tool has a future option that can be extracted delay time from IBIS and S-parameter automatically. Then user can assign a constrained design rule easily to adjust skew !!